

HD404302/HD404304/ HD4074308

Description

The HD404302, HD404304, and HD4074308 are CMOS 4-bit single-chip microcomputers basically equivalent to the HMCS400 series, providing high programming productivity, high speed operation, and low power dissipation. They incorporate ROM, RAM, I/O, A/D converter, 2 timer/counters, including high voltage I/O pins to drive fluorescent display tubes directly. The HD404302 and HD404304 are mask ROM versions. The HD4074308 is a PROM version (ZTAT™ microcomputer).

Features

- 2048-word × 10-bit ROM (mask ROM version, HD404302)
4096-word × 10-bit ROM (HD404304)
8192-word × 10-bit ROM (ZTAT™ version)
- 160-digit × 4-bit RAM
- 33 I/O pins, including 25 high-voltage I/O pins (40 V max.)
- Two timer/counters
 - 11-bit prescaler
 - 8-bit timer (free-running timer/watch-dog timer)
 - 8-bit timer (auto-reload timer/event counter)
- Five interrupt sources
 - Two by external sources
 - Two by timer/counters
 - One by A/D converter

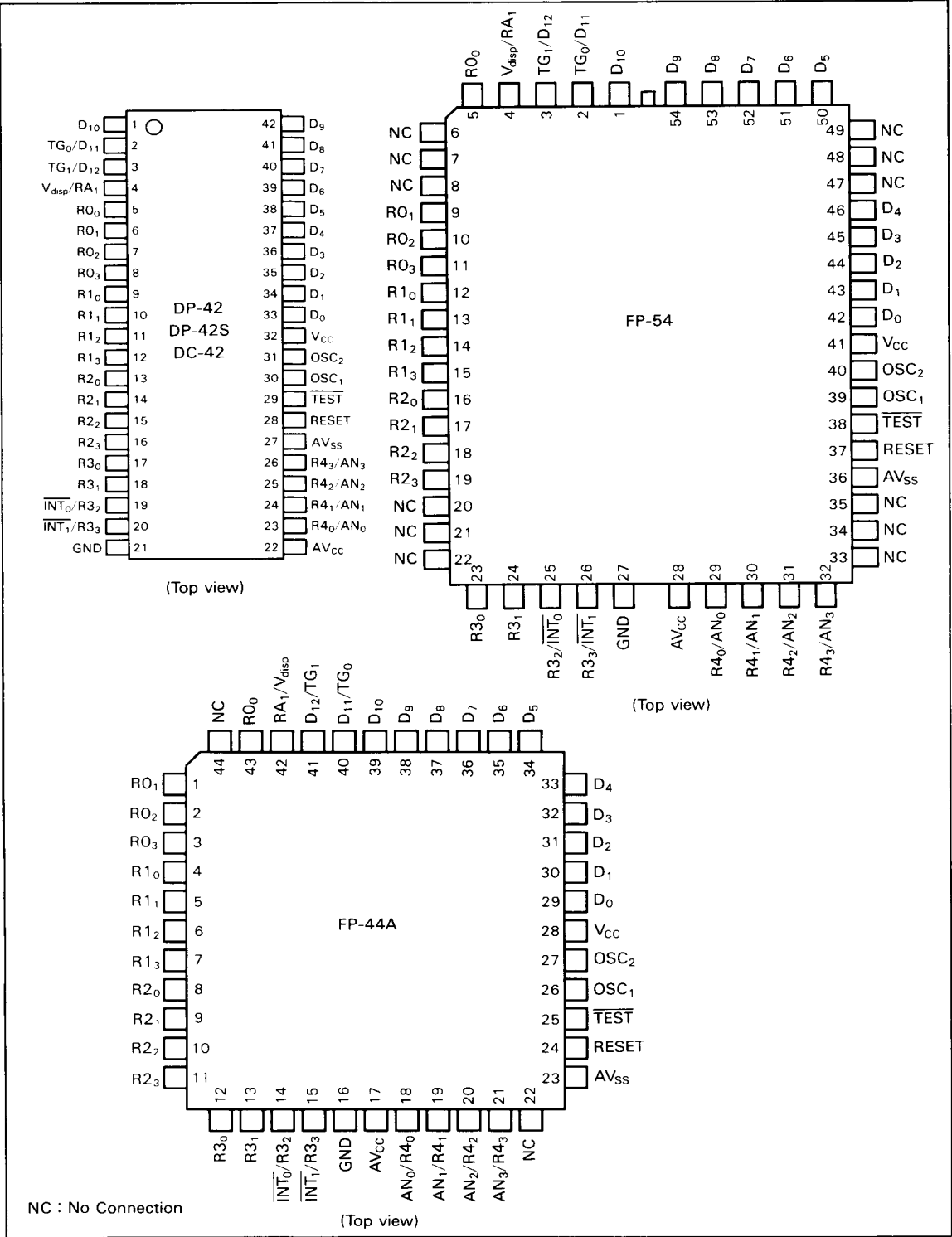
- 4-channel × 8-bit A/D converter
- Two tone generator outputs
- Subroutine stack, up to 16 levels including interrupts
- Two low-power dissipation modes
 - Standby mode
 - Stop mode
- On-chip oscillator
 - Crystal or ceramic filter
 - External clock
- Package
 - 42-pin plastic DIP (DP-42)
 - 42-pin ceramic DIP with window (DC-42)
 - 42-pin plastic shrink DIP (DP-42S)
 - 44-pin flat plastic package (FP-44A)
 - 54-pin flat plastic package (FP-54)
- Instruction cycle time: 2μs (f_{OSC} = 4 MHz)

Ordering Information

Type	Product Number	ROM (Words)	Package
Mask ROM	HD404302P	2,048	DP-42
	HD404302S		DP-42S
	HD404304P	4,096	DP-42
	HD404304S		DP-42S
	HD404304A*		FP-44A*
	HD404304F*		FP-54*
ZTAT™	HD4074308P	8,192	DP-42
	HD4074308S		DP-42S
	HD4074308C*		DC-42*
	HD4074308F*		FP-54*

Note: *Under development

Pin Arrangement



Pin Description

Pin Number					Pin Number				
DP-42, DP-42S, DC-42	FP-54	FP-44A	Pin Name	I/O	DP-42, DP-42S, DC-42	FP-54	FP-44A	Pin Name	I/O
1	1	39	D ₁₀	I/O	28	37	24	RESET	I
2	2	40	D ₁₁ /TG ₀	I/O	29	38	25	TEST	I
3	3	41	D ₁₂ /TG ₁	I	30	39	26	OSC ₁	I
4	4	42	RA ₁ /V _{disp}	I	31	40	27	OSC ₂	O
5	5	43	RO ₀	I/O	32	41	28	V _{CC}	
6	9	1	RO ₁	I/O	33	42	29	D ₀	I/O
7	10	2	RO ₂	I/O	34	43	30	D ₁	I/O
8	11	3	RO ₃	I/O	35	44	31	D ₂	I/O
9	12	4	R1 ₀	I/O	36	45	32	D ₃	I/O
10	13	5	R1 ₁	I/O	37	46	33	D ₄	I/O
11	14	6	R1 ₂	I/O	38	50	34	D ₅	I/O
12	15	7	R1 ₃	I/O	39	51	35	D ₆	I/O
13	16	8	R2 ₀	I/O	40	52	36	D ₇	I/O
14	17	9	R2 ₁	I/O	41	53	37	D ₈	I/O
15	18	10	R2 ₂	I/O	42	54	38	D ₉	I/O
16	19	11	R2 ₃	I/O	–	6	22	NC	
17	23	12	R3 ₀	I/O	–	7	44	NC	
18	24	13	R3 ₁	I/O	–	8	–	NC	
19	25	14	R3 ₂ /INT ₀	I/O	–	20	–	NC	
20	26	15	R3 ₃ /INT ₁	I/O	–	21	–	NC	
21	27	16	GND		–	22	–	NC	
22	28	17	AV _{CC}		–	33	–	NC	
23	29	18	R4 ₀ /AN ₀	I/O	–	34	–	NC	
24	30	19	R4 ₁ /AN ₁	I/O	–	35	–	NC	
25	31	20	R4 ₂ /AN ₂	I/O	–	47	–	NC	
26	32	21	R4 ₃ /AN ₃	I/O	–	48	–	NC	
27	36	23	AV _{SS}		–	49	–	NC	

NC: No connection

Pin Functions

Power Supply

V_{CC}: Apply power supply voltage to this pin.

GND: Connect to ground.

V_{dis}: This pin, multiplexed with RA₁, is for the power supply of the high-voltage output pins with a maximum voltage of V_{CC}-40 V. For details, see the Input/Output section.

AV_{CC}, AV_{SS}: Power supply pins for the A/D converter.

TEST: Non-user pin. Connect this pin to V_{CC}.

RESET: MCU reset pin. For details, see the Reset section.

Oscillators

OSC₁, OSC₂: Input pins for the internal oscillator circuit. They can be connected to a crystal resonator, ceramic filter resonator, or external oscillator circuit. For details, see the Internal Oscillator Circuit section.

Ports

D₀-D₁₂ (D Port): Input/output port addressed by its bits. These 13 pins are all high-voltage input/output pins. The circuit type for each pin can be selected using a mask

option. For details, see the Input/Output section.

R₀-R₃, R₁-R₁, R₂-R₂, R₃-R₃, R₄-R₄, RA₁ (R Ports): R₀ to R₄ are 4-bit I/O ports. RA is a 1-bit input-only port. The pins of R₀-R₂ and RA₁ are high-voltage pins, and the pins of R₃-R₄ are standard pins. R₃₂ and R₃₃ are multiplexed with INT₀ and INT₁, respectively. For details, see the Input/Output section.

Interrupts

INT₀, INT₁: External interrupt pins. INT₁ can be used as an external event input pin for timer B. INT₀ and INT₁ are multiplexed with R₃₂ and R₃₃, respectively. For details, see the Interrupt section.

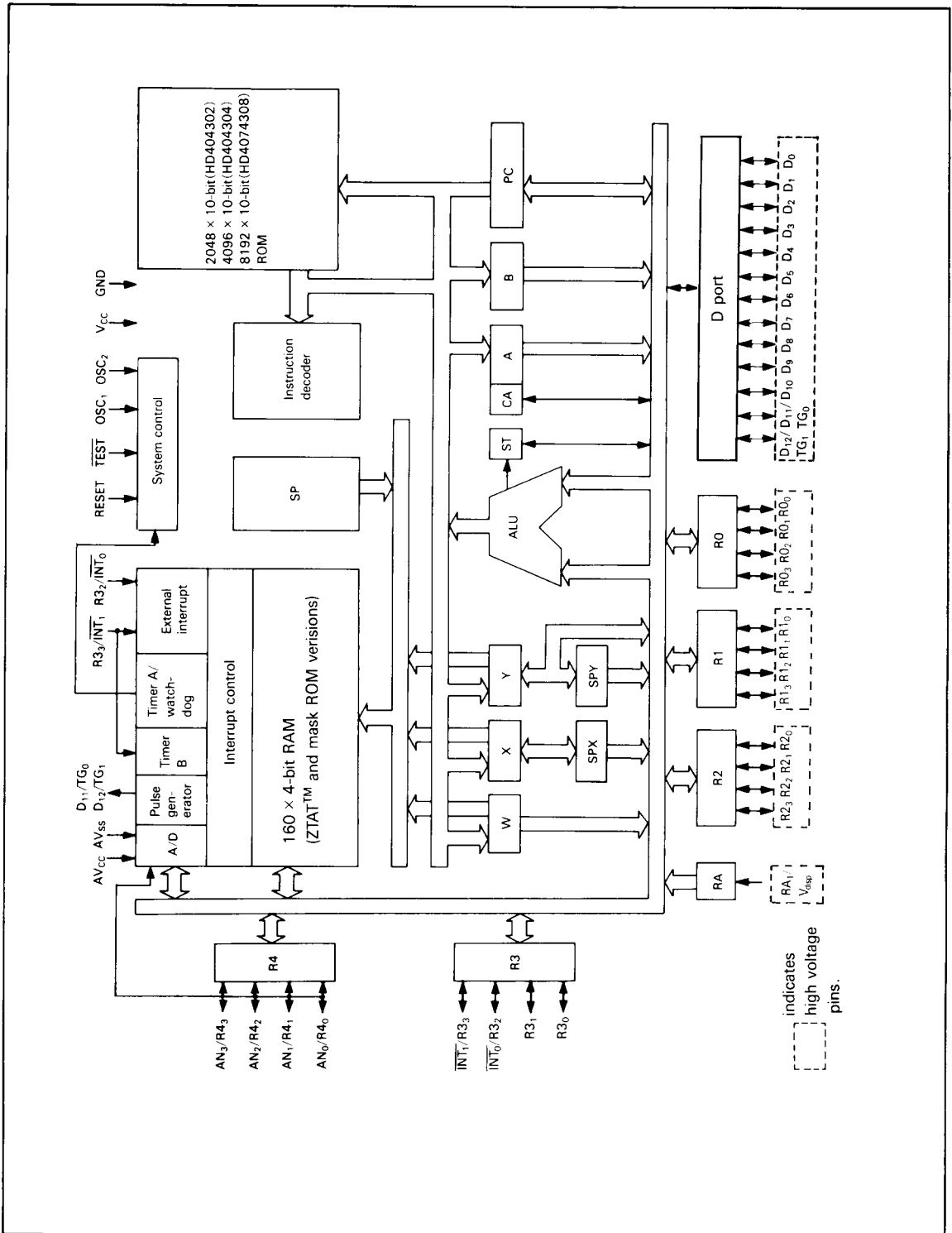
Tone Generator

TG₀, TG₁: Tone generator output pins. These pins are high-voltage pins multiplexed with D₁₁ and D₁₂, respectively.

A/D Converter

AN₀-AN₃ (AN Port): A/D converter input port. AN₀-AN₃ are multiplexed with R₄₀-R₄₃, respectively. For details, see the A/D Converter section.

Block Diagram



Memory Map

ROM Memory Map

The ROM is described in the following paragraphs with the ROM memory map in figure 1.

Vector Address Area (\$0000 to \$000F): Locations \$0000 through \$000F are reserved for JMPL instructions to branch to the starting address of the initialization program and the interrupt programs. After a reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area (\$0000 to

\$003F): Locations \$0000 through \$003F are reserved for subroutines. The CAL instruction branches to these subroutines.

Pattern Area (\$0000 to \$07FF: HD404302; \$0000 to \$0FFF: HD404304, HD4074308): Locations \$0000 through \$07FF or \$0FFF are reserved for ROM data. The P instruction allows reference to ROM data as a pattern.

Program Area (\$0000-\$07FF: HD404302; \$0000-\$0FFF: HD404304; \$0000-\$1FFF: HD4074308): Locations from \$0000 to \$1FFF can be used for program code.

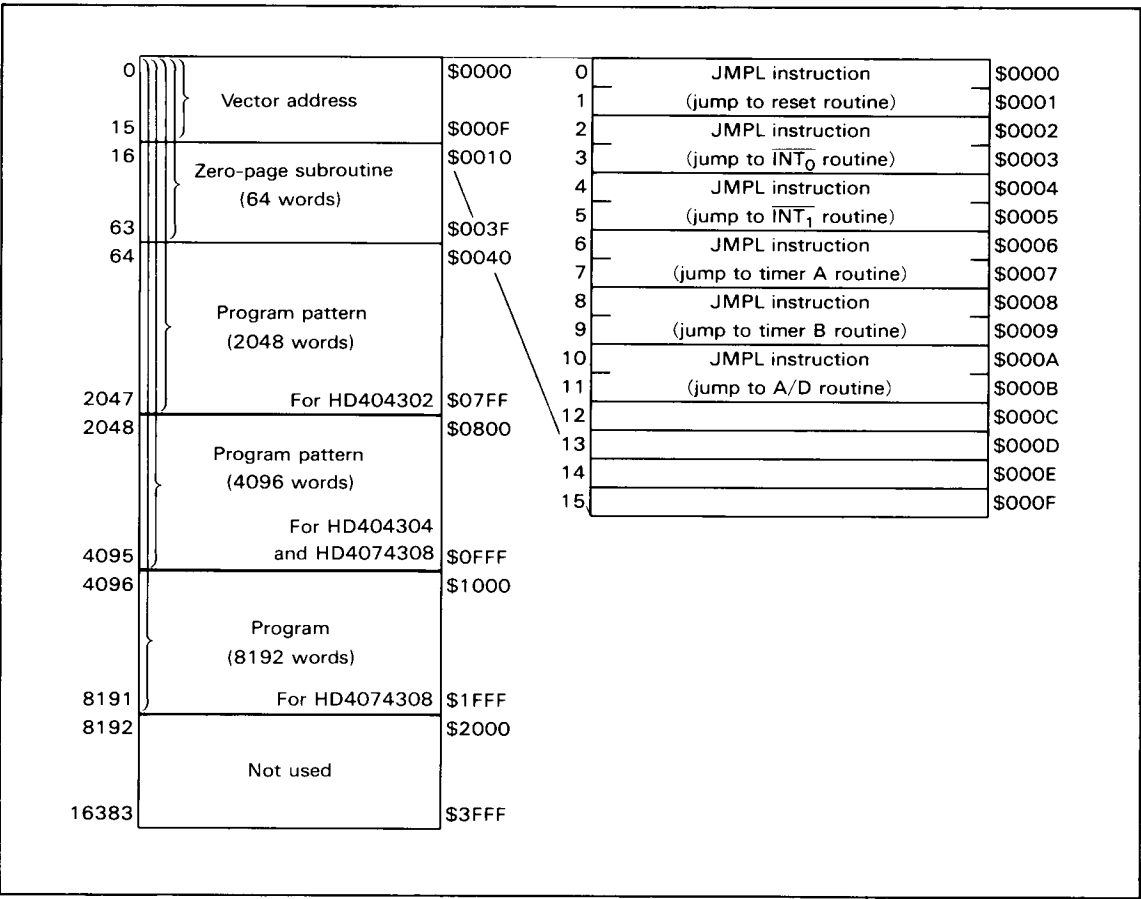


Figure 1 ROM Memory Map

RAM Memory Map

The MCU contains a 160-digit \times 4-bit RAM as the data and stack area. In addition to these areas, interrupt control bits and special function registers are also mapped on the RAM memory space. The RAM memory map (figure 2) is described in the following paragraphs.

Interrupt Control Bits Area (\$000 to \$003): The interrupt control bits area (figure 3) is used for interrupt control. It is accessible only by RAM bit manipulation instructions. However, the interrupt request flag cannot be set by software. The RSP bit is used only to reset the stack pointer.

Special Function Registers Area (\$004 to \$034): The special function registers are the mode or data registers for external interrupt, A/D conversion, and the timer/counters, and are the I/O port data control registers. These registers are classified into three types: write-only, read-only, and read/write as shown in

figure 2. These registers cannot be accessed by RAM bit manipulation instructions. However, WDON (\$020) can be accessed only by those bit instructions.

Data Area (\$040 to \$09F): The 16 digits of \$040 through \$04F are called memory registers (MR) and are accessible by the LAMR and XMRA instructions (figure 4).

Stack Area (\$3C0 to \$3FF): Locations \$3C0 through \$3FF are reserved for the stack area to save the contents of the program counter (PC), status flag (ST), and carry flag (CA) when subroutine calls (CAL and CALL instructions) and interrupts are processed. This area can be used as a 16-level nesting stack in which one level requires 4 digits. Figure 4 shows the save condition. The program counter is restored by the RTN and RTNI instructions. The status and carry flags are restored only by the RTNI instruction. This area, when not used as a stack, is available as a data area.

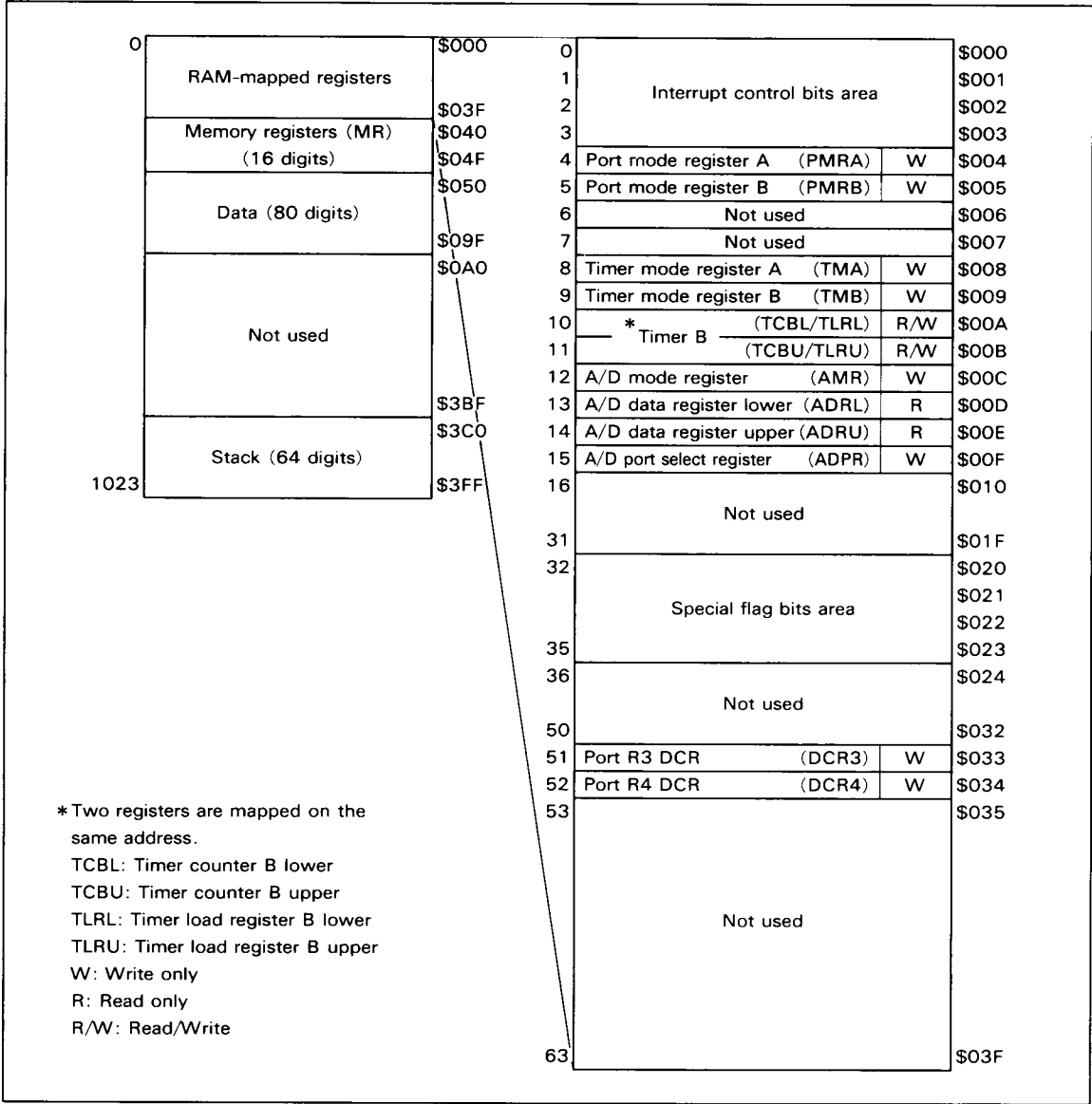


Figure 2 RAM Memory Map

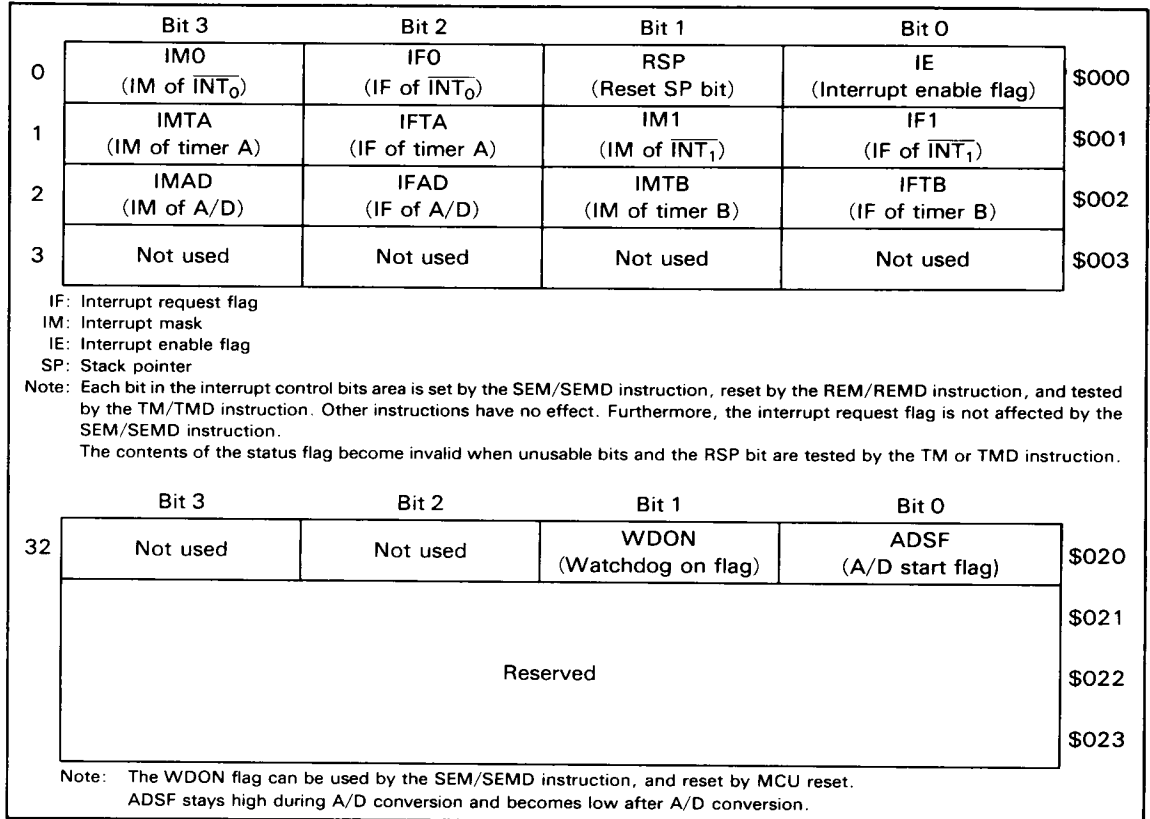


Figure 3 Configuration of Interrupt Control Bits Area

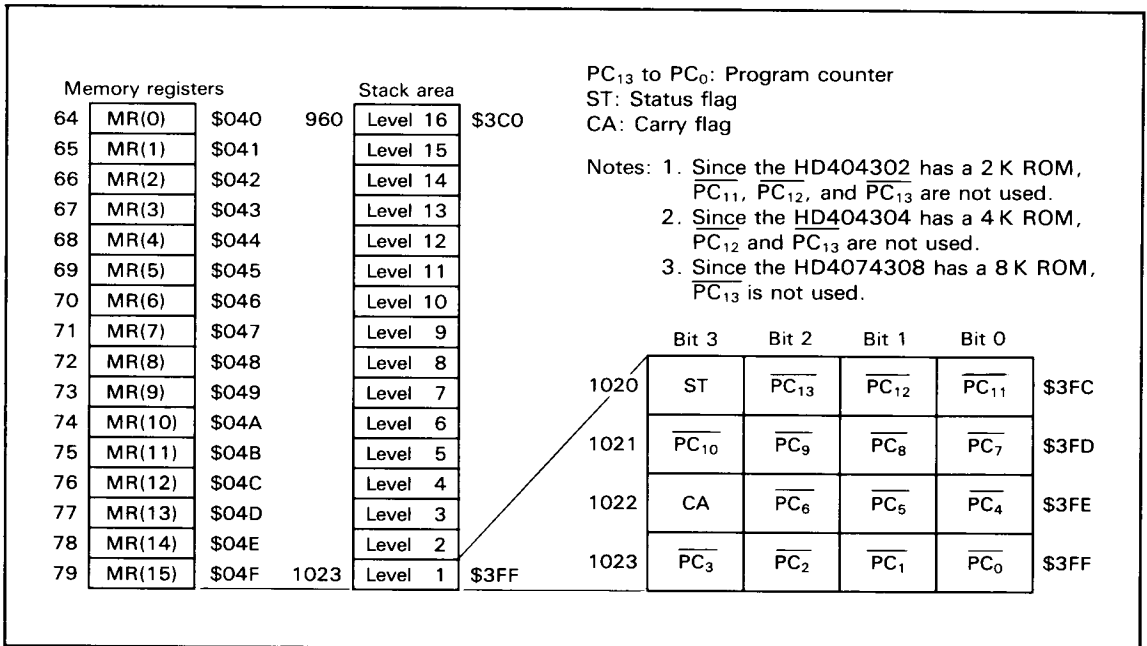


Figure 4 Configuration of Memory Registers, Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. The following paragraphs describe the registers and flags shown in figure 5 in detail.

Accumulator (A), B Register (B): The 4-bit accumulator and B register hold the results from the arithmetic logic unit (ALU) as well as the transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): The 2-bit W register and the 4-bit X and Y registers indirectly address the RAM. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): The 4-bit SPX and SPY registers are used to assist the X and Y registers, respectively.

Carry Flag (CA): The carry flag (CA) indicates an overflow generated from the ALU during arithmetic operation. It is also affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Status Flag (ST): The status flag (ST) indicates an ALU overflow and ALU non-zero during arithmetic or compare instructions, and the result of a bit test instruction. Moreover, the status flag controls branching caused by the BR, BRL, CAL, or CALL instruction. Whether these instructions are executed or skipped, the status flag is always set to 1. The state of this flag remains unchanged until the next arithmetic, compare, bit test, or branch instruction is executed. During an interrupt, ST is pushed onto the stack, and popped off the stack by the RTNI instruction. This flag is not affected by the RTN instruction.

Program Counter (PC): The program counter is a 14-bit binary counter which holds the address of the next program instruction to be executed.

Stack Pointer (SP): The stack pointer (SP) is a 10-bit register which indicates the next stack address. This pointer, which is initialized to \$3FF, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped off the stack. The highest four bits are fixed to 1111, which allows the pointer to indicate up to 16 levels of subroutines. The stack pointer is initialized when the MCU is reset or the RSP bit (\$000, bit 1) is reset by the REM or REMD instruction.

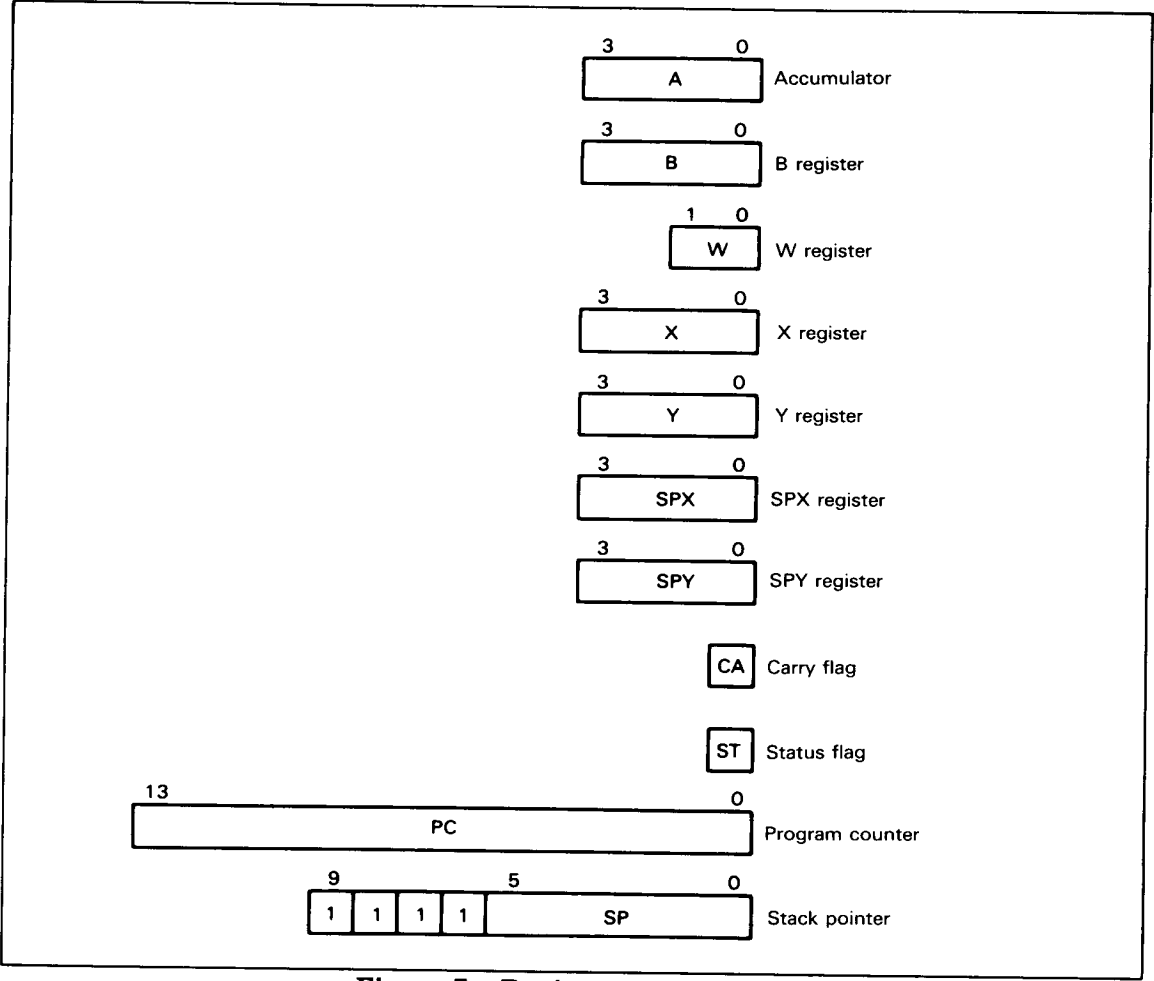


Figure 5 Registers and Flags

Interrupts

Five interrupt sources are available on the MCU: external requests ($\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$), timer/counters (timer A, timer B), and A/D. For each source, the interrupt request flag (IF), interrupt mask (IM), and interrupt vector addresses are provided to control and maintain the interrupt request. The interrupt enable flag (IE) is also used to control interrupt operations.

Interrupt Control Bits and Interrupt Service:

The interrupt control bits are mapped on \$000 through \$003 of the RAM space. They are accessible by RAM bit manipulation instructions. However, the interrupt request flag (IF) cannot be set by software. The interrupt enable flag (IE) and IF are cleared to 0, and the interrupt mask (IM) is set to 1 after MCU reset.

Figure 6 is a block diagram of the interrupt control circuit. Table 1 shows the interrupt priority and vector addresses, and table 2

shows the interrupt conditions corresponding to each interrupt source. The interrupt request is generated when the IF is set to 1 and IM is 0. If the IE is 1 at this time, the interrupt will be activated and vector addresses will be generated from the priority PLA corresponding to the interrupt sources.

Figure 7 shows the interrupt processing sequence, and figure 8 shows the interrupt processing flowchart. If an interrupt is requested, the instruction being executed finishes in the first cycle. The IE is reset in the second cycle. In the second and third cycles, the carry flag, status flag, and program counter are pushed onto the stack. In the third cycle, the instruction is re-executed, after jumping to the vector address.

At each vector address, program the JMPL instruction to branch to the starting address of the interrupt program. The IF which caused the interrupt must be reset by software in the interrupt program.

Table 1 Vector Addresses and Interrupt Priority

Reset/Interrupt	Priority	Vector Addresses
RESET	—	\$0000
$\overline{\text{INT}}_0$	1	\$0002
$\overline{\text{INT}}_1$	2	\$0004
Timer A	3	\$0006
Timer B	4	\$0008
A/D	5	\$000A

Table 2 Interrupt Conditions

Interrupt Control Bit	$\overline{\text{INT}}_0$	$\overline{\text{INT}}_1$	Timer A	Timer B	A/D
IE	1	1	1	1	1
$\text{IFO} \cdot \overline{\text{IMO}}$	1	0	0	0	0
$\text{IF1} \cdot \overline{\text{IM1}}$	*	1	0	0	0
$\text{IFTA} \cdot \overline{\text{IMTA}}$	*	*	1	0	0
$\text{IFTB} \cdot \overline{\text{IMTB}}$	*	*	*	1	0
$\text{IFAD} \cdot \overline{\text{IMAD}}$	*	*	*	*	1

*: Don't care

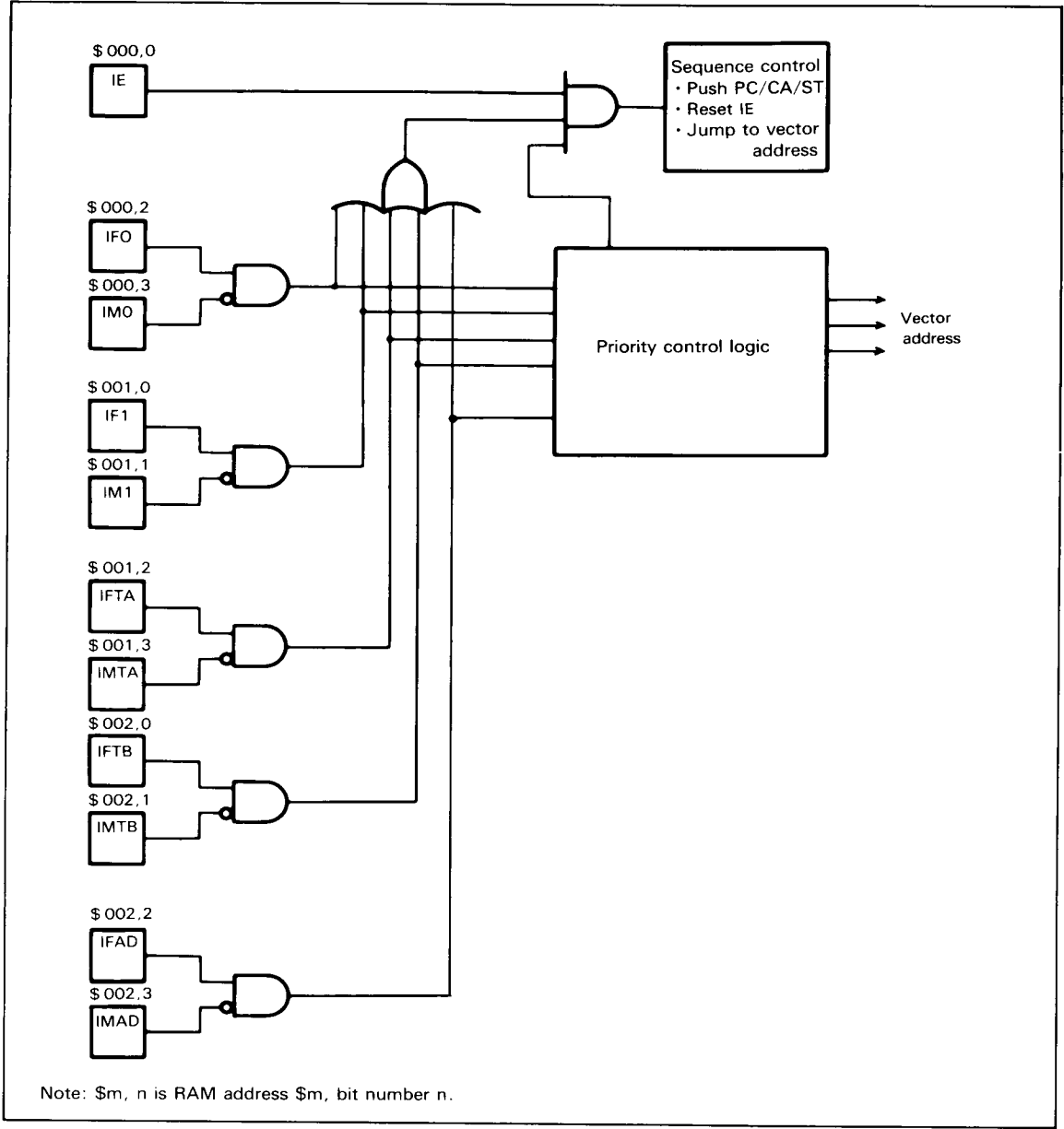


Figure 6 Interrupt Control Circuit Block Diagram

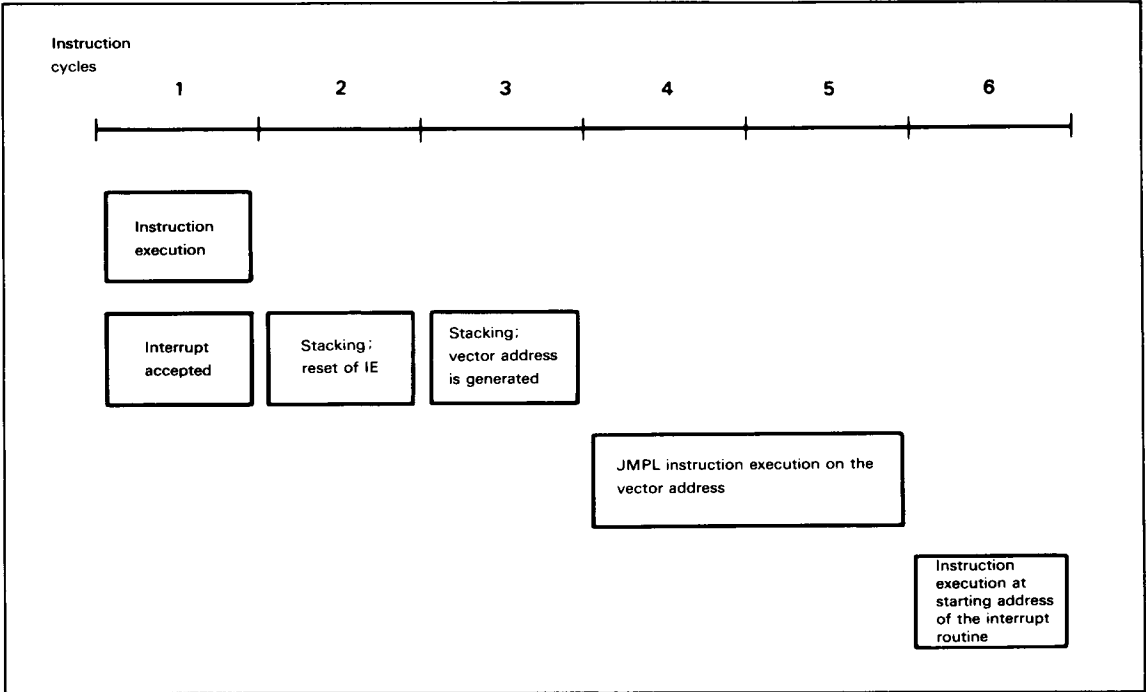


Figure 7 Interrupt Processing Sequence

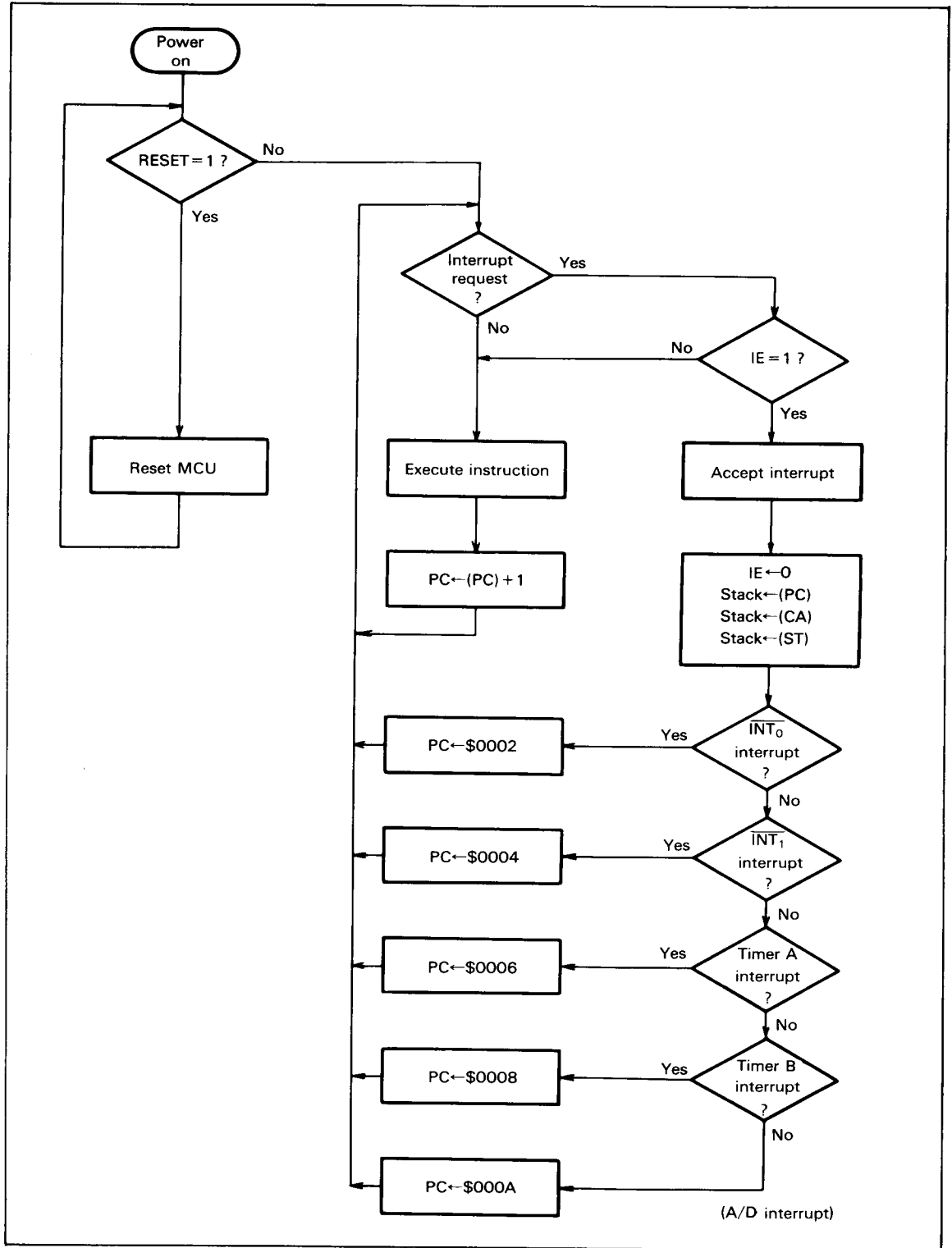


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: \$000, Bit 0): The interrupt enable flag enables/disables interrupt requests. It is reset by an interrupt and set by the RTNI instruction.

External Interrupts ($\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$): The external interrupt request inputs ($\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$) can be selected by port mode register A (PMRA: \$004) (figure 10).

The external interrupt request flags (IF0, IF1) are set at the falling edge of $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ inputs, respectively.

The $\overline{\text{INT}}_1$ input can be used as a clock signal input to timer B. Timer B is incremented at each falling edge of the $\overline{\text{INT}}_1$. When using $\overline{\text{INT}}_1$ as the timer B external event input, the external interrupt mask (IM1) must be set so that the interrupt request by $\overline{\text{INT}}_1$ will not be accepted. Figure 9 shows the interrupt mode register.

External Interrupt Request Flags (IF0: \$000, Bit 2; IF1: \$001, Bit 0): The external interrupt request flags (IF0, IF1) (figure 9) are set at the falling edge of the $\overline{\text{INT}}_0$ and $\overline{\text{INT}}_1$ inputs, respectively.

External Interrupt Masks (IM0: \$000, Bit 3; IM1: \$001, Bit 1): The external interrupt mask bits (figure 9) mask an interrupt request caused by the external interrupt request flags.

Port Mode Register A (PMRA: \$004): Port mode register A is a 4-bit write-only register which controls the R3₂/ $\overline{\text{INT}}_0$ pin and R3₃/ $\overline{\text{INT}}_1$ pin as shown in figure 10. Port mode register A will be initialized to \$0 by MCU reset.

Timer A Interrupt Request Flag (IFTA: \$001, Bit 2): The timer A interrupt request flag (figure 9) is set when an overflow occurs in timer A.

Timer A Interrupt Mask (IMTA: 001, Bit 3): The timer A interrupt mask bit (figure 9) masks an interrupt request caused by the timer A interrupt request flag.

Timer B Interrupt Request Flag (IFTB: \$002, Bit 0): The timer B interrupt request flag (figure 9) is set when an overflow occurs in timer B.

Timer B Interrupt Mask (IMTB: \$002, Bit 1): The timer B interrupt mask bit (figure 9) masks an interrupt request caused by the timer B interrupt request flag.

A/D Interrupt Request Flag (IFAD: \$002, Bit 2): The A/D interrupt request flag (figure 9) is set when an A/D conversion is completed.

A/D Interrupt Mask (IMAD: \$002, Bit 3): The A/D interrupt mask bit (figure 9) masks an interrupt request caused by the A/D interrupt request flag.

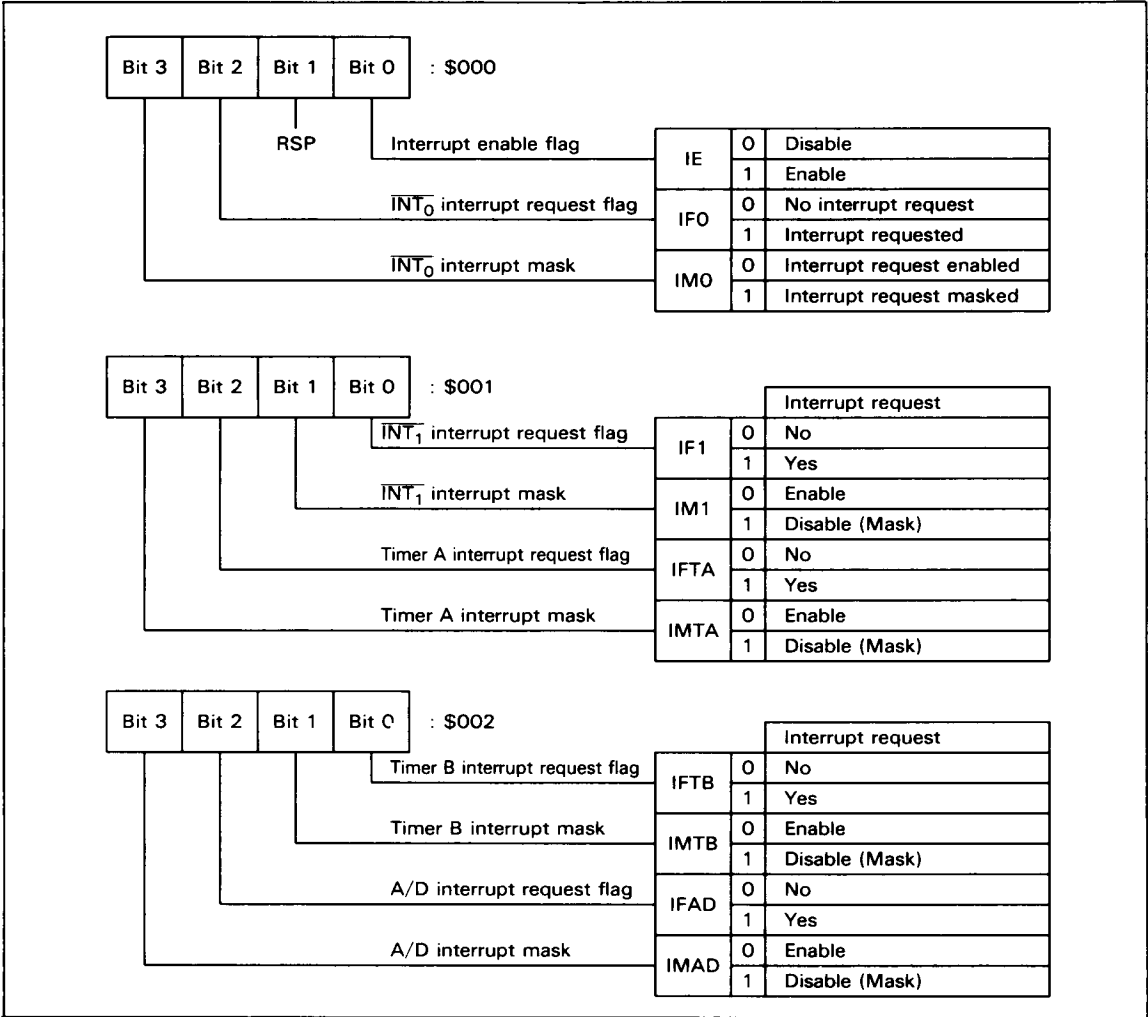


Figure 9 Interrupt Control Bits

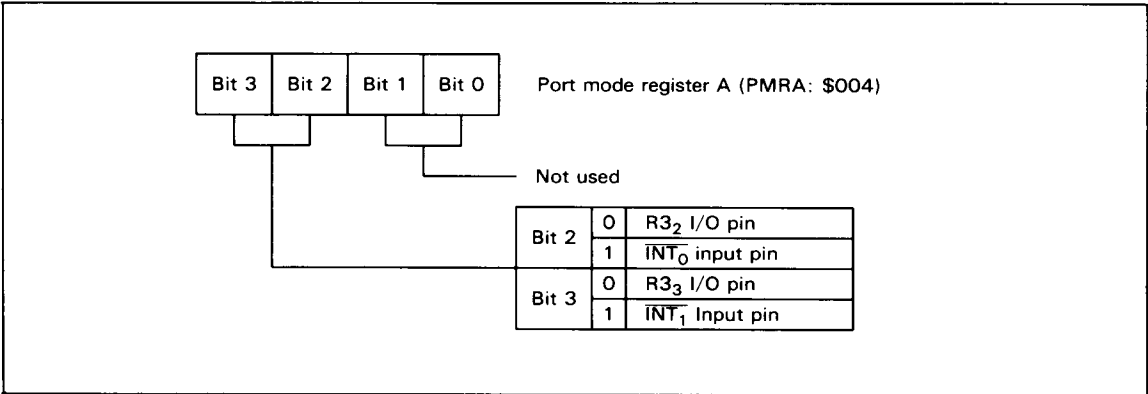


Figure 10 Port Mode Register A

Timers

The MCU contains a prescaler and two timer/counters (timers A and B) as shown by the block diagram in figure 11.

Prescaler: The input to the prescaler is the system clock signal. The prescaler is initialized to \$000 by MCU reset or by setting bit 3 of timer mode register A (TMA: \$008) when the watchdog timer on flag (WDON: \$020, bit 1) is 0, after which the prescaler starts to divide the system clock. It continues operation until MCU reset or stop mode occurs.

The pulse frequency of timer A input clock, timer B input clock, and the tone generator outputs (TG₀, TG₁) are selected among prescaler outputs by timer mode register A (TMA: \$008), timer mode register B (TMB: \$009), and port mode register B (PMRB: \$005), respectively.

After MCU reset, WDON is 0. Thus, when timer A is reset by setting bit 3 of timer mode register A (TMA) when the watchdog timer is off, the prescaler is also reset, which affects the operation of timer B and the tone generator outputs (TG₀, TG₁). Consequently, the program should control these conditions.

Timer A operation: Timer A is an 8-bit interval timer which can be used also as a watchdog timer. The prescaler divide ratio of timer A is selected by timer mode register A (TMA: \$008).

After timer A is initialized to \$00 by MCU reset or setting bit 3 of timer mode register A (TMA: \$008), it is incremented at every clock input signal. Eight different clock signals,

divided by the prescaler, can be used as an input clock. The clock input signals to timer A are selected by timer mode register A. When the next clock signal is applied after timer A becomes \$FF, an overflow is generated and timer A is reset to \$00. This overflow causes the timer A interrupt request flag (IFTA: \$001, bit 2) to go to 1.

This timer can function as a watchdog timer to detect a runaway program. The MCU is reset when an overflow output is generated from a timer counter that cannot be controlled due to a runaway program while the watchdog timer on flag (WDON) is 1.

Timer B operation: Timer mode register B (TMB: \$009) selects the auto-reload function, input clock source, and the prescaler divide ratio for timer B. When an external event input is used as an input clock signal to timer B, select R3₃ /INT₁ as INT₁ by setting port mode register A (PMRA: \$004), and set the external interrupt mask (IM1) to prevent an external interrupt request from occurring.

Timer B is initialized according to data written into timer load register B by software. Timer B is incremented at every clock input signal. When the next clock signal is applied to timer B after it is set to \$FF, it will generate an overflow output. In this case, if the auto-reload function is selected, timer B is initialized according to the value of timer load register B. If it is not selected, timer B is reset to \$00. The timer B interrupt request flag (IFTB: \$002, bit 0) will be set at this overflow output.

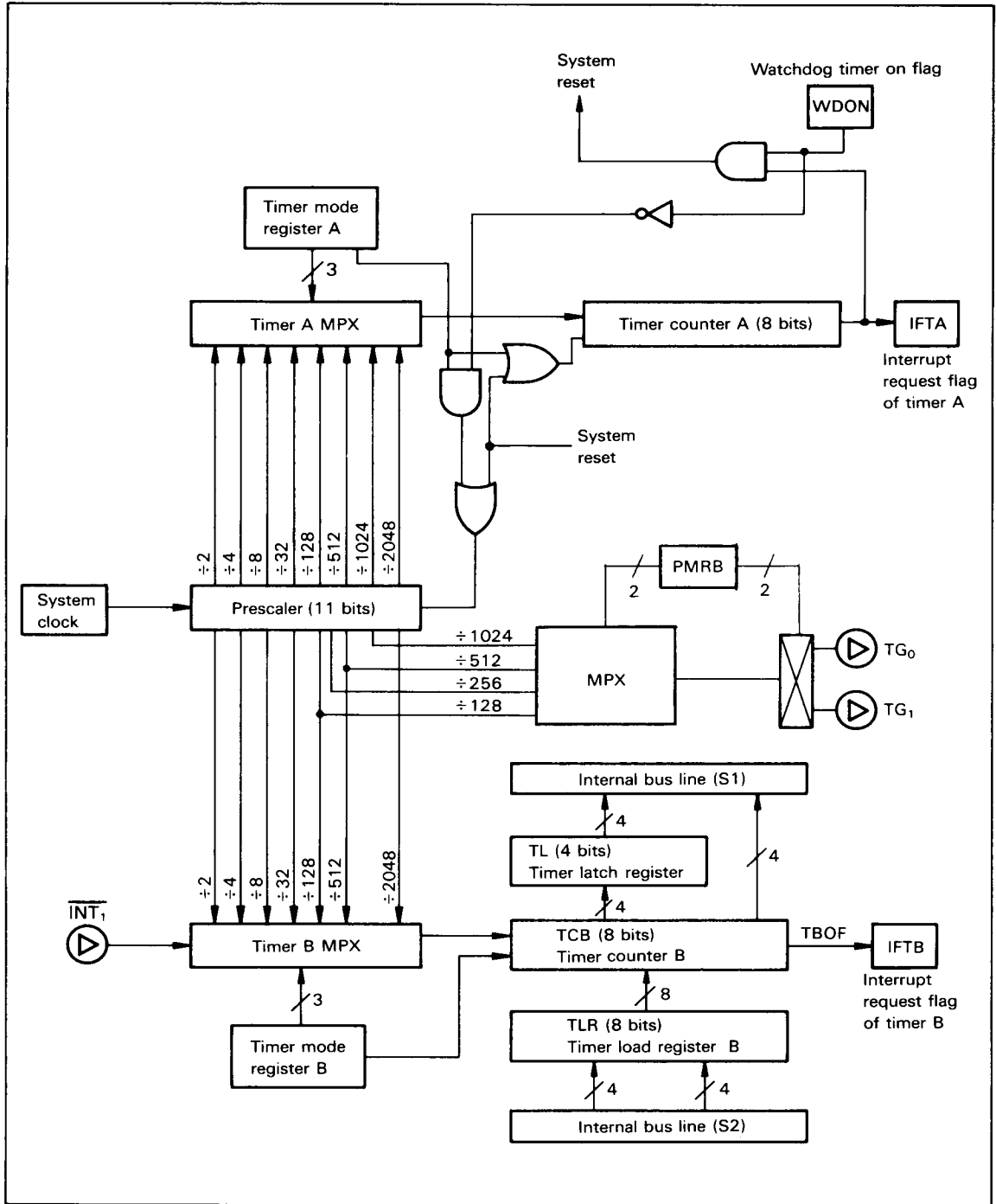


Figure 11 Timers A and B Block Diagram

Timer Mode Register A (TMA: \$008):
Timer mode register A is a 4-bit write-only register. Bits 0 to 2 of TMA control the prescaler divide ratio of the timer counter A clock input, as shown in figure 12. Bit 3 resets timer A when set to 1; if WDON = 0, the prescaler is

also reset. Bit 3 retains a 1 for only one instruction cycle.

Timer mode register A can be modified from the second instruction cycle of the write instruction.

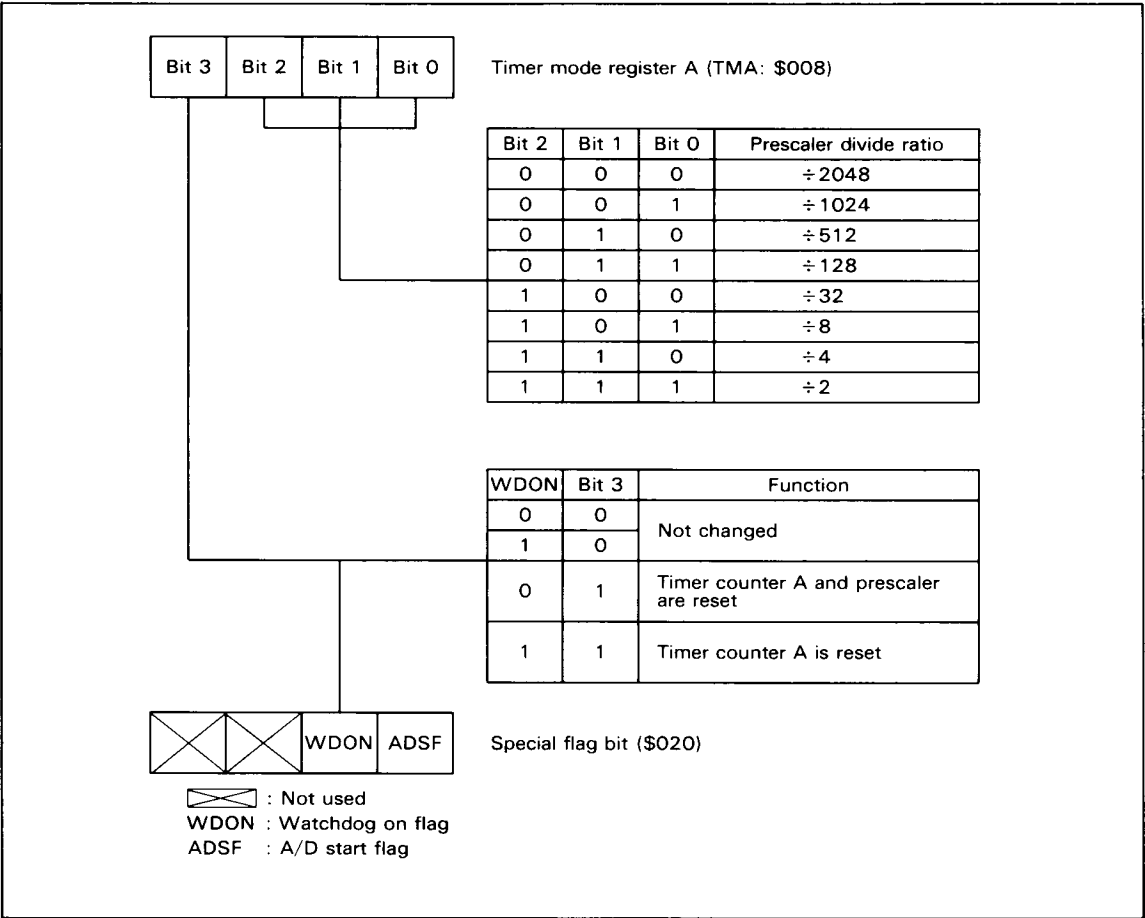


Figure 12 Timer Mode Register A Configuration

Timer Mode Register B (TMB: \$009):

Timer mode register B is a 4-bit write-only register which selects the auto-reload function, the prescaler divide ratio, and the source of the clock input signal, as shown in figure 13. Timer mode register B is initialized to \$0 by MCU reset.

The operation mode of timer B can be modified from the second instruction cycle after timer mode register B is written to. The initialization of timer B by a write to the timer load register should be performed after the contents of timer mode register B have been appropriately changed.

Timer B (TCBL: \$00A, TCBU: \$00B, TLRL: \$00A, TLRU: \$00B): Timer B consists of an 8-bit write-only timer load register, and an 8-bit

read-only timer counter. Each of them has a low-order digit (TCBL: \$00A, TLRL: \$00A) and a high-order digit (TCBU: \$00B, TLRU: \$00B).

Timer counter B can be initialized by writing data into timer load register B. In this case, write the low-order digit first, and then the high-order digit. The timer counter is initialized when the high-order digit is written. The timer load register is initialized to \$00 by MCU reset.

The counter value of timer B can be obtained by reading timer counter B. In this case, read the high-order digit first, and then the low-order digit. The count value of the low-order digit is latched when the high-order digit is read.

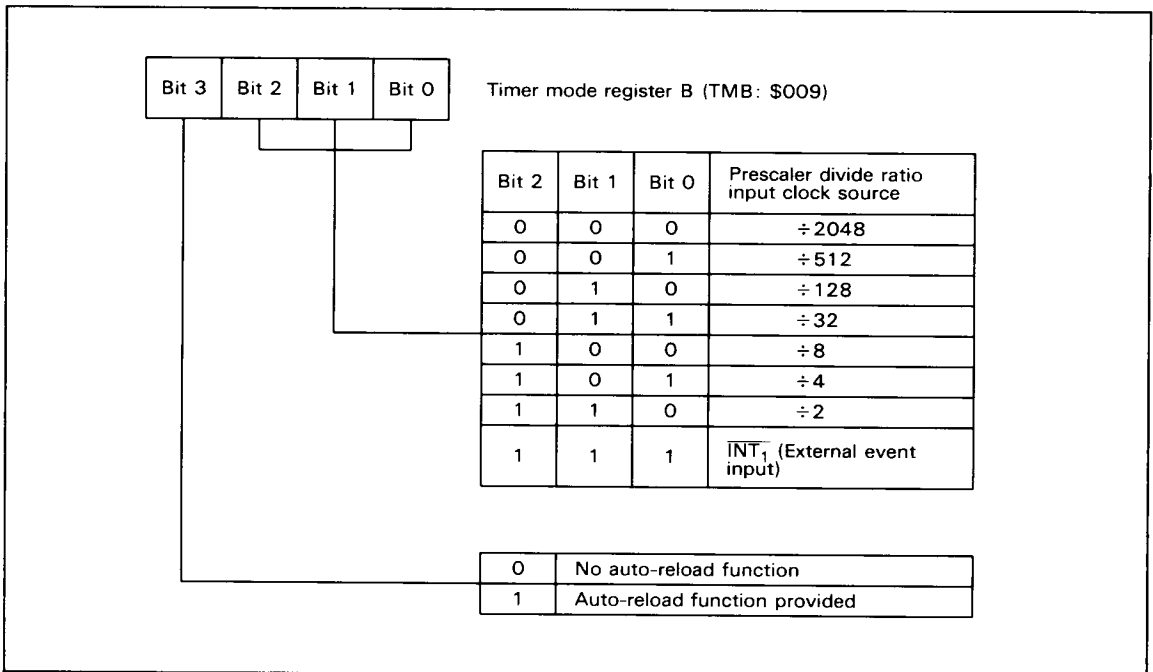


Figure 13 Timer Mode Register B Configuration

Timer A Interrupt Request Flag (IFTA: \$001, Bit 2): The timer A interrupt request flag (figure 14) is set by the overflow output of timer A. When the watchdog timer function is selected, the timer interrupt request flag is not set since the MCU is reset by an overflow output.

Timer A Interrupt Mask (IMTA: \$001, Bit 3): The timer A interrupt mask (figure 14) prevents an interrupt request from being generated by the timer A interrupt request

flag.

Timer B Interrupt Request Flag (IFTB: \$002, Bit 0): The timer B interrupt request flag (figure 14) is set by the overflow output of timer B.

Timer B Interrupt Mask (IMTB: \$002, Bit 1): The timer B interrupt mask (figure 14) prevents an interrupt request from being generated by the timer B interrupt request

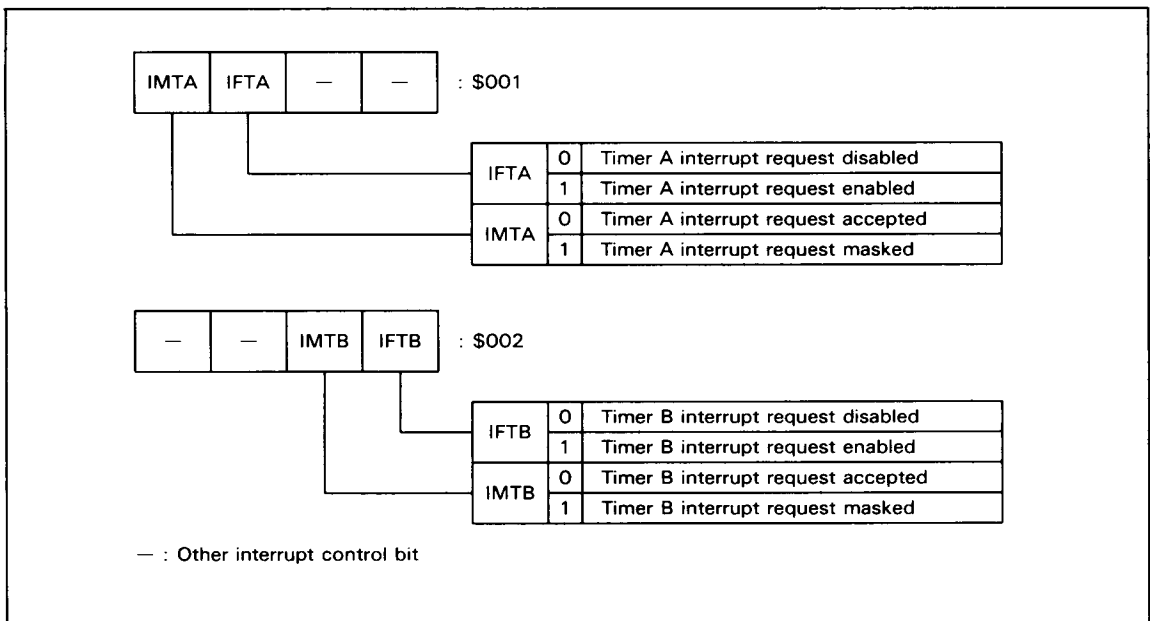


Figure 14 Timer Interrupt Control Bits

A/D Converter

The HD404302, HD404304, and HD4074308 incorporate a sequential comparison system A/D converter consisting of a resistor ladder. It can measure four analog inputs with 8-bit resolution. Figure 15 shows the A/D converter block diagram. The A/D converter consists of the following registers:

- A/D mode register (4 bits)
- A/D start flag (1 bit)
- A/D port select register (4 bits)
- A/D data register (4 bits + 4 bits)

A/D Mode Register (AMR): The A/D mode register (figure 16) is a 4-bit write-only register which selects the A/D conversion speed (bit 0, bit 1) and analog input channel (bit 2, bit 3).

A/D Start Flag (ADSF): A/D conversion is started when a 1 is written to the A/D start flag (figure 16). After a conversion is completed, the conversion data is set in the A/D data register and the A/D start flag is cleared simultaneously.

Note that the bit manipulation instruction SEM or SEMD should be used to write data to ADSF. During A/D conversion, ADSF must not be written to.

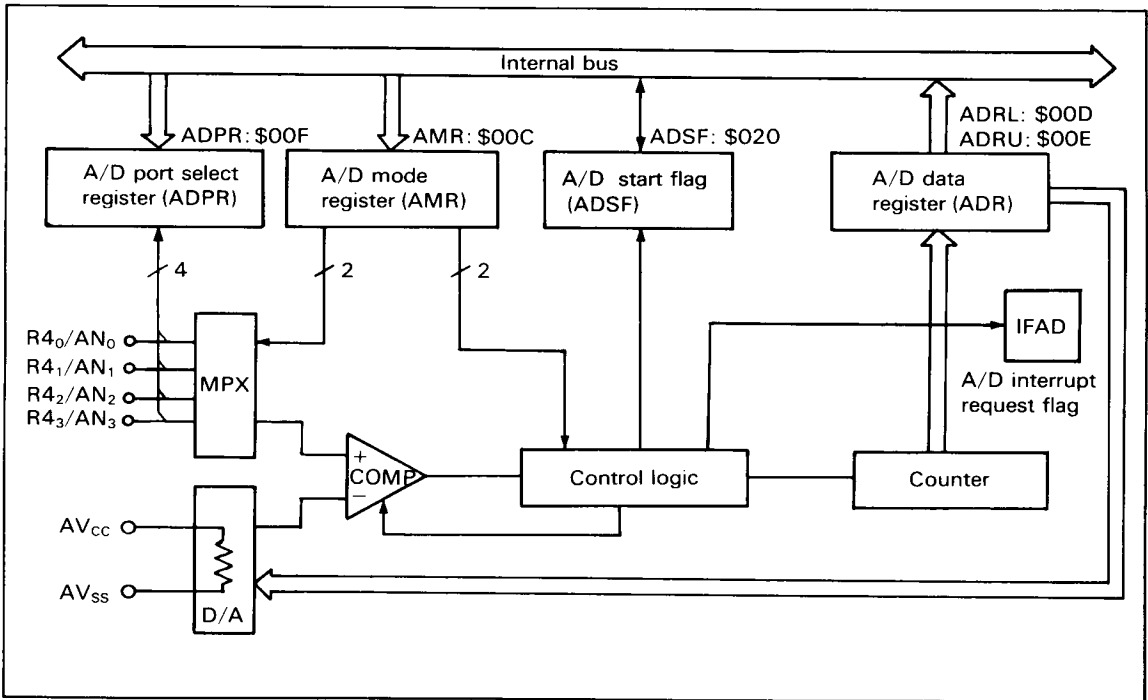


Figure 15 A/D Converter Block Diagram

A/D Port Select Register (ADPR): The only register which selects the digital port and analog port.

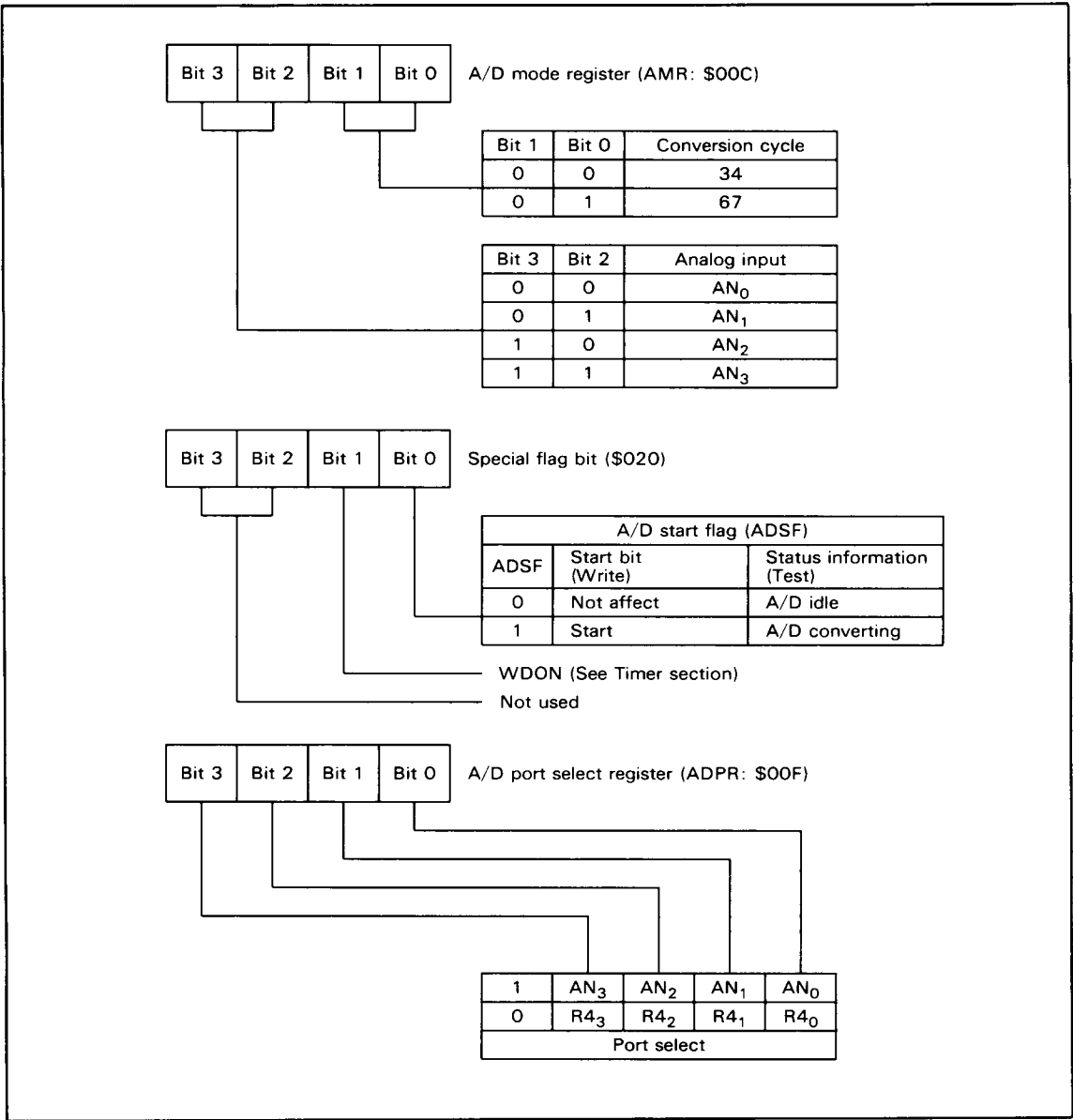


Figure 16 A/D Register Configuration

A/D Data Register (ADRL: \$00D, ADRU: \$00E): The A/D data register (figure 17) is a 4-bit/4-bit read-only register in which the 8-bit conversion result is set after completing A/D conversion. The data is preserved until the next conversion begins. Data read is not guaranteed during A/D conversion. The A/D data register is initialized to \$80 by the MCU reset.

Precautions on using the A/D converter:

- If a digital signal is input to the R4₀-R4₃ or adjacent pins during A/D conversion, conversion accuracy may be affected.
- Data in the A/D data register is not guaranteed during A/D conversion.
- Port output instructions should not be executed during A/D conversion to allow for a stable A/D converter operation.

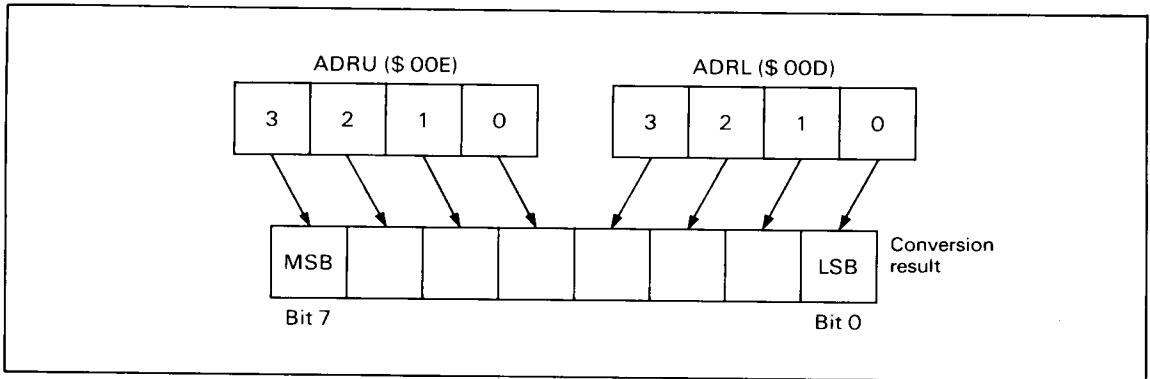


Figure 17 A/D Data Register Configuration

Input/Output

The MCU has 33 I/O pins, 25 being high-voltage pins. The on/off status of the output buffers of the standard pins (figure 19) is controlled by the combinations of the value of the port register (PDR) and data control register (DCR).

D Port: The D port is an I/O port which has 13 discrete I/O pins, each of which can be addressed independently. It can be set/reset through the SED/RED and SEDD/REDD instructions, and can be tested through the TD and TDD instructions. Furthermore, the contents of the status flag become invalid when the unused ports are tested. D_{11} and D_{12} ports are multiplexed with tone generator pins TG_0 and TG_1 , respectively. The circuit type of the D port is shown in table 3.

R Ports: The R ports are composed of 20 I/O pins and one input-only pin. Data is input through the LAR and LBR instructions and output through the LRA and LRB instructions. The MCU will not be affected by writing into the input-only and non-existing ports. The on/off status of the output buffers of the R3 and R4 ports are controlled by the R port data control register (DCR3, DCR4). R_{32} and R_{33} are multiplexed with \overline{INT}_0 and \overline{INT}_1 , respectively. R_{40} , R_{41} , R_{42} , and R_{43} pins are

multiplexed with AN_0 , AN_1 , AN_2 , and AN_3 , respectively. The circuit type of the R port is shown in table 3.

Port Mode Register B (PMRB: \$005): Port mode register B is a 4-bit write-only register which controls the D_{11}/TG_0 pin and D_{12}/TG_1 pin as shown in figure 18. The port mode register is initialized to \$0 by MCU reset. These pins are therefore initially used as ports.

Unused I/O Pins: If any unused I/O pins are left floating, the LSI may malfunction due to noise. The I/O pins should be fixed as follows to prevent malfunction.

- If without pull-down MOS (PMOS open drain) is selected for high-voltage pins, connect to V_{CC} on the printed circuit board.
- If without pull-up MOS is selected for standard pins, connect to GND on the printed circuit board.

The contents of PDR and DCR of the corresponding pin should be programmed to remain the same as in the reset state. The corresponding pin should not be used as a peripheral function I/O pin.

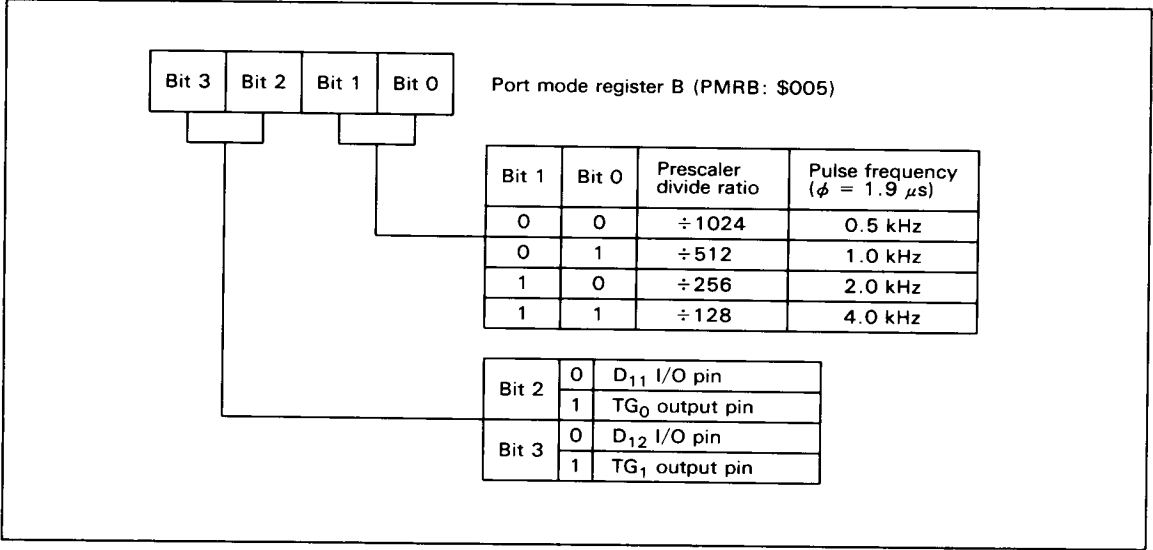


Figure 18 Port Mode Register B Functions

Table 3 I/O Pin Circuit Types

Standard pins

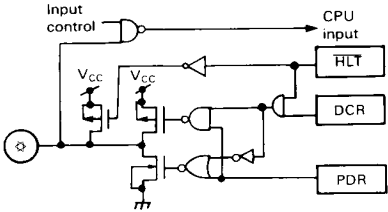
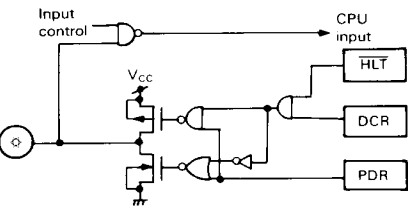
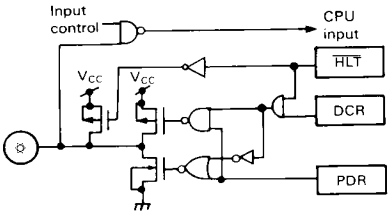
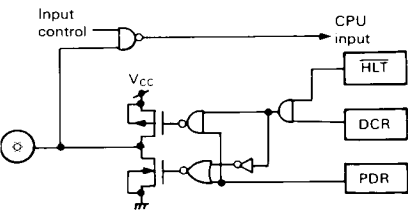
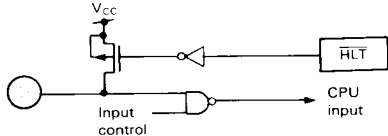
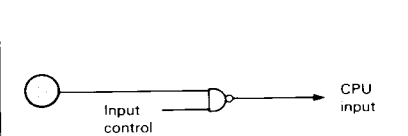
Pin Type	With Pull-Up MOS (B)	Without Pull-Up MOS (C)	Pin Name
I/O common pins			R3 ₀ -R3 ₃
	 <p>Note: Cannot be used as an analog input pin (AN₀-AN₃).</p>		R4 ₀ -R4 ₃
Input pins			$\overline{\text{INT}}_0$ $\overline{\text{INT}}_1$

Table 3 I/O Pin Circuit Types (cont)

High-voltage pins

Pin Type	Without Pull-Down MOS (D)	With Pull-Down MOS (E)	Pin Name
I/O common pins			D ₀ -D ₁₂ R ₀ -R ₃ R ₁₀ -R ₁₃ R ₂₀ -R ₂₃
Input pins			RA ₁

Note: In the stop mode, the MCU is reset, peripheral functions cannot be selected, HLT becomes 1, and I/O pins are in high impedance.

Circuit type	B	C	D	E
Product type				
Mask ROM (HD404302, HD404304)	Option			
ZTAT™ (HD4074308)		Fixed		

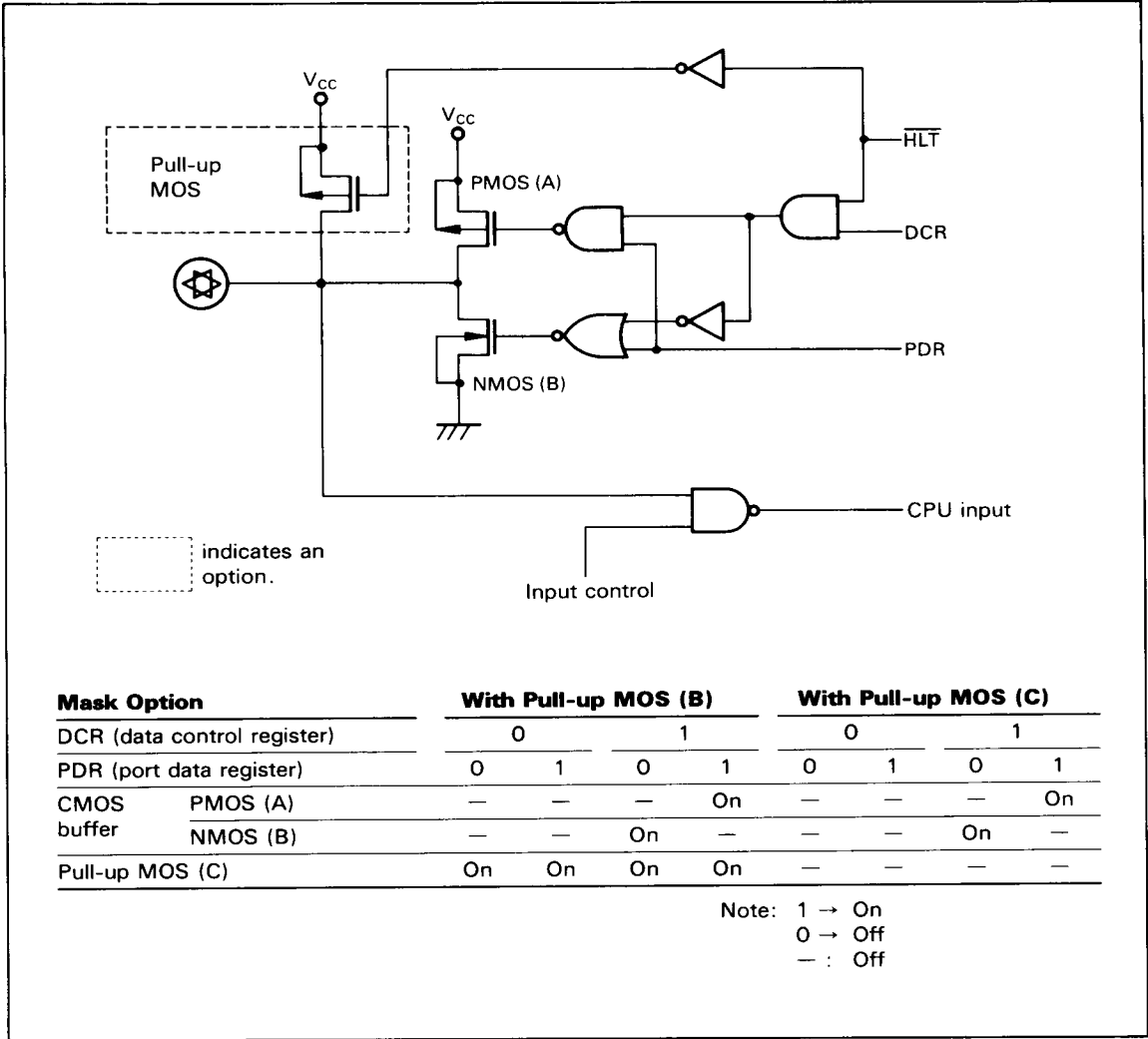


Figure 19 I/O Buffer Configuration (Standard Pins)

Reset

Setting the RESET pin high resets the MCU. At power-on or when cancelling stop mode, the reset must satisfy t_{RC} for the oscillator to stabilize. In all other cases, at least two instruction cycles are required for the MCU to be reset.

Table 4 shows the components initialized by

MCU reset and the status of each after the reset has been carried out.

Note: After reset, the standard pin port data register (PDR) is not stable. Therefore, write the data to the standard pin port data register (PDR) and set data control register (DCR) to output the data.

Table 4 Initial Values after MCU Reset

Item		Initial Value	Contents
Program counter (PC)		\$0000	Execute program from the top of ROM address
Status flag (ST)		1	Enable branching with conditional instructions
Stack pointer (SP)		\$3FF	Stack level is 0
I/O	High-voltage pin port data register (PDR)	All bits are 0	Enable to output 0
	Standard pin port data register (PDR)	—	Enable to output 1 (With pull-up MOS)
	Data control register (DCR)	All bits are 0	Output buffer is off (high impedance)
	Port mode register A (PMRA)	0000	See Port Mode Register A section
	Port mode register B (PMRB)	0000	See Port Mode Register B section
Interrupt flags/mask	Interrupt enable flag (IE)	0	Inhibit all interrupts
	Interrupt request flag (IF)	0	No interrupt request
	Interrupt mask (IM)	1	Mask interrupt request
Mode registers	Timer mode register A (TMA)	0000	See Timer Mode Register A section
	Timer mode register B (TMB)	0000	See Timer Mode Register B section
Timer/counter	Timer counter	\$00	—
	Timer counter B (TCB)	\$00	—
	Timer load register (TLR)	\$00	—
	Prescaler	\$000	See Prescaler section
A/D	A/D port select register (ADPR)	0000	See A/D Port Select Register section
	A/D mode register (AMR)	0000	See A/D Mode Register section
	A/D data register (ADR)	\$80	See A/D Data Register section
	A/D start flag (ADSF)	0	See A/D Start Flag section
Bit register	Watchdog timer on flag (WDON)	0	See Timer A section

Note: Registers and flags except above become as follows after MCU reset.

Item	Abbr	After MCU reset to recover from stop mode	After MCU reset to recover from other modes
Carry flag	(CA)	The contents of these items following MCU reset are not retained; they must be reinitialized by software	The contents of these items following MCU reset are not retained; they must be reinitialized by software
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
RAM		The contents of RAM just before MCU reset (just before a STOP instruction) are retained	

Internal Oscillator Circuit

Figure 20 is a block diagram of the internal oscillator circuit. Refer to table 5 for the

selection type. In addition, see figure 21 for the layout of the crystal or ceramic filter. In all cases, an external clock operation is available.

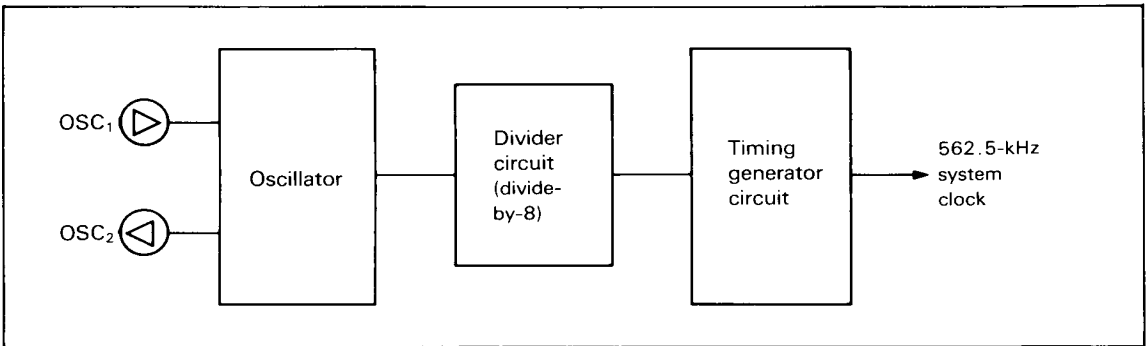


Figure 20 Internal Oscillator Circuit

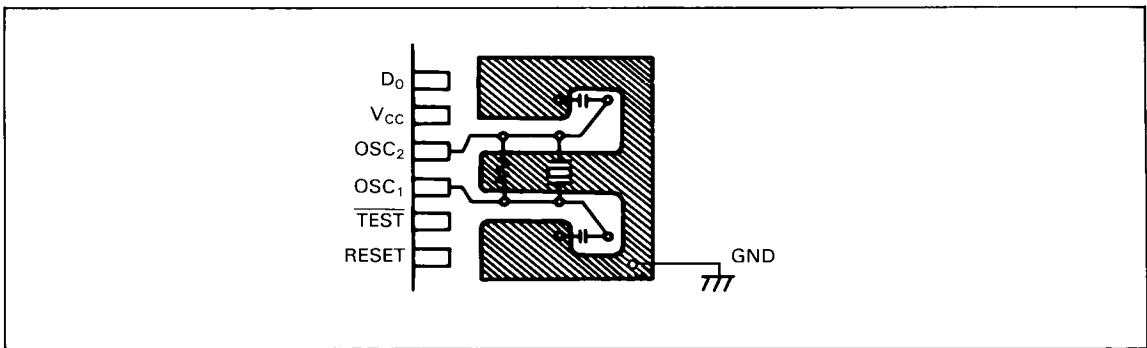
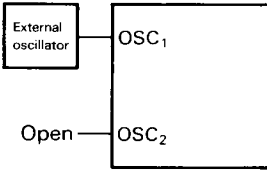
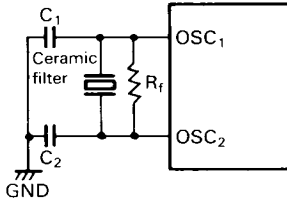
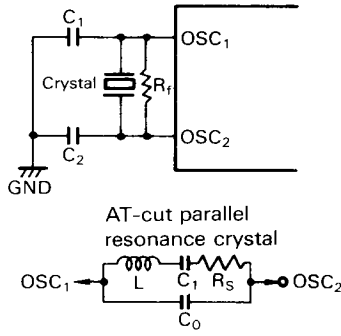


Figure 21 Layout of Crystal and Ceramic Filter

Table 5 Example of Oscillator Circuits

	Circuit configuration	Circuit constant
External clock operation		
Ceramic filter oscillator		<p>Ceramic filter: CSA 4.00 MG (Murata)</p> <p>$R_f = 1\text{ M}\Omega \pm 20\%$</p> <p>$C_1 = C_2 = 30\text{ pF} \pm 20\%$</p>
Crystal oscillator	 <p>AT-cut parallel resonance crystal</p>	<p>$R_f = 1\text{ M}\Omega \pm 20\%$</p> <p>$C_1 = 10\text{ to }22\text{ pF} \pm 20\%$</p> <p>$C_2 = 10\text{ to }22\text{ pF} \pm 20\%$</p> <hr/> <p>Crystal: Equivalent to the circuit shown at bottom left</p> <p>$C_0 = 7\text{ pF max.}$</p> <p>$R_S = 100\text{ }\Omega\text{ max.}$</p> <p>$f = 1.0\text{ to }4.5\text{ MHz}$</p>

Notes: 1. The circuit parameters written above are recommended by the crystal or ceramic filter maker. The circuit parameters are affected by the crystal, ceramic filter resonator, and the floating capacitance when designing the board. When using the resonator, consult with the crystal or ceramic filter manufacturer to determine the circuit parameters.

2. Wiring among OSC₁, OSC₂, and other elements should be as short as possible, and avoid crossing other wires. Refer to the recommended layout of the crystal and ceramic filter (figure 21).

Low-Power Dissipation Modes

The MCU has two low-power dissipation

modes, standby mode and stop mode (table 6). Figure 22 is a mode transition diagram of these modes.

Table 6 Low-Power Dissipation Modes

Condition	Standby Mode	Stop Mode
Instruction	SBY instruction	STOP instruction
Oscillator circuit	Active	Stopped
Instruction execution	Stopped	Stopped
Registers, flags	Retained	Reset ^{Note 1}
Interrupt function	Active	Stopped
RAM	Retained	Retained
Input/output pins	Retained ^{Note 2}	High impedance
Timer/counters	Active	Stopped
A/D	Active	Stopped
Cancellation method	RESET input, interrupt request	RESET input

- Notes:
1. The MCU recovers from stop mode by RESET input. Refer to table 4 for the contents of flags and registers.
 2. When I/O circuits are active, an I/O current may flow in standby mode, depending on the state of the I/O pins. This is an additional current added to the standby mode current dissipation.

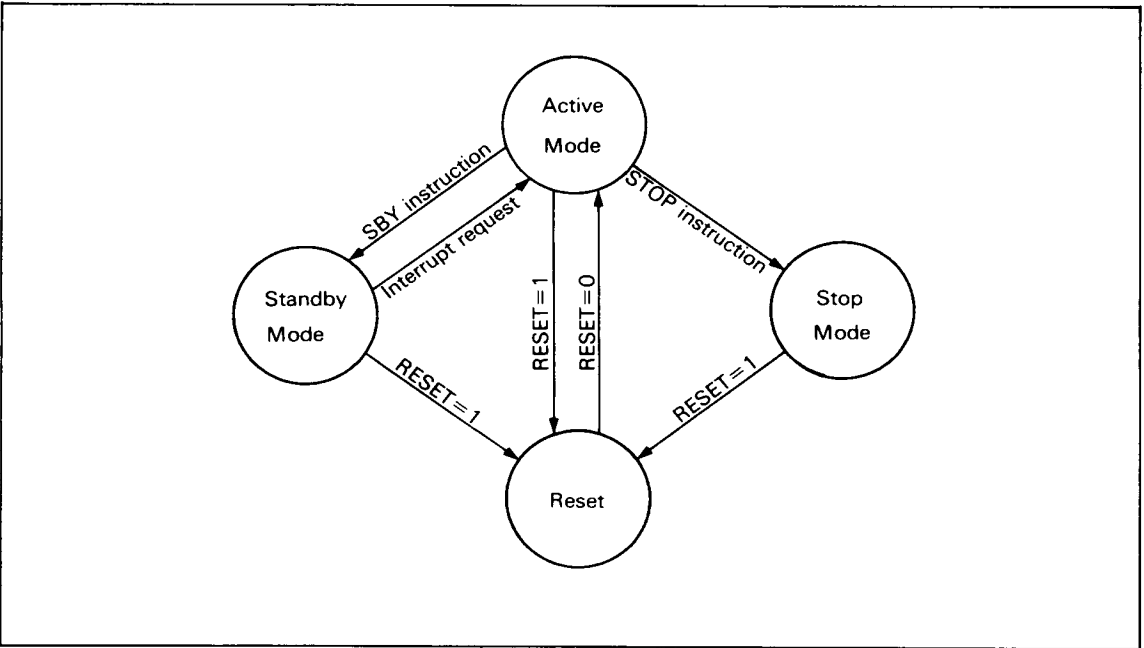


Figure 22 MCU Operation Mode Transition

Stop Mode: Executing the STOP instruction brings the MCU into stop mode, in which the oscillator circuit and every function of the MCU stop.

The stop mode may be cancelled by resetting the MCU. At this time, as shown in figure 24, reset input must be applied for at least t_{RC} for

oscillation to stabilize. (Refer to AC Characteristics table.) After the stop mode is cancelled, RAM retains the state it was in just before the MCU went into stop mode, but the accumulator, B register, W register, X/SPX registers, Y/SPY registers, carry flag, and A/D data register will not retain their contents.

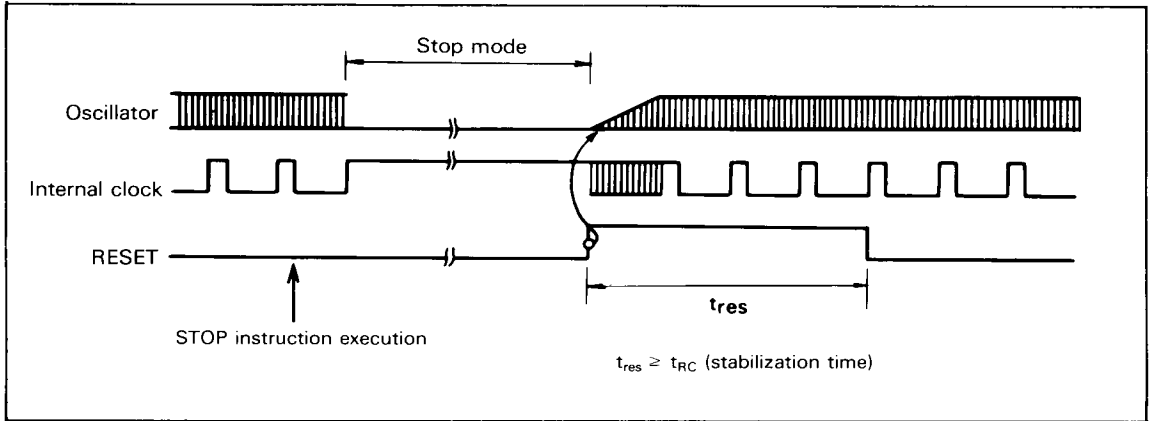


Figure 24 Timing of Stop Mode Cancellation

PROM Mode Pin Description (DP-42, DP-42S, DC-42)

MCU Mode			PROM Mode		MCU Mode			PROM Mode	
Pin No.	Pin Name	I/O	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin Name	I/O
1	D ₁₀	I/O	M ₂	I	22	AV _{CC}		V _{CC}	
2	D ₁₁ /TG ₀	I/O	V _{CC}		23	R4 ₀ /AN ₀	I/O	O ₄	I/O
3	D ₁₂ /TG ₁	I/O	V _{CC}		24	R4 ₁ /AN ₁	I/O	O ₅	I/O
4	RA ₁ /V _{disp}	I			25	R4 ₂ /AN ₂	I/O	O ₆	I/O
5	RO ₀	I/O	A ₁	I	26	R4 ₃ /AN ₃	I/O	O ₇	I/O
6	RO ₁	I/O	A ₂	I	27	AV _{SS}		GND	
7	RO ₂	I/O	A ₃	I	28	RESET	I	V _{PP} /RESET	
8	RO ₃	I/O	A ₄	I	29	TEST	I	TEST	I
9	R1 ₀	I/O	A ₅	I	30	OSC ₁	I		
10	R1 ₁	I/O	A ₆	I	31	OSC ₂	O		
11	R1 ₂	I/O	A ₇	I	32	V _{CC}		V _{CC}	
12	R1 ₃	I/O	A ₈	I	33	D ₀	I/O	M ₀	I
13	R2 ₀	I/O	A ₀	I	34	D ₁	I/O	M ₁	I
14	R2 ₁	I/O	A ₁₀	I	35	D ₂	I/O	A ₉	I
15	R2 ₂	I/O	A ₁₁	I	36	D ₃	I/O		
16	R2 ₃	I/O	A ₁₂	I	37	D ₄	I/O	A ₁₃	I
17	R3 ₀	I/O	O ₀	I/O	38	D ₅	I/O	A ₁₄	I
18	R3 ₁	I/O	O ₁	I/O	39	D ₆	I/O	CE	I
19	R3 ₂ /INT ₀	I/O	O ₂	I/O	40	D ₇	I/O	OE	I
20	R3 ₃ /INT ₁	I/O	O ₃	I/O	41	D ₈	I/O		
21	GND		GND		42	D ₉	I/O		

Note: I/O: Input/output pin; I: Input pin; O: Output pin

PROM Mode Pin Description (FP-54)

MCU Mode		PROM Mode		MCU Mode		PROM Mode	
Pin No.	Pin Name	I/O	Pin Name	I/O	Pin No.	Pin Name	I/O
1	D ₁₀	I/O	M ₂	I	28	AV _{CC}	V _{CC}
2	D ₁₁ /TG ₀	I/O	V _{CC}		29	R ₄₀ /AN ₀	I/O O ₄ I/O
3	D ₁₂ /TG ₁	I/O	V _{CC}		30	R ₄₁ /AN ₁	I/O O ₅ I/O
4	RA ₁ /V _{disp}	I			31	R ₄₂ /AN ₂	I/O O ₆ I/O
5	R0 ₀	I/O	A ₁	I	32	R ₄₃ /AN ₃	I/O O ₇ I/O
6	NC				33	NC	
7	NC				34	NC	
8	NC				35	NC	
9	R0 ₁	I/O	A ₂	I	36	AV _{SS}	GND
10	R0 ₂	I/O	A ₃	I	37	RESET	I V _{pp} /RESET
11	R0 ₃	I/O	A ₄	I	38	TEST	I TEST I
12	R1 ₀	I/O	A ₅	I	39	OSC ₁	I
13	R1 ₁	I/O	A ₆	I	40	OSC ₂	O
14	R1 ₂	I/O	A ₇	I	41	V _{CC}	V _{CC}
15	R1 ₃	I/O	A ₈	I	42	D ₀	I/O M ₀ I
16	R2 ₀	I/O	A ₉	I	43	D ₁	I/O M ₁ I
17	R2 ₁	I/O	A ₁₀	I	44	D ₂	I/O A ₉ I
18	R2 ₂	I/O	A ₁₁	I	45	D ₃	I/O
19	R2 ₃	I/O	A ₁₂	I	46	D ₄	I/O A ₁₃ I
20	NC				47	NC	
21	NC				48	NC	
22	NC				49	NC	
23	R3 ₀	I/O	O ₀	I/O	50	D ₅	I/O A ₁₄ I
24	R3 ₁	I/O	O ₁	I/O	51	D ₆	I/O CE I
25	R3 ₂ /INT ₀	I/O	O ₂	I/O	52	D ₇	I/O OE I
26	R3 ₃ /INT ₁	I/O	O ₃	I/O	53	D ₈	I/O
27	GND		GND		54	D ₉	I/O

Note: I/O: Input/output pin; I: Input pin; O: Output pin; NC: No connection

PROM Mode Pin Functions (HD4074308)

V_{PP}: Apply the programming voltage (12.5 V \pm 0.3 V) to this pin.

$\overline{\text{CE}}$: Inputs the control signal to enable PROM programming and verification.

$\overline{\text{OE}}$: Inputs the data output control signal for verification.

A₀-A₁₄: Address input pins of the internal PROM.

O₀-O₇: Data bus input/output pins of the internal PROM.

M₀, M₁, M₂: Used to set the PROM mode. The MCU is set to the PROM mode by pulling AV_{SS} and $\overline{\text{TEST}}$ low, and RESET, M₀, M₁, M₂, and AV_{CC} high.

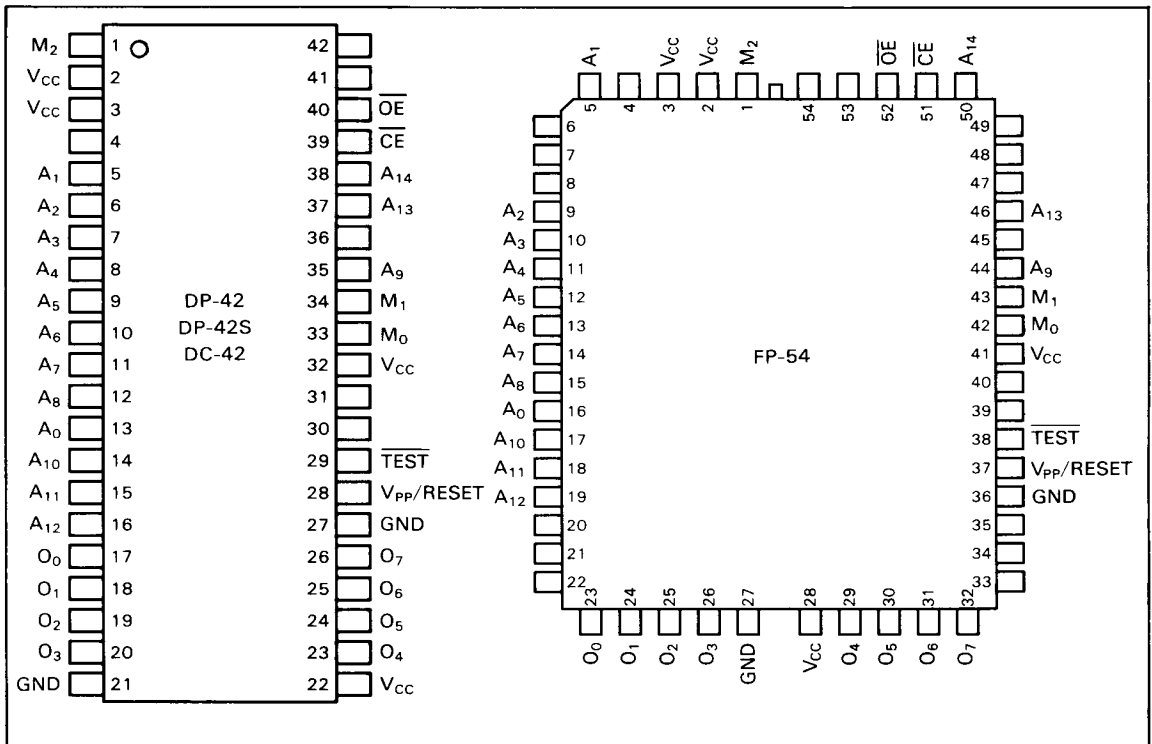


Figure 25 Pin Arrangement in PROM Mode

Programmable ROM (HD4074308)

The MCU on-chip PROM is programmed in PROM mode (figures 26 and 27). PROM mode is set by pulling TEST low, and RESET, M₀, M₁, and M₂ high, as shown in figure 26. In PROM mode, the MCU does not operate. Table 7 shows the PROM mode selection. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a 42-to-28-pin socket adapter. Table 8 lists recommended PROM programmers and socket adapters.

Since an instruction of the HMCS400 series consists of 10 bits, the HMCS400 series MCU incorporates a conversion circuit to enable the use of a general-purpose PROM programmer. By this circuit, an instruction is read or programmed using 2 addresses, generated as the lower 5 bits and upper 5 bits, as shown in figure 27. For example, if 8 Kwords of on-chip PROM are programmed by a general-purpose PROM programmer, 16 Kbytes of addresses (\$0000-\$3FFF) should be specified.

Programming and Verification

The MCU can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 7 shows how programming and verification modes are selected. Figure 28 is a programming flowchart.

Erasing

PROMs with ceramic window packages can be erased by ultraviolet light. All erased bits are set to 1.

Erasing conditions are: ultraviolet (UV) light with a wavelength of 2537 Å with a minimum irradiation of 15 W·sec/cm². These conditions are satisfied by exposing the LSI to a 12,000-μW/cm² UV source for 15 to 20 minutes at a distance of 1 inch.

Table 7 PROM Mode Selection

Mode	Pin			
	CE	OE	V _{PP}	O ₀ -O ₇
Programming	Low	High	V _{PP}	Data input
Verification	High	Low	V _{PP}	Data output
Programming inhibited	High	High	V _{PP}	High impedance

Table 8 PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Maker	Type Name	Maker	Package	Type Name
DATA I/O	22B	Hitachi	DP-42	HS430ESD01H
	29B		DP-42S	HS430ESS01H
			FP-54*	HS430ESF01H*
AVAL Corp.	PKW-1100	Hitachi	DP-42	HS430ESD01H
	PKW-1000		DP-42S	HS430ESS01H
			FP-54*	HS430ESF01H*

Note: An automatic programming mode of the PROM programmer is not available, therefore if a silicon signature check is performed, the A9 port will be permanently damaged. The A9 port is a high-voltage I/O port of the MCU. It will be damaged if an overvoltage (12.5 V) exceeding the voltage resistance of the MCU buffer is applied.

When a connection check is made using a protection diode between the MCU and its socket, an open error occurs on an address port. Since the direction of the protection diode of the MCU high-voltage pin is reversed, the address port is regarded as open.

* Under development

Precautions

1. Addresses \$0000 to \$3FFF must be specified if the PROM is programmed by a PROM programmer. If addresses of \$4000 or higher are accessed, the PROM may not be programmed or verified. Note that the plastic type packages cannot be erased and reprogrammed. (Ceramic window packages can be erased and reprogrammed by ultraviolet light.) Data in unused addresses must be set to \$FF.
2. Be sure that the PROM programmer,

socket adapter, and LSI are inserted correctly (pin 1 positions match). Using the wrong programmer or socket adapter may cause an overvoltage and damage the LSI (table 8). Make sure that the LSI is firmly fixed in the socket adapter, and that the socket adapter is firmly fixed onto the programmer.

3. The PROM should be programmed with $V_{PP}=12.5\text{ V}$. Other PROMs use 21 V. If 21 V is applied to the MCU, the LSI may be permanently damaged. 12.5 V is Intel's 27256 V_{PP} .

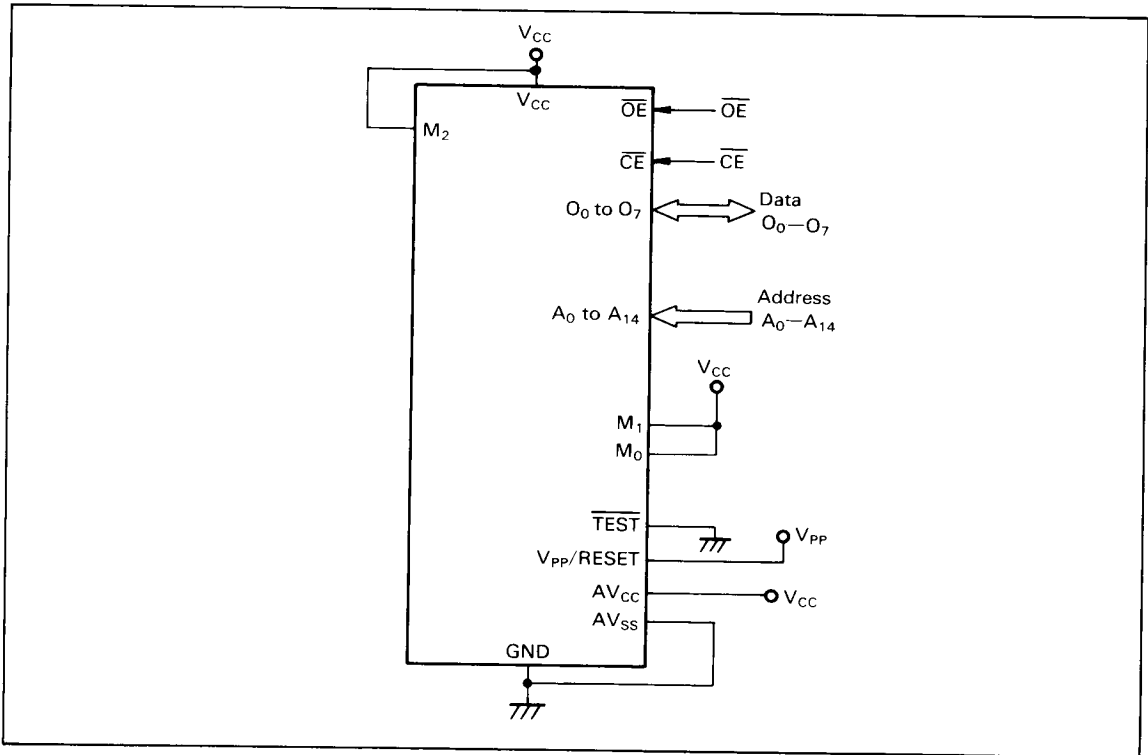


Figure 26 Connections for PROM Mode

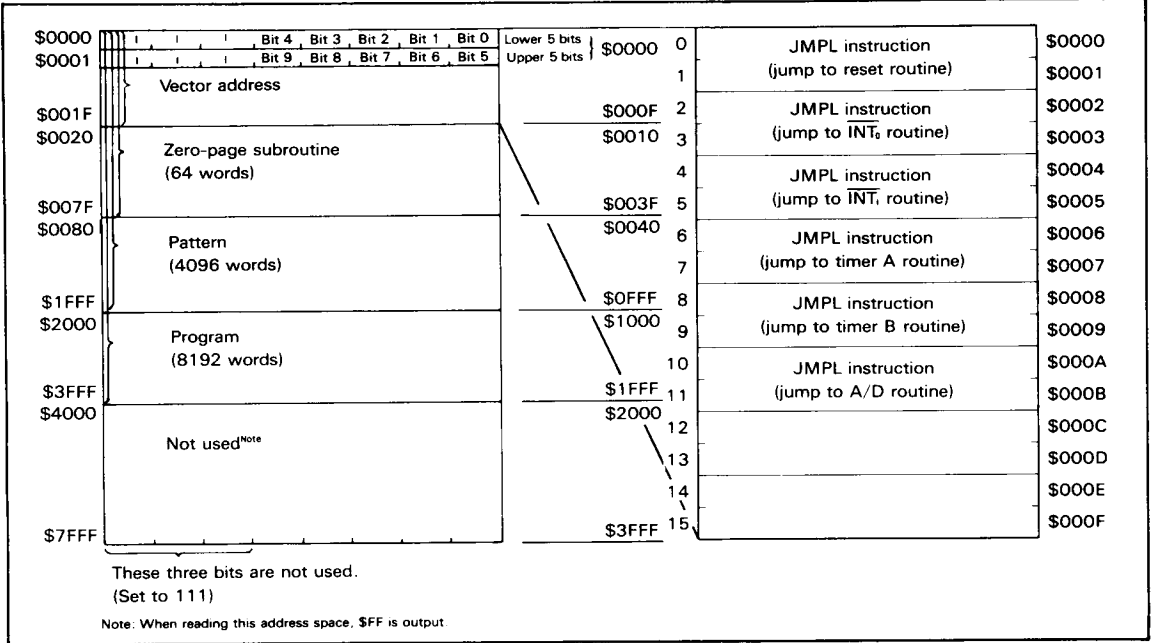


Figure 27 PROM Mode Memory Map

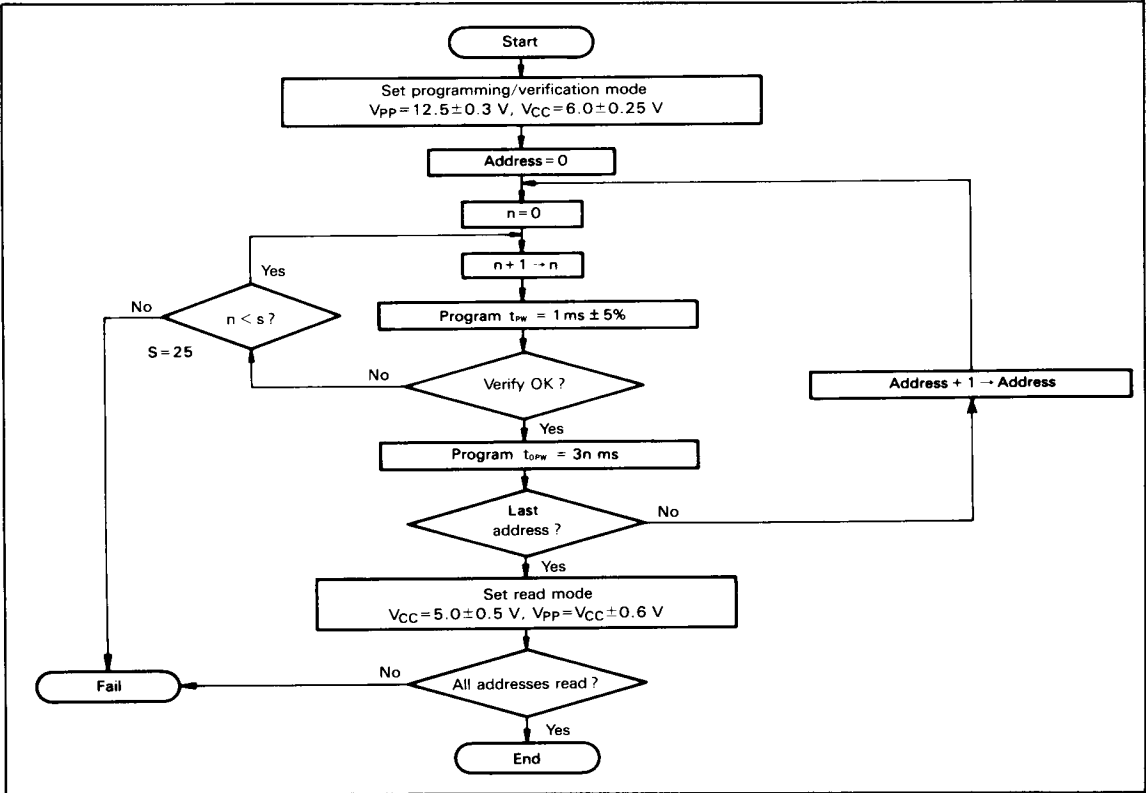


Figure 28 High-Speed Programming Flowchart

ZTAT™ MCU On-Chip PROM Characteristics and Precautions

Principles of Programming/Erasing: The ZTAT™ memory cells are the same as an EPROM's. They are programmed by applying a high voltage between the control gate and drain to inject hot electrons into the floating gate. These electrons then become stable, surrounded by an energy barrier of SiO_2 film. Such a cell becomes a 0 bit due to the memory threshold voltage change. A cell with no condensed electrons in its floating gate appears as a 1 bit (figure 29).

The electron charge in memory cells may

decrease as time goes by. This can be caused by:

- Ultraviolet light: Discharged by photo-emitted electrons according to the erasure principle
- Heat: Discharged by thermal emitted electrons
- High voltage: Discharged by a high electric field at the control gate or drain

If the oxide film covering a floating gate is defective, the erasure rate is greatly increased. Normally, electron erasure does not occur, since such defective devices are found and removed during screening tests.

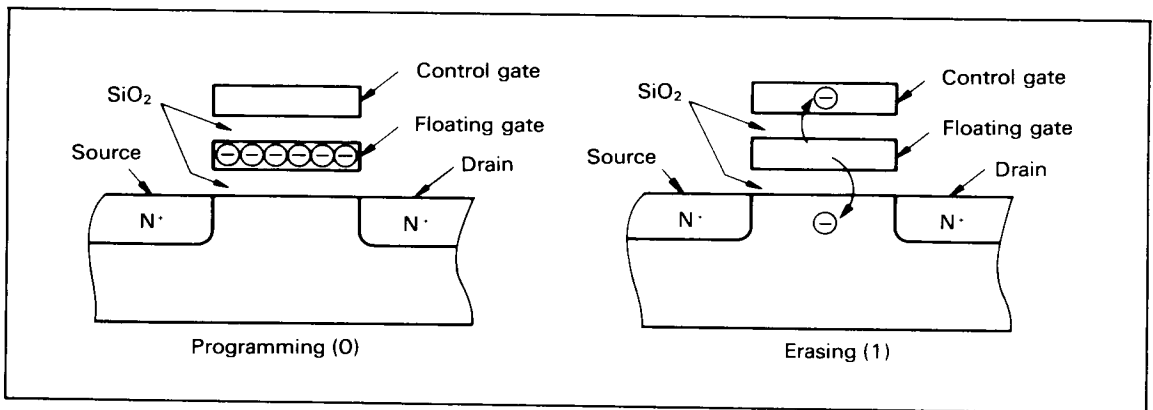


Figure 29 Cross-Sections of a EPROM Memory Cell

Programming Precautions: The PROM memory cells should be programmed under specific voltage and timing conditions. The higher the program voltage and the longer the program pulse is applied, the more electrons will be injected into the floating gate. However, if an overvoltage is applied to V_{PP} , the pn junction may be permanently damaged. Pay particular attention to PROM programmer overshoot. Negative voltage noise will cause a parasitic transistor effect, which may reduce breakdown voltage.

The ZTATTM microcomputer is connected electrically to the PROM programmer through a socket adapter. Therefore, pay careful attention to the following:

- Ensure that the socket adapter is firmly fixed onto the PROM programmer.

- Do not touch the socket adapter or the LSI during programming.

- Misprogramming can be caused by poor contacts.

On-Chip PROM Reliability after Programming: Generally, semiconductors are reliable except for initial failures which can be screened during testing. Exposure to high temperature is a kind of screening test which quickly removes PROM memory cells with data hold failures. This is done to ZTATTM microcomputers in the wafer stage, so ZTATTM data hold characteristics are very reliable. Exposing the LSI to 150°C after being programmed can effectively upgrade these characteristics. Figure 30 shows the recommended screening flow.

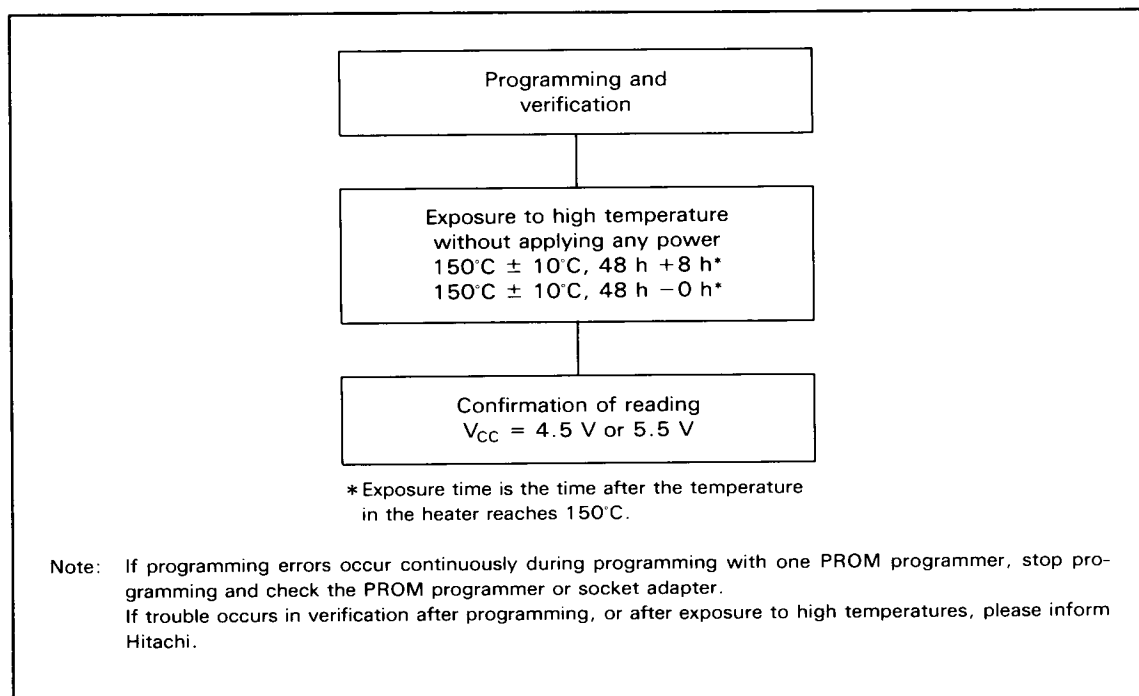


Figure 30 Recommended Screening Flow

Window-Type Package Precautions

Glass Erasure Window: If the glass window comes in contact with plastic or anything with a static charge, the LSI may malfunction due to the electrostatic charge on the surface of the window. If this occurs, exposing the LSI to ultraviolet light for a few minutes neutralizes the charge, and restores the LSI to normal operation. However, charge stored in the floating gates decreases at the same time, so reprogramming is recommended.

Electrostatic charge buildup on the window is a fundamental cause of malfunctions. Measures for its prevention are the same as those for preventing electrostatic breakdown:

1. Operators should be grounded when handling equipment.
2. Do not rub the glass window with plastics.
3. Be careful of coolant sprays which may contain ions.
4. The ultraviolet shading label (which includes conductive material) effectively neutralizes charge.

Ultraviolet Shading Label: If the LSI is exposed to fluorescent light or sunlight, its memory contents may be erased by the small quantity of ultraviolet light in these sources.

In strong light, the MCU may fail under the influence of photocurrent. To prevent this problem, it is recommended that the device be used with an ultraviolet shading label covering the erasure window after programming.

Special labels contain metal particles to absorb the ultraviolet light. When choosing a label, note the following:

1. Adhesion: Reuse and dust reduce adhesion. Peeling off a label may cause static electricity, therefore, erasing and rewriting is recommended after peeling off a label. Sticking a new label over the old one is preferable to replacing a label.
2. Allowable temperature range: The allowable environmental temperature range of the label should be noted. If it is used under conditions outside this range, the paste may harden or adhere to the window, causing the paste to remain on the window when the label is removed.
3. Moisture resistance: The allowable moisture range and environmental conditions of the label should be noted. It is difficult to find an appropriate label for all conditions. The proper label should be selected depending on the intended use of the MCU.

Addressing Modes

RAM Addressing Modes

As shown in figure 31, the MCU has three RAM addressing modes: register indirect addressing, direct addressing, and memory register addressing.

Register Indirect Addressing Mode: The W register, X register, and Y register contents (10 bits) are used as the RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words, with the word (10 bits) following the opcode used as the RAM address.

Memory Register Addressing Mode: The memory registers (16 digits from \$040 to \$04F) are accessed by executing the LAMR and XMRA instructions.

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes as shown in figure 32.

Direct Addressing Mode: The program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction. These instructions replace the 14 program counter bits (PC_{13} to PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 8 pages of ROM with 256 words per page. By executing the BR instruction, the program can branch to an address in the current page. This instruction replaces the low-order 8 bits of the program counter (PC_7 to PC_0) with 8-bit immediate data.

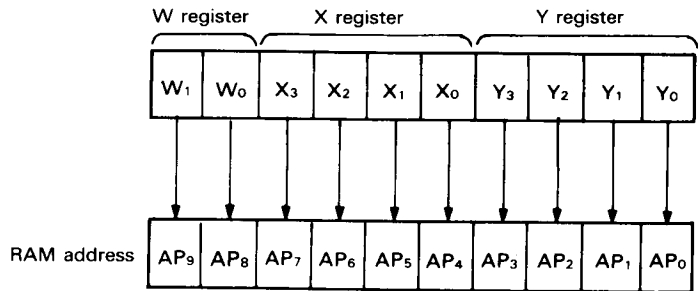
When the BR instruction is on a page boundary ($256n + 255$) (figure 33), executing it transfers the PC contents to the next page according to the hardware architecture. Consequently, the program branches to the next page when the BR instruction is used on a page boundary. The HMCS400-series cross macroassembler has an automatic paging facility for ROM pages.

Zero-Page Addressing Mode: By executing the CAL instruction, the program can branch to the zero-page subroutine area, which is located at \$0000-\$003F. When the CAL instruction is executed, 6 bits of immediate data are placed in the low-order six bits of the program counter (PC_5 to PC_0) and 0s are placed in the high-order eight bits (PC_{13} to PC_6).

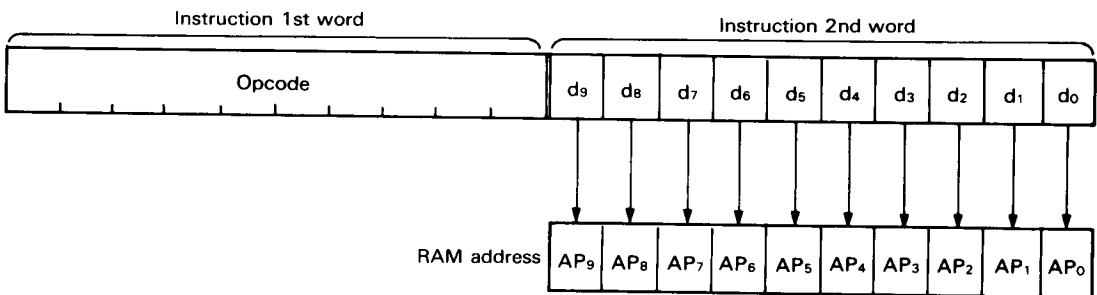
Table Data Addressing Mode: By executing the TBR instruction, the program can branch to the address determined by the contents of the 4-bit immediate data, accumulator, and B register.

P Instruction: ROM data addressed by table data addressing can be referenced by the P instruction (figure 34). When bit 8 in the referred ROM data is 1, 8 bits of ROM data are written into the accumulator and B register. When bit 9 is 1, 8 bits of ROM data are written into the R1 and R2 port output registers. When both bits 8 and 9 are 1, ROM data are written into the accumulator and B register, and also to the R1 and R2 port output registers at the same time.

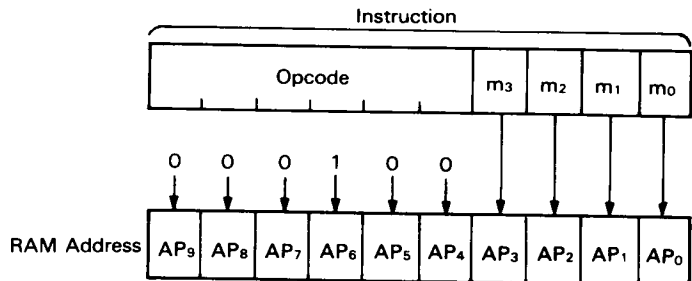
The P instruction has no effect on the program counter.



Register Indirect Addressing



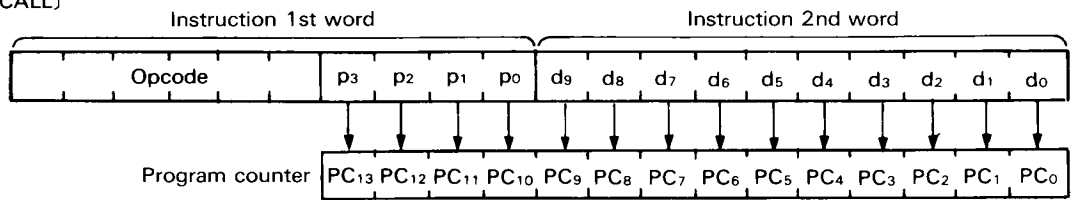
Direct Addressing



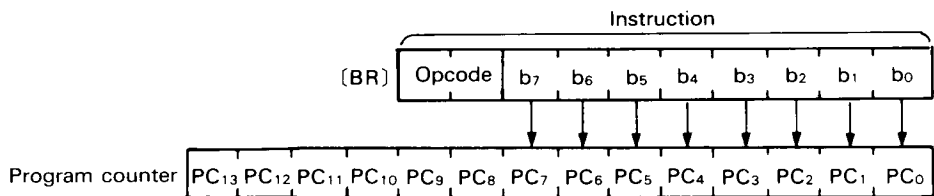
Memory Register Addressing

Figure 31 RAM Addressing Modes

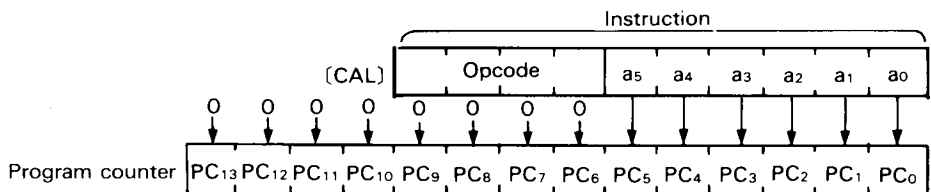
[JMPL]
[BRL]
[CALL]



Direct Addressing



Current Page Addressing



Zero Page Addressing

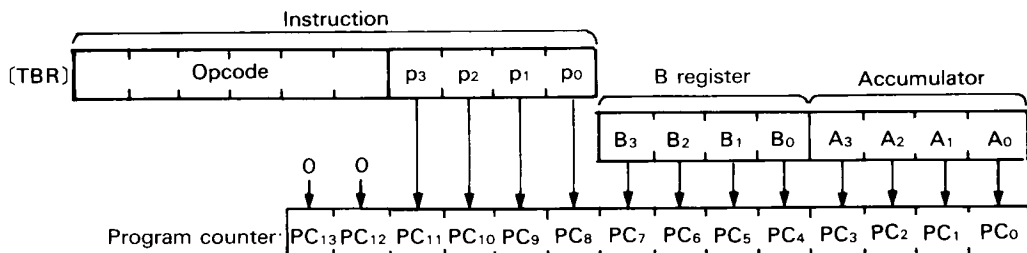


Table Data Addressing

Figure 32 ROM Addressing Modes

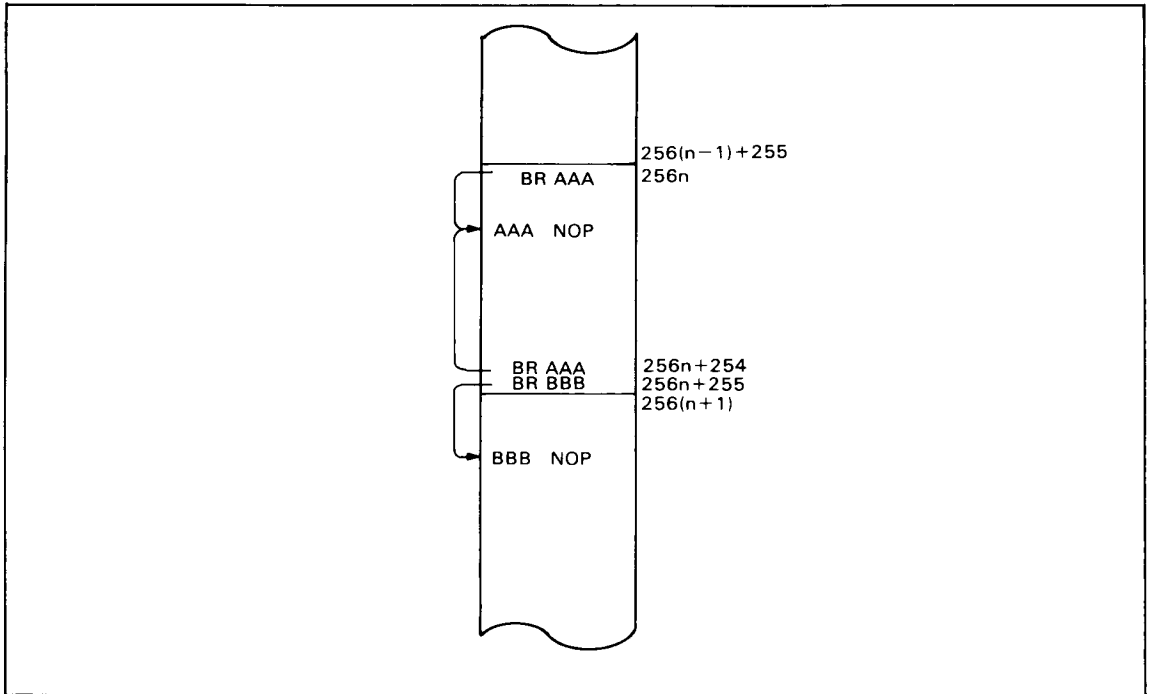


Figure 33 BR Instruction Branch Destination on a Page Boundary

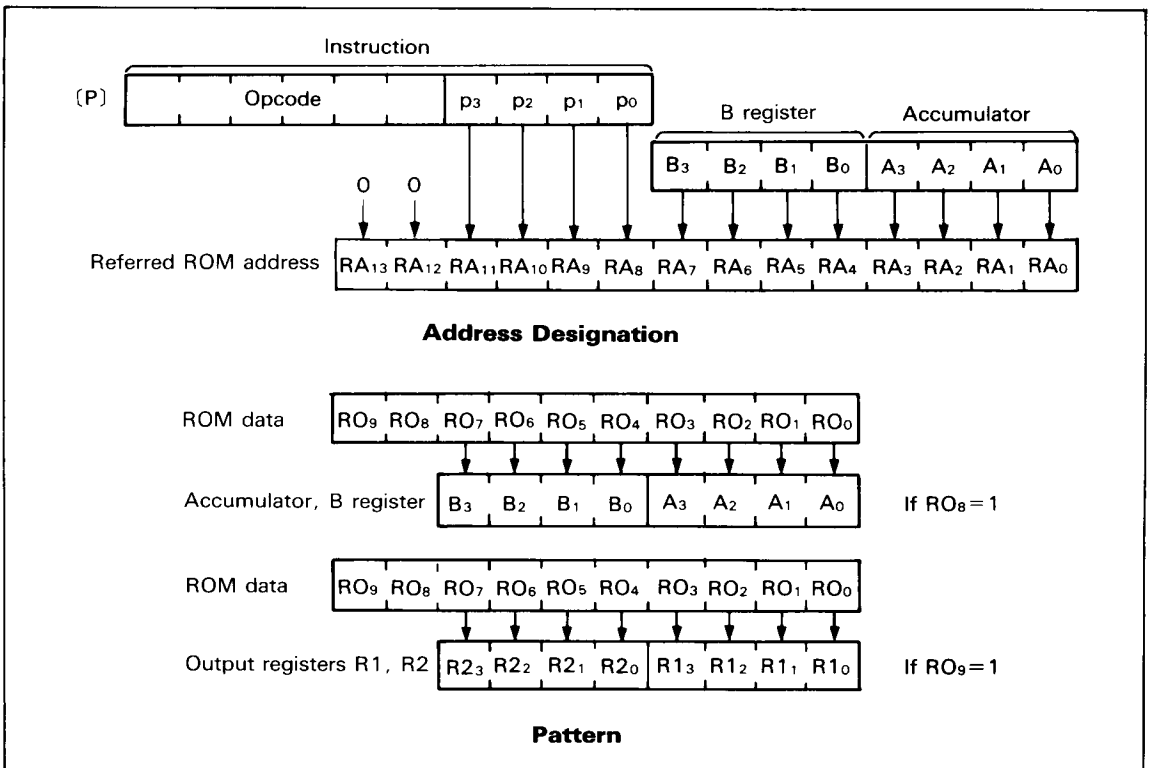


Figure 34 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	-0.3 to +7.0	V	1, 12
Program voltage	V_{PP}	-0.3 to +14.0	V	2, 13
Pin voltage	V_T	-0.3 to $V_{CC} + 0.3$	V	3
		$V_{CC} - 45$ to $V_{CC} + 0.3$	V	4
Total permissible input current	ΣI_o	50	mA	5
Maximum input current	I_o	15	mA	7, 8
Maximum output current	$-I_o$	4	mA	8, 9
		6	mA	9, 10
		30	mA	9, 11
Total permissible output current	$-\Sigma I_o$	150	mA	6
Operation temperature	T_{opr}	-20 to +75	°C	
Storage temperature	T_{str}	-55 to +125	°C	
Storage temperature (bias)	T_{bias}	-25 to +80	°C	13

- Notes:
1. Normal operation should be performed under the conditions specified by the electrical characteristics. Exceeding these conditions can result in malfunction, degraded performance, and permanent damage to the LSI.
 2. Applies to the RESET pin (V_{PP}). (HD4074308)
 3. Applies to pins other than high-voltage pins.
 4. Applies to high-voltage pins.
 5. Total permissible input current is the sum of input currents which flow in from all I/O pins to GND simultaneously.
 6. Total permissible output current is the sum of output currents which flow from V_{CC} to all I/O pins simultaneously.
 7. Maximum input current is the amount of input current allowed from each I/O pin to GND.
 8. Applies to R3 and R4.
 9. Maximum output current is the amount of output current allowed from V_{CC} to each I/O pin.
 10. Applies to R0 to R2.
 11. Applies to D₀ to D₁₂.
 12. Voltage is based on GND.
 13. Applies to the HD4074308.

Electrical Characteristics

DC Characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V}$ to V_{CC} , $T_a = -20^\circ$ to $+75^\circ\text{C}$ unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	RESET, $\overline{INT_0}$, INT_1	$0.8V_{CC}$		$V_{CC} + 0.3$	V		
		OSC ₁	$V_{CC} - 0.5$		$V_{CC} + 0.3$	V		
Input low voltage	V_{IL}	RESET, $\overline{INT_0}$, INT_1	-0.3		$0.2V_{CC}$	V		
		OSC ₁	-0.3		0.5	V		
Input/output leakage current	$ I_{IL} $	RESET, $\overline{INT_0}$, INT_1 , OSC ₁			1	μA	$V_{in} = 0\text{ V}$ to V_{CC}	1
Current dissipation in active mode	I_{CC}	V_{CC}			3.0	mA	$V_{CC} = 5\text{ V}$; $f_{OSC} = 4\text{ MHz}$	2,5
Current dissipation in standby mode	I_{SBY}	V_{CC}			1.5	mA	$V_{CC} = 5\text{ V}$; $f_{OSC} = 4\text{ MHz}$	3,5
Current dissipation in stop mode	I_{STOP}	V_{CC}			10	μA	$V_{in}(\overline{TEST}) = V_{CC}$ $V_{in}(\text{RESET}) = GND$	4
Stop mode retaining voltage	V_{STOP}	V_{CC}	2			V		

- Notes:
- Excluding pull-up MOS current and output buffer current.
 - The MCU is in the reset state. Input/output current does not flow.
 - MCU in reset state, operation mode
 - RESET, \overline{TEST} : V_{CC}
 - R3, R4: V_{CC}
 - D₀-D₁₂, RO-R2, RA₁: V_{disp}
 - The timer/counter operates with the fastest clock. Input/output current does not flow.
 - MCU in standby mode
 - Input/output in reset state
 - RESET: GND
 - \overline{TEST} : V_{CC}
 - R3, R4: V_{CC}
 - D₀-D₁₂, RO-R2, RA₁: V_{disp}
 - Excluding pull-down MOS current.
 - When $f_{OSC} = x$ (MHz) estimate the current dissipation as follows:
 Max. value $f_{OSC} = x$ (MHz) = $x/4 \times$ (max. value $f_{OSC} = 4\text{ MHz}$)

HD404302/HD404304/HD4074308

Input/Output Characteristics for Standard Pins ($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V}$ to V_{CC} , $T_a = -20^\circ$ to $+75^\circ\text{C}$ unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	R3, R4	$0.7V_{CC}$		$V_{CC} + 0.3$	V		
Input low voltage	V_{IL}	R3, R4	-0.3		$0.2V_{CC}$	V		
Output high voltage	V_{OH}	R3, R4	$V_{CC} - 1.0$			V	$-I_{OH} = 1.0\text{ mA}$	1
		R3, R4	$V_{CC} - 0.5$			V	$-I_{OH} = 0.5\text{ mA}$	1
Output low voltage	V_{OL}	R3, R4			0.4	V	$I_{OL} = 1.6\text{ mA}$	
Input/output leakage current	$ I_{IL} $	R3, R4			1	μA	$V_{in} = 0\text{ V}$ to V_{CC}	2
Pull-up MOS current	$-I_p$	R3, R4	30	70	150	μA	$V_{CC} = 5\text{ V}$, $V_{in} = 0\text{ V}$	3

- Notes:
1. Applied to I/O pins selected as CMOS output by mask option.
 2. Pull-up MOS current and output buffer current are excluded.
 3. Applied to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High Voltage Pins ($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V}$ to V_{CC} , $T_a = -20^\circ$ to $+75^\circ\text{C}$ unless otherwise specified)

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0 - D_{12} , R_1 , R_2 , RA_1 , RO	$0.7V_{CC}$		$V_{CC} + 0.3$	V		
Input low voltage	V_{IL}	D_0 - D_{12} , R_1 , R_2 , RA_1 , RO	$V_{CC} - 40$		$0.2V_{CC}$	V		
Output high voltage	V_{OH}	D_0 - D_{12} , TG_0 , TG_1	$V_{CC} - 3.0$			V	$-I_{OH} = 15\text{ mA}$	
			$V_{CC} - 2.0$			V	$-I_{OH} = 10\text{ mA}$	
			$V_{CC} - 1.0$			V	$-I_{OH} = 4\text{ mA}$	
		RO - R_2	$V_{CC} - 3.0$			V	$-I_{OH} = 3\text{ mA}$,	
			$V_{CC} - 2.0$			V	$-I_{OH} = 2\text{ mA}$	
			$V_{CC} - 1.0$			V	$-I_{OH} = 0.8\text{ mA}$	
Output low voltage	V_{OL}	D_0 - D_{12} , RO - R_2			$V_{CC} - 37$	V	$V_{disp} = V_{CC} - 40\text{ V}$	1
		D_0 - D_{12} , RO - R_2			$V_{CC} - 37$	V	$150\text{ k}\Omega$ at $V_{CC} - 40\text{ V}$	2
Input/output leakage current	$ I_{IL} $	D_0 - D_{12} , RO - R_2 , RA_1			20	μA	$V_{in} = V_{CC} - 40\text{ V}$ to V_{CC}	3
Pull-down MOS current	I_d	D_0 - D_{12} , RO - R_2	100	300	700	μA	$V_{disp} = V_{CC} - 35\text{ V}$,	1, 4
			200	400	800		$V_{in} = V_{CC}$	1, 5

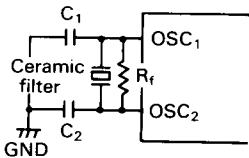
- Notes:
1. Applied to I/O pins selected as with pull-up MOS by mask option.
 2. Applied to I/O pins selected as without pull-up MOS (PMOS open drain) by mask option.
 3. Pull-up MOS current and output buffer current are excluded.
 4. Applied to HD404302.
 5. Applied to HD404304.

AC Characteristics

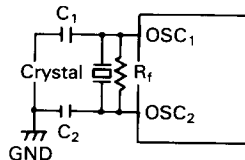
($V_{CC} = 5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, $V_{disp} = V_{CC} - 40\text{ V}$ to V_{CC} , $T_a = -20^\circ$ to $+75^\circ\text{C}$, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Oscillation frequency (divide-by-8)	f_{OSC}	OSC ₁ , OSC ₂	0.4	4	4.5	MHz		
Instruction cycle time	t_{cyc}		1.78	2	20	μs		
Oscillation stabilization time	t_{RC}	OSC ₁ , OSC ₂			20	ms	(Ceramic filter)	1
					40	ms	(Crystal)	
External clock frequency	f_{CP}	OSC ₁	0.4		4.5	MHz		
External clock high and low widths	t_{CPH} , t_{CPL}	OSC ₁	92			ns	Divide-by-8	2
	t_{CPr} , t_{CPf}							
External clock rising and falling times	t_{CPr} , t_{CPf}	OSC ₁			20	ns		2
INT ₀ high and low widths	t_{I0H} , t_{I0L}	INT ₀	2			t_{cyc}		3
INT ₁ high and low widths	t_{I1H} , t_{I1L}	INT ₁	2			t_{cyc}		3
RESET high width	t_{RSTH}	RESET	2			t_{cyc}		4
Input capacitance	HD404302	All pins (except RESET)		15		pF	$f=1\text{ MHz}$, $V_{in}=0\text{ V}$	
	C_{in}	RESET		20		pF	$f=1\text{ MHz}$, $V_{in}=0\text{ V}$	
	HD404304	All pins (except RESET)		30		pF	—	
	C_{in}	RESET		30		pF	—	
	HD4074308	All pins (except RESET)		20		pF	$f=1\text{ MHz}$, $V_{in}=0\text{ V}$	
	C_{in}	RESET		250		pF	$f=1\text{ MHz}$, $V_{in}=0\text{ V}$	
RESET falling time	t_{RSTf}	RESET		20		ms		4

Notes: 1. The oscillation stabilization time is the period from when V_{CC} reaches 4.5 V at power-on until when the oscillator stabilizes, or after RESET goes to high to quit the stop mode. At power-on or when cancelling the stop mode, RESET must remain high for at least t_{RC} . Since t_{RC} depends on the crystal or ceramic filter's circuit constant and stray capacitance, it is recommended that the user follow the crystal or ceramic filter manufacturer's recommendations when designing the reset circuit. Applies to the HD404302, HD4074308, and HD404304.



Crystal: HC-491U
(4.194304MHz : Kinseki)
 $R_f = 1\text{ M}\Omega \pm 20\%$
 $C_1 = C_2 = 20\text{ pF} \pm 20\%$



Ceramic filter: CSA 4.00 MG
(Murata)
 $R_f = 1\text{ M}\Omega \pm 20\%$
 $C_1 = C_2 = 30\text{ pF} \pm 20\%$

2. See figure 35.
3. See figure 36.
4. See figure 37.

**A/D Converter Characteristics ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = \text{GND}$,
 $T_a = 0^\circ \text{ to } +70^\circ \text{C}$)**

Item	Symbol	Pin	Min	Typ	Max	Unit	Test Condition	Note
Analog power supply voltage	AV_{CC}	AV_{CC}	$V_{CC} - 0.3$	V_{CC}	$V_{CC} + 0.3$	V		
Analog input voltage	AV_{in}	AN_0 - AN_3	AV_{SS}	—	AV_{CC}	V		
Current between AV_{CC} and AV_{SS}	I_{ad}		—	0.08	—	mA		
Analog input capacity	C_{ain}	AN_0 - AN_3	—	15	—	pF		
Resolution	—	—	—	8	—	Bit		
Conversion time	—	—	61	—	536	μs		1
Number of inputs	—	—	0	—	4	Channel		
Absolute accuracy	—	—	—	—	± 2	LSB	$T_a = 25^\circ \text{C}$, $V_{CC} = 5.0 \text{ V}$	1, 2
Input impedance	—	AN_0 - AN_3	1 M	—	—	Ω		

- Notes: 1. The operating frequency f_{OSC} of the A/D conversion is from 1 MHz to 4.5 MHz.
2. When using the R4/AN port as an analog input, the I/O option of the R4 port must be set as without pull-up MOS.

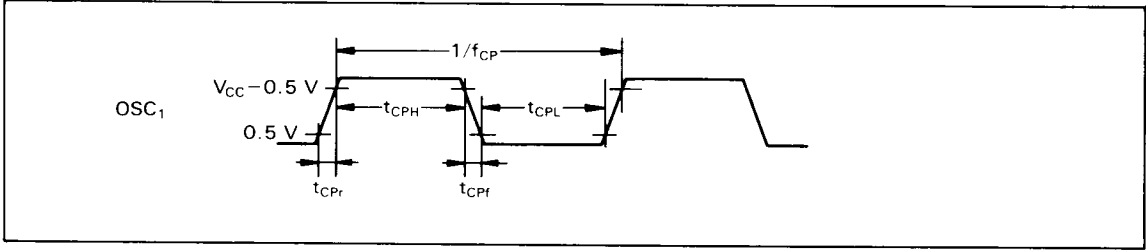


Figure 35 Oscillator Timing

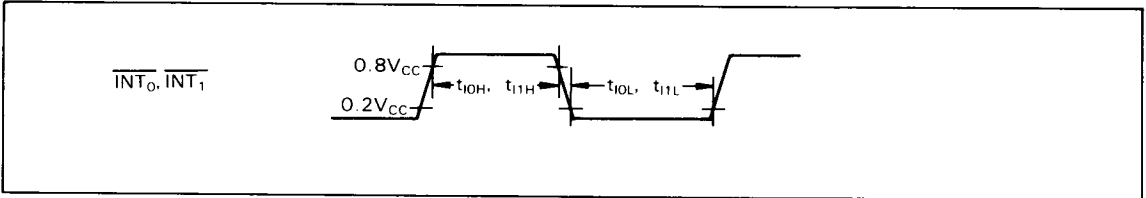


Figure 36 Interrupt Timing

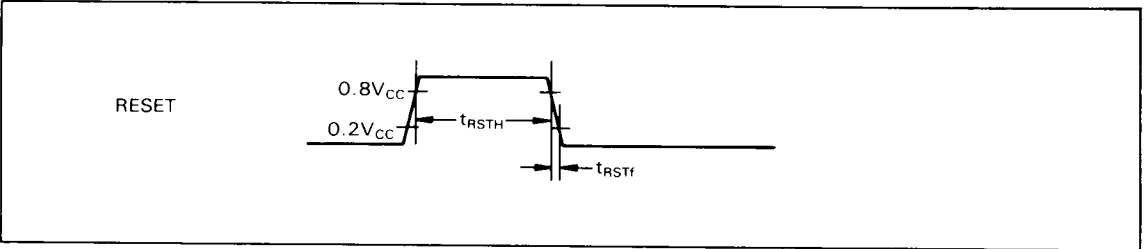


Figure 37 Reset Timing

Electrical Characteristics for HD4074308

DC Characteristics

($V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition
Input high voltage	V_{IH}	O_0-O_7 , A_0-A_{14} , \overline{OE} , \overline{CE}	2.2		$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	O_0-O_7 , A_0-A_{14} , \overline{OE} , \overline{CE}	-0.3		0.8	V	
Output high voltage	V_{OH}	O_0-O_7	2.4			V	$I_{OH} = -200\text{ }\mu\text{A}$
Output low voltage	V_{OL}	O_0-O_7			0.4	V	$I_{OL} = 1.6\text{ mA}$
Input leakage current	$ I_{IL} $	O_0-O_7 , A_0-A_{14} , \overline{OE} , \overline{CE}			2	μA	$V_{in} = 5.25\text{ V}/0.5\text{ V}$
V_{CC} current	I_{CC}				30	mA	
V_{PP} current	I_{PP}				40	mA	

AC Characteristics

($V_{CC} = 6\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Address setup time	t_{AS}	2			μs	Figure 38
\overline{OE} setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	0			μs	
Data hold time	t_{DH}	2			μs	
Output disable delay time	t_{DF}			130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
\overline{CE} pulse width when overprogramming	t_{OPW}	2.85		78.75	ms	
V_{CC} setup time	t_{VCS}	2			μs	
Data output delay time	t_{OE}	0		500	ns	

Note : Input pulse level: 0.8 to 2.2 V
 Input rise/fall time $\leq 20\text{ ns}$
 Input timing reference levels: 1.0 V, 2.0 V
 Output timing reference levels: 0.8 V, 2.0 V

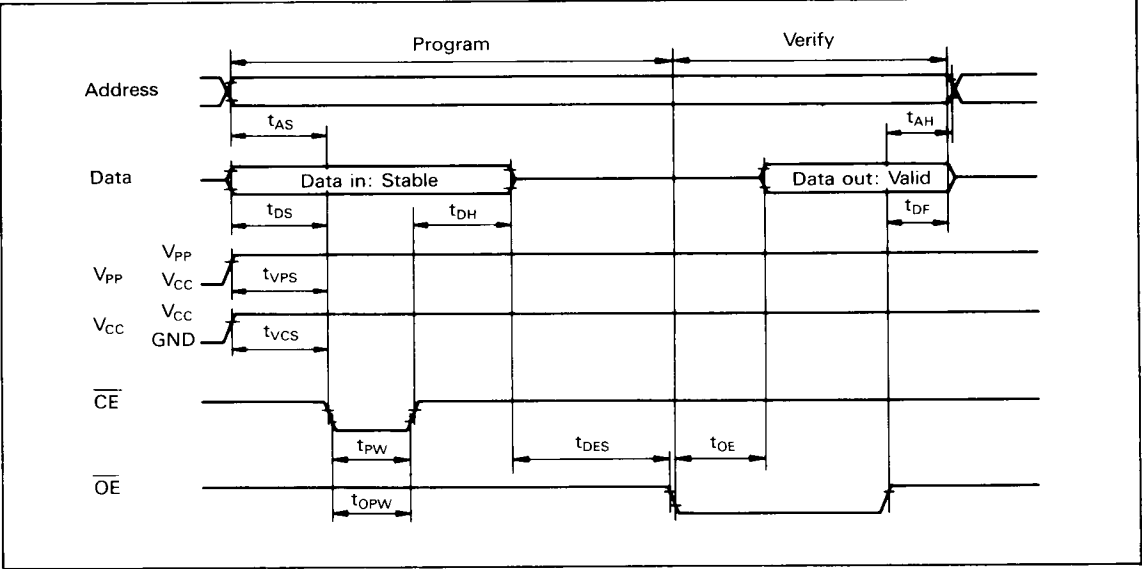


Figure 38 PROM Programming/Verification Timing

HD404302 and HD404304 Option List

Please check off applicable items by ■, ×, or ✓ within □.

1. Package type

☐ DP-42 ☐ DP-42S (Shrink PKG)

2. ZTAT™ compatibility

☐ I/O circuit compatibility with the HD4074308
☐ No I/O circuit compatibility with the HD4074308

Note: ZTAT™ compatibility is enabled only when all pins use C or D type circuits. In this case do not use checklists 3 and 5.

Order data	
Company name	
Department	
Name	
ROM code	
LSI type:	

3. I/O option (I/O options masked by ☐ are not available)

Pin name	I/O	I/O option				
		A	B	C	D	E
D ₀	I/O					
D ₁	I/O					
D ₂	I/O					
D ₃	I/O					
D ₄	I/O					
D ₅	I/O					
D ₆	I/O					
D ₇	I/O					
D ₈	I/O					
D ₉	I/O					
D ₁₀	I/O					
D ₁₁	I/O					
D ₁₂	I/O					
RA RA ₁	I	Use checklist 5				
R0	RO ₀	I/O				
	RO ₁	I/O				
	RO ₂	I/O				
	RO ₃	I/O				
R1	R1 ₀	I/O				
	R1 ₁	I/O				
	R1 ₂	I/O				
	R1 ₃	I/O				
R2	R2 ₀	I/O				
	R2 ₁	I/O				
	R2 ₂	I/O				
	R2 ₃	I/O				

Pin name (Note 1)	I/O	I/O option				
		A	B	C	D	E
R3	R3 ₀	I/O				
	R3 ₁	I/O				
	R3 ₂	I/O				
	R3 ₃	I/O				
	R3 ₄	I/O				
R4	R4 ₀	I/O				
	R4 ₁	I/O				
	R4 ₂	I/O				
	R4 ₃	I/O				
	R4 ₄	I/O				

4. ROM media

☐ EPROM: Emulator type
☐ HD4074308

5. RA₁/V_{disp}

☐ RA₁: Without pull-down MOS (D)
☐ V_{disp}

Note: RA₁/V_{disp} must be selected as V_{disp} except for the case when all high voltage pins are of option E.

Condition

6. OSC₁ and OSC₂ oscillators

<input type="checkbox"/> Ceramic filter	f =	MHz
<input type="checkbox"/> Crystal	f =	MHz
<input type="checkbox"/> External clock	f =	MHz

Please write an O under the pin names to select the following I/O option.

B: CMOS output with pull-up MOS

C: CMOS output

D: Without pull-down MOS (PMOS open drain)

E: With pull-down MOS

Notes: 1. When all pins are selected as C or D, checklists 3 and 5 should not be used.

2. When using R4/AN as the analog input, the I/O option of R4/AN port should be selected as C.