



MIC58P01

8-Bit Parallel-Input Protected Latched Driver

General Description

The MIC58P01 parallel-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Similar to the MIC5801, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and overcurrent shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC58P01 has open-collector outputs capable of sinking 500 mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers may be paralleled for higher load current capability.

With a 5V logic supply, the MIC58P01 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors.

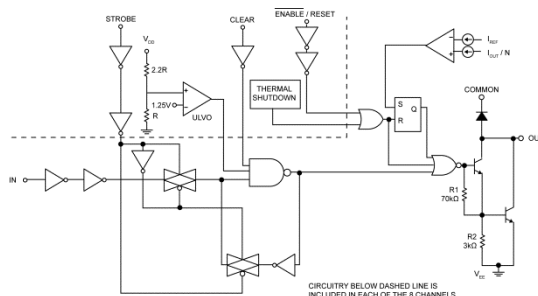
Each of these eight outputs has an independent overcurrent shutdown of 500mA. Upon current shutdown, the affected channel will turn OFF until V_{DD} is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2 μ s will not activate current shutdown. Temperatures above 165°C will shut down all outputs. The UVLO circuit disables the outputs at low V_{DD} ; hysteresis of 0.5V is provided.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- 4.4MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Per-Output Overcurrent Shutdown (500mA typical)
- Under Voltage Lockout
- Thermal Shutdown
- Output Transient Protection Diodes
- CMOS, PMOS, NMOS, and TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

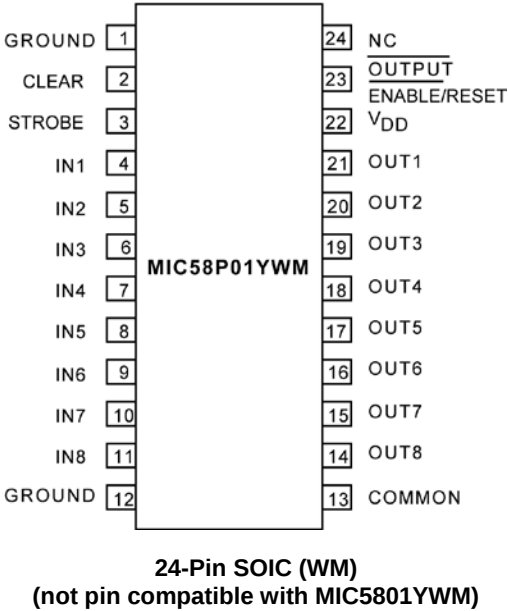
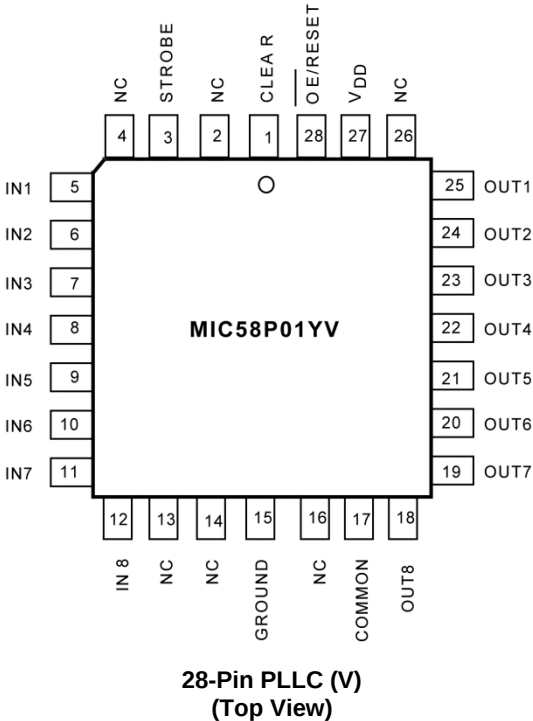
Typical Application



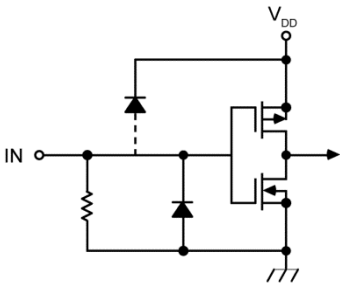
Ordering Information

Part Number	Junction Temperature Range	Package	Pb-Free
MIC58P01YV	−40°C to +85°C	28-Pin PLCC	√
MIC58P01YWM	−40°C to +85°C	28-Pin Wide SOIC	√

Pin Configuration



Typical Input



Pin Description

Pin Number (PLCC)	Pin Number (SOIC)	Pin Name	Pin Function
1	2	CLEAR	Resets all Latches and turns all outputs OFF (open).
3	3	STROBE	Input Strobe Pin. Loads output latches when High.
5 – 12	4 – 11	IN _N	Parallel Inputs, 1 through 8.
15	1, 12	GROUND	Logic and Output Ground pin.
17	13	COMMON	Transient suppression diode common cathode pin.
18 – 25	14 – 21	OUT _N	Parallel Outputs, 8 through 1.
27	22	V _{DD}	Logic Supply voltage.
28	23	<u>OUTPUT</u> ENABLE / RESET	When Low, Outputs are active. When High, outputs are inactive and device is reset from a fault condition. An undervoltage condition emulates a high OE output.

Absolute Maximum Ratings⁽¹⁾

Output Voltage (V_{CE})	+80V
Logic Supply Voltage (V_{DD})	+15V
Input Voltage Range (V_{IN})	-0.3V to V_{DD} +0.3V
Operating Temperature Range (T_A)	-55°C to +85°C
Storage Temperature Range (T_S)	-65°C to +125°C
ESD Rating ⁽³⁾	ESD Sensitive

Operating Ratings⁽²⁾

Package Power Dissipation, P_D	
MIC58P01YV	1.6W
Derate above $T_A = +25^\circ\text{C}$	16mW/°C
MIC58P01YWM	1.4W
Derate above $T_A = +25^\circ\text{C}$	14mW/°C
Operating Temperature Range (T_A)	-40°C to +85°C

Electrical Characteristics⁽⁴⁾

$V_{DD} = 5V$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I _{CEX}	Output Leakage Current	V _{CE} = 80V, T _A = +25°C			50	μA
		V _{CE} = 80V, T _A = +70°C			100	
V _{CE(SAT)}	Collector-Emitter Saturation Voltage	I _C = 100mA		0.9	1.1	V
		I _C = 200mA		1.1	1.3	
		I _C = 350mA		1.3	1.6	
V _{IN(0)}	Input Voltage (Low)				1.0	V
V _{IN(1)}	Input Voltage (High)	V _{DD} = 12V	10.5			
		V _{DD} = 10V	8.5			
		V _{DD} = 5V, Note 5	3.5			
R _{IN}	Input Resistance	V _{DD} = 12V	50	200		kΩ
		V _{DD} = 10V	50	300		
		V _{DD} = 5V	50	600		
I _{DD(1ON)}	Supply Current	One Driver ON, V _{DD} = 12V, Outputs Open		3.3	4.5	mA
		One Driver ON, V _{DD} = 10V, Outputs Open		3.1	4.5	
		One Driver ON, V _{DD} = 5V, Outputs Open		2.4	3.6	
I _{DD(ON)}		All Drivers ON, V _{DD} = 12V, Outputs Open		6.4	10.0	mA
		All Drivers ON, V _{DD} = 10V, Outputs Open		6.0	9.0	
		All Drivers ON, V _{DD} = 5V, Outputs Open		4.7	7.5	
I _{DD(OFF)}		All Drivers OFF, V _{DD} = 12V, Outputs Open, Inputs = 0V		3.0	4.5	mA
		All Drivers OFF, V _{DD} = 5V, Outputs Open, Inputs = 0V		2.2	3.6	
I _R	Clamp Diode Leakage Current	V _R = 80V, T _A = +25°C			50	μA
		V _R = 80V, T _A = +70°C			100	
I _{LIM}	Overcurrent Threshold	Per Output		500		mA
V _{SU}	Start-Up Voltage	Note 6	3.5	4.0	4.5	V

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Micrel CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.
4. Specification for packaged product only.
5. Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".
6. Under-Voltage Lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V.

Electrical Characteristics⁽⁴⁾ (Continued)

$V_{DD} = 5V$, $T_A = 25^{\circ}C$, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{DD\ MIN}$	Minimum Operating V_{DD}		3.0	3.5	4.0	V
V_F	Clamp Diode Forward Voltage	$I_F = 350mA$		1.7	2.0	V
	Thermal Shutdown			165		$^{\circ}C$
	Thermal Shutdown Hysteresis			10		$^{\circ}C$

Truth Table

IN_N	Strobe	Clear	Output Enable	OUT_N	
				$t - 1$	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

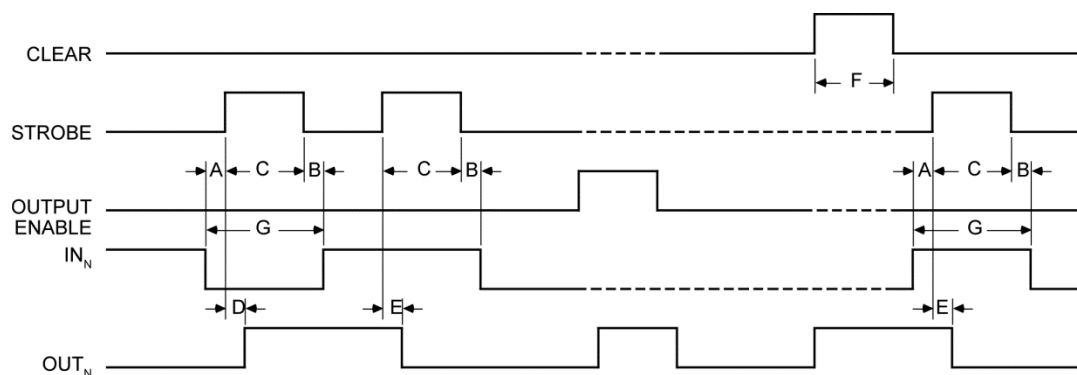
X = Irrelevant

$t - 1$ = Previous output state

t = Present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the Data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches. If current shutdown is activated, the OUTPUT ENABLE must be pulsed high to restore operation. Over temperature faults are not latched and require no reset pulse.

Timing

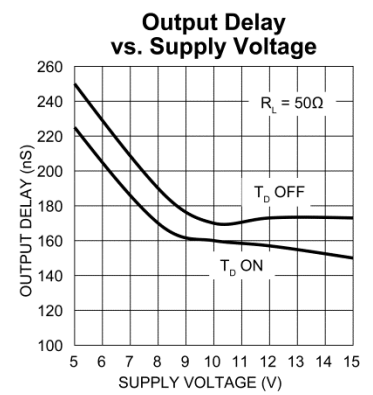
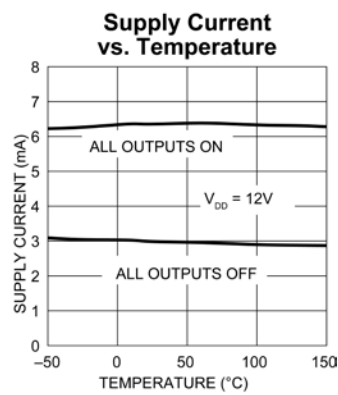
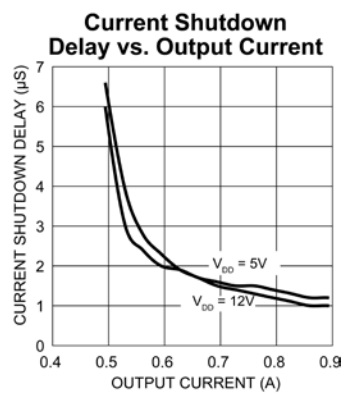
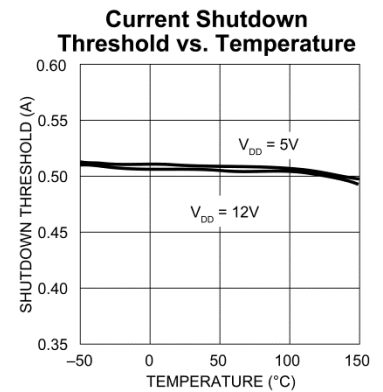
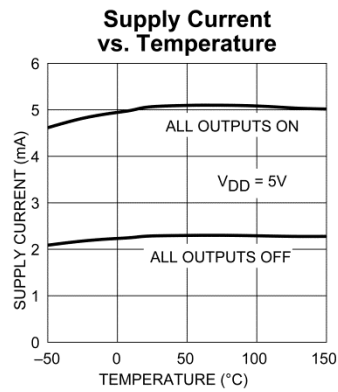
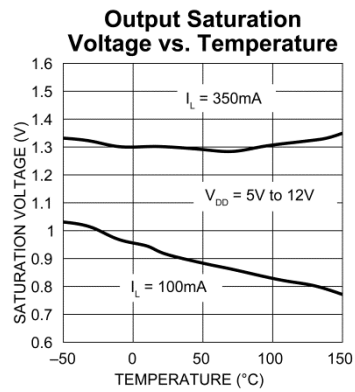


Timing Conditions

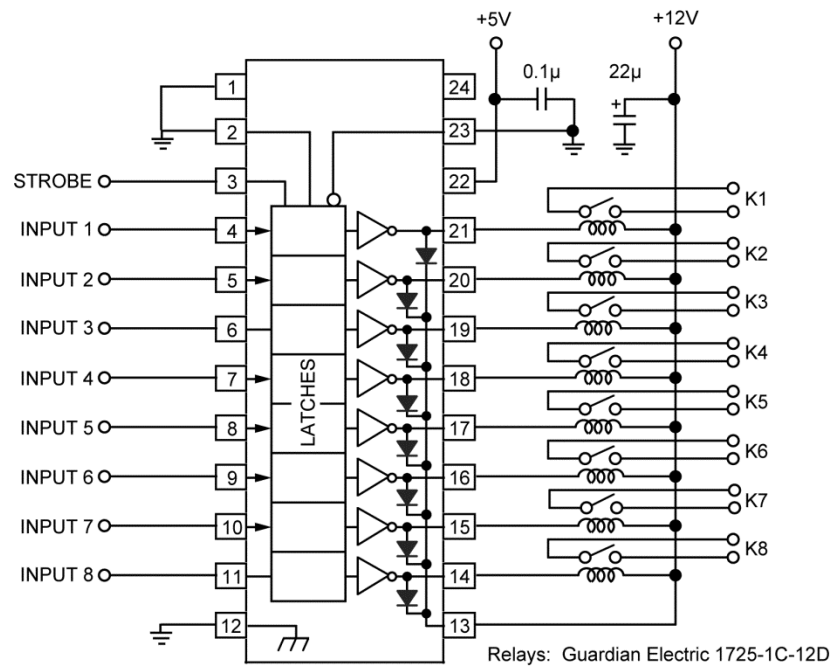
($T_A = +25^\circ\text{C}$, Logic Levels are V_{DD} and Ground, $V_{DD} = 5\text{V}$)

A. Minimum data active time before strobe enabled (data set-up time)	50ns
B. Minimum data active time after strobe disabled (data hold time)	50ns
C. Minimum strobe pulse width	125ns
D. Typical time between strobe activation and output on to off transition	500ns
E. Typical time between strobe activation and output off to on transition	500ns
F. Minimum clear pulse width	300ns
G. Minimum data pulse width	225ns

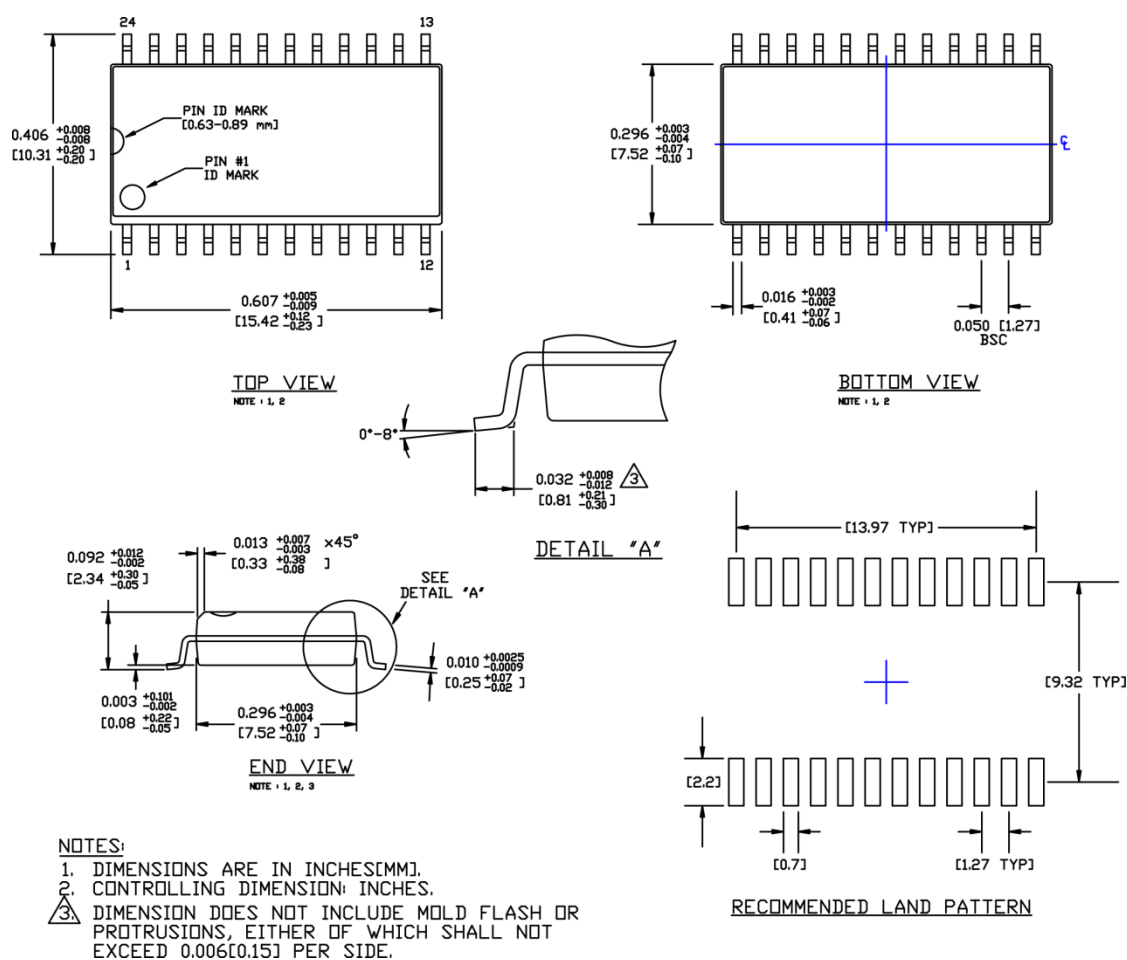
Typical Characteristics



Typical Application Schematic



Package Information and Recommended Landing Pattern⁽⁵⁾

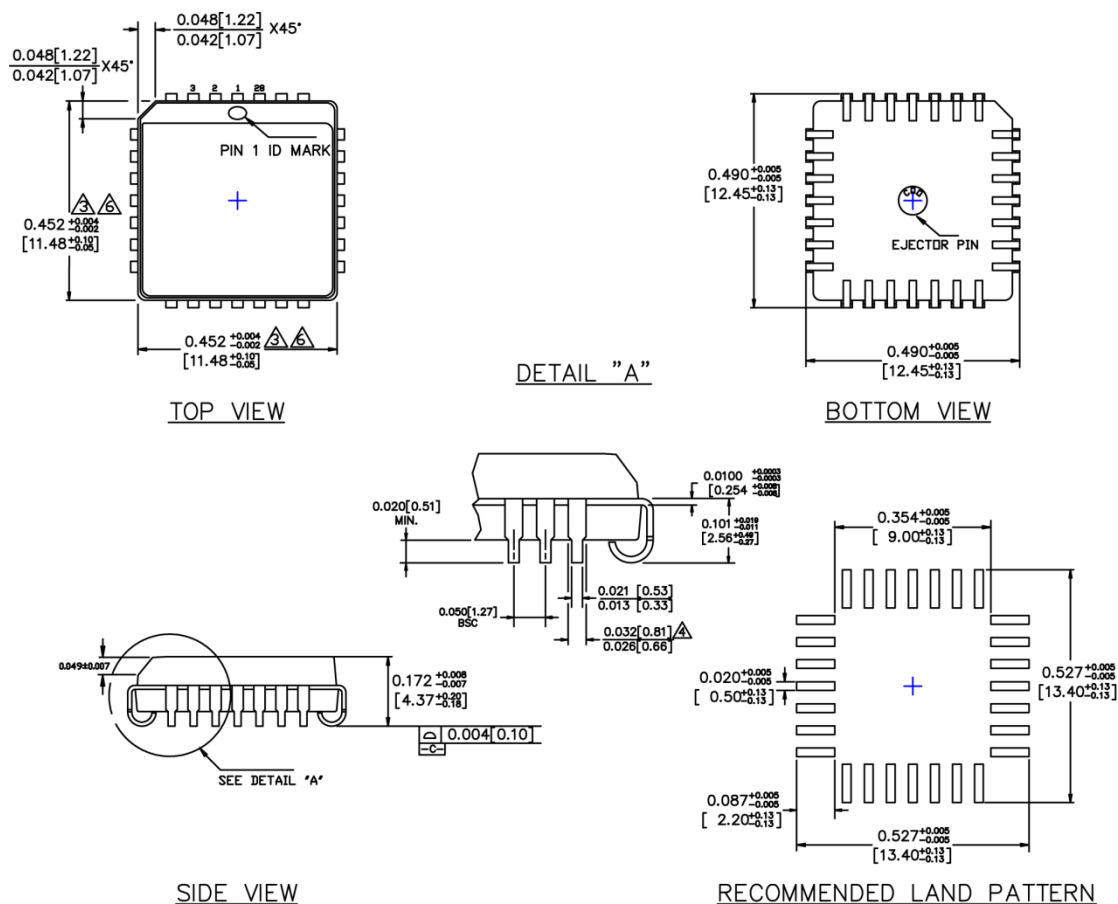


24-Pin Wide SOIC (WM)

Note:

7. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Landing Pattern⁽⁵⁾ (Continued)



NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS : MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

28-Pin PLCC (V)

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