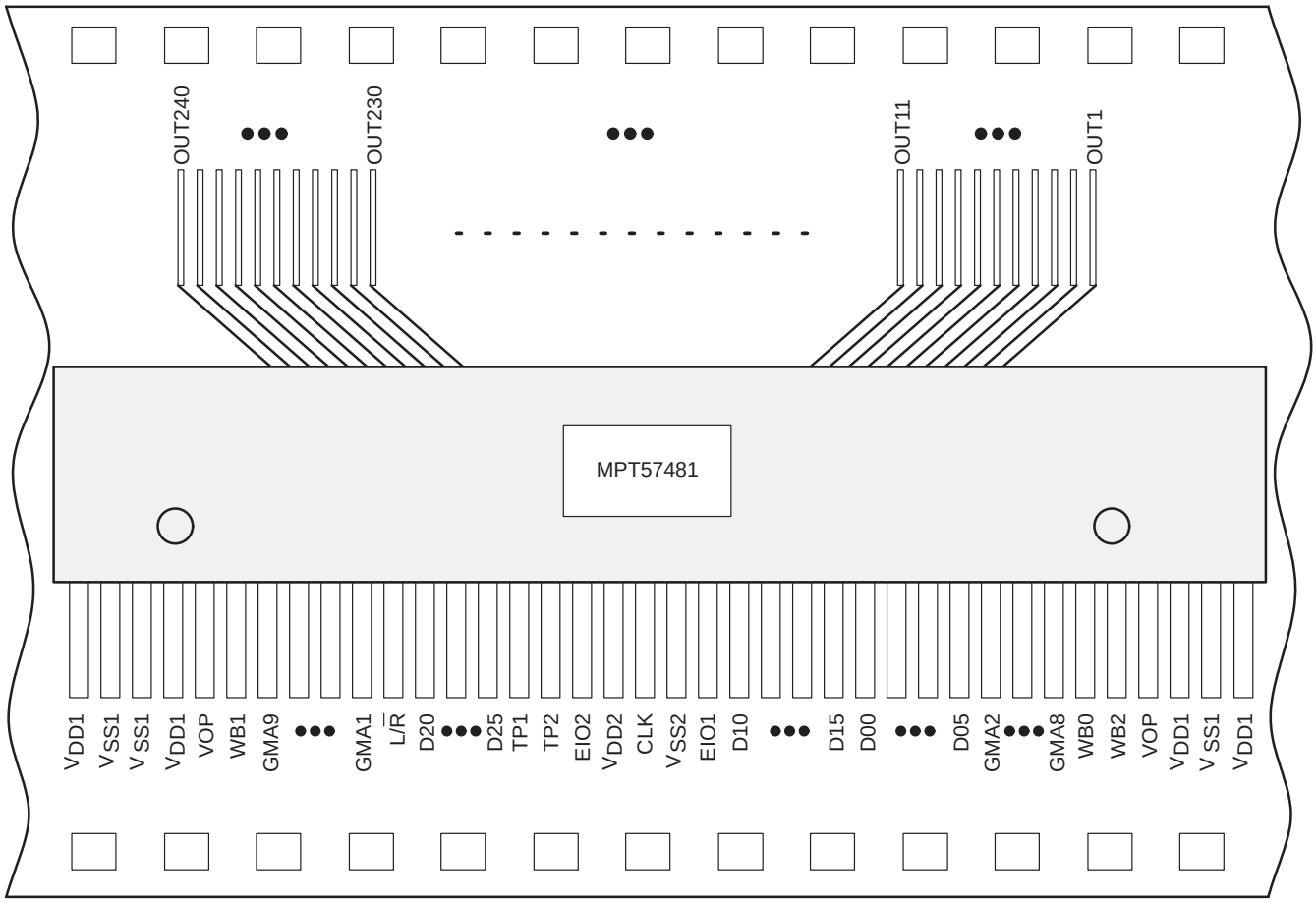
- **436 Terminal 70-mm Tab Assembly**
- **Selection Of Start Driver Input From Right Or Left By $\overline{L}$/R Function**
- **CMOS Technology**
- **6-Bit × 3 RGB Color Data Inputs**
- **64-Gray-Scale Sub-Pixel Outputs Generated By 6-Bit DAC**
- **55-MHz Operation**
- **Gamma Correction**
- **RGB Voltage Adjust**
- **Automatic Low-Power Standby Function**
- **5-V Digital and Analog Voltage Supply**

description

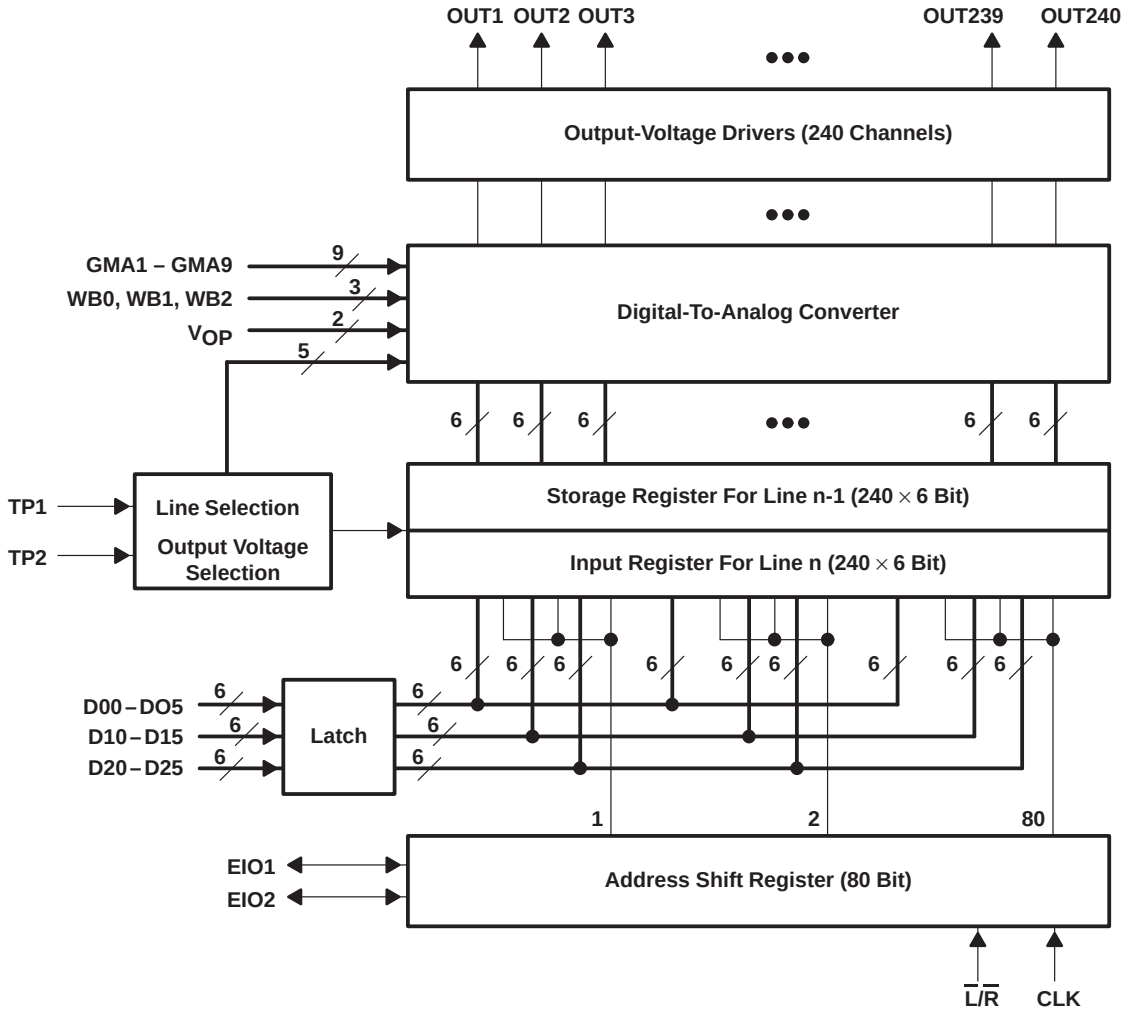
The MPT57481 is a 240-channel output, low-power, 5-V, signal source (column) driver for an active matrix LCD panel. This device has a digital-to-analog converter for each output. The MPT57481 utilizes 10 reference voltages for a 64 gray-scale subpixel output. Eight drivers are required for a 640 × 480 color LCD and ten drivers are required for a 800 × 600 color LCD.



NOTES: A. This figure shows the copper foil side. This figure doesn't describe the TAB outline.
B. There are 46 input terminals and 240 output terminals.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



detailed description

acquisition of line data

Acquisition of line data begins when a start pulse is applied to the EIO1 or EIO2 input terminal and is complete when all 240 channels of the Input Register have been loaded with new RGB data. When the first clock pulse, CLK0, is applied while the EIO terminal is biased high by the start pulse, an enable pulse enters the Shift Register and RGB data enters the Data Latch on the clock's rising edge. The enable pulse, after entering the Shift Register, positions itself to address the Input Register for loading of RGB data from the Data Latch on the rising edge of succeeding clock pulses after CLK0.

With each succeeding clock pulse, CLK (1 – 80), the Input Register is repeatedly addressed by the Shift Register and updated with new RGB data. One of 80 parallel outputs of the Shift Register addresses the Input Register with each transition of the clock pulse. Each output addresses three separate but adjacent channels of the Input Register simultaneously in a ascending or descending order between channels (1..240) as the enable pulse advances to the right or left from one output to the next. Channels (3n–2, 3n–1, and 3n) are addressed on the rising edge of CLKn by each output where 'n' is the number of clock pulse and addressing output.

While channels (3n–2, 3n–1, and 3n) are being addressed by the Shift Register outputs, 18-bit (6 bit $\times$ 3) RGB data stored in the Data Latch is loaded into the channels that are enabled. RGB data, originating at three 6-bit data input terminals, D05..D00, D15..D10, and D25..D20, is routed through the 18-bit Data Latch to the input of channels (3n–2, 3n–1, and 3n), respectively. New RGB data can be entered at the data input terminals and routed to the Input Register with each transition of the clock pulse from 1 to 80. After CLK(80), all 240 channels of the Input Register are addressed and loaded completing the acquisition of RGB line data.

cascading drivers

If the pixels of a LCD display are greater than what one MPT57481 can drive, additional drivers can be cascaded together to extend the RGB line data by connecting the EIO output terminals of one driver to the EIO input terminals of the next driver. Between the rising edges of clock pulse, CLK(d80–1 and d80: d = number of driver), the enable pulse exits the Shift Register of one driver at the EIO output terminal and enters at the EIO input terminal of the next driver. When the enable pulse exits a driver, the driver enters a low-power standby mode while the next driver is set up to receive new RGB input data. The driver in standby mode goes back into normal mode when the next enable start pulse enters at its EIO input terminal.

transfer of line data

RGB line data is transferred from the Input Register to subpixel outputs, OUT (1..240) by a sequence of transitions of the TP1 and TP2 inputs. TP1 and TP2 are biased high while data is being acquired. After line data is acquired, data is transferred to the Storage Register and enters each DAC on the rising edge of the last clock pulse, CLK(d80+1; d = number of last driver) after TP1 transitions to low while TP2 remains high. Transfer of data beyond the Storage Register is independent of the clock. When TP1 or TP2 are low, each DAC is disabled from the subpixel outputs while the panel is precharged by V_{DD1} using the outputs. During the precharging period, line data from the Storage Register, already inside each DAC, is converted to analog voltages during the second and third sequence when TP2 transitions to low with TP1 remaining low, and then when TP1 transitions back to high with TP2 remaining low. After TP1 goes high, line data, now represented as analog voltages, transfers to the output of each DAC. The last sequence, when TP2 goes back to high while TP1 remains high, the precharging period ends and all of the DACs are enabled allowing the analog voltages to transfer to the subpixel outputs.

64 gray scale subpixel outputs

All 240 outputs of the MPT57481 are driven by separate 6-bit DACs. The output voltage of each DAC, 64 gray scale, is determined by the reference voltages GMA(0..9) and WB(0,1, or 2) selected by a 6-bit data input and by the VOP bias voltage. GMA (0..9) gamma correction voltages, WB(0..2) RGB Shift voltages , and VOP

bias voltage can be adjusted to tailor the pixel output voltages needed for the particular LCD panel. GMA and VOP voltages affect all outputs, while WB0, WB1, and WB2 voltages affect only the 3n–2, 3n–1, or 3n outputs, respectively.

calculation of subpixel output voltage

Theoretical calculation of analog voltage with no process deviations assumed.

$$V_O = \frac{(m + 1)\ \big(VA(n + 1)\big) + (7 - m)\ \big(VA(n)\big)}{8} \quad (1)$$

m: Upper 3 bits of 6-bit data
n: Lower 3 bits of 6-bit data

$$VAd = VOP + \frac{8\big(VOP - GMA(d + 1)\big)}{7} + \frac{VOP - Vk}{7} \quad (2)$$

Vk:WB0, WB1, and WB2
d = 0 – 8

graphical representation of output voltage

Calculation of analog voltage is shown graphically in Figure 1. The graph represents the output voltage verse 6-bit data input.

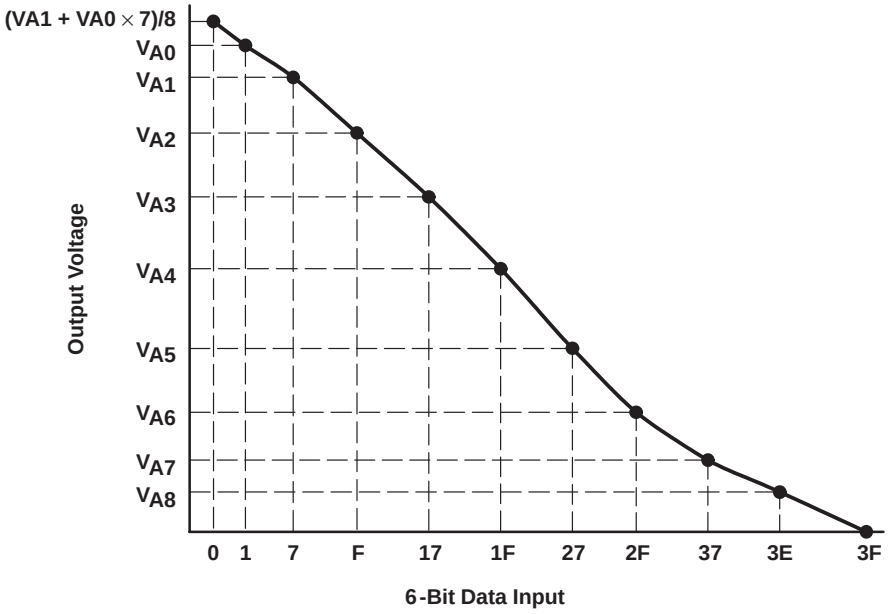


Figure 1. Output Voltage Verse 6-Bit Data Input

timing diagram

terminal functions

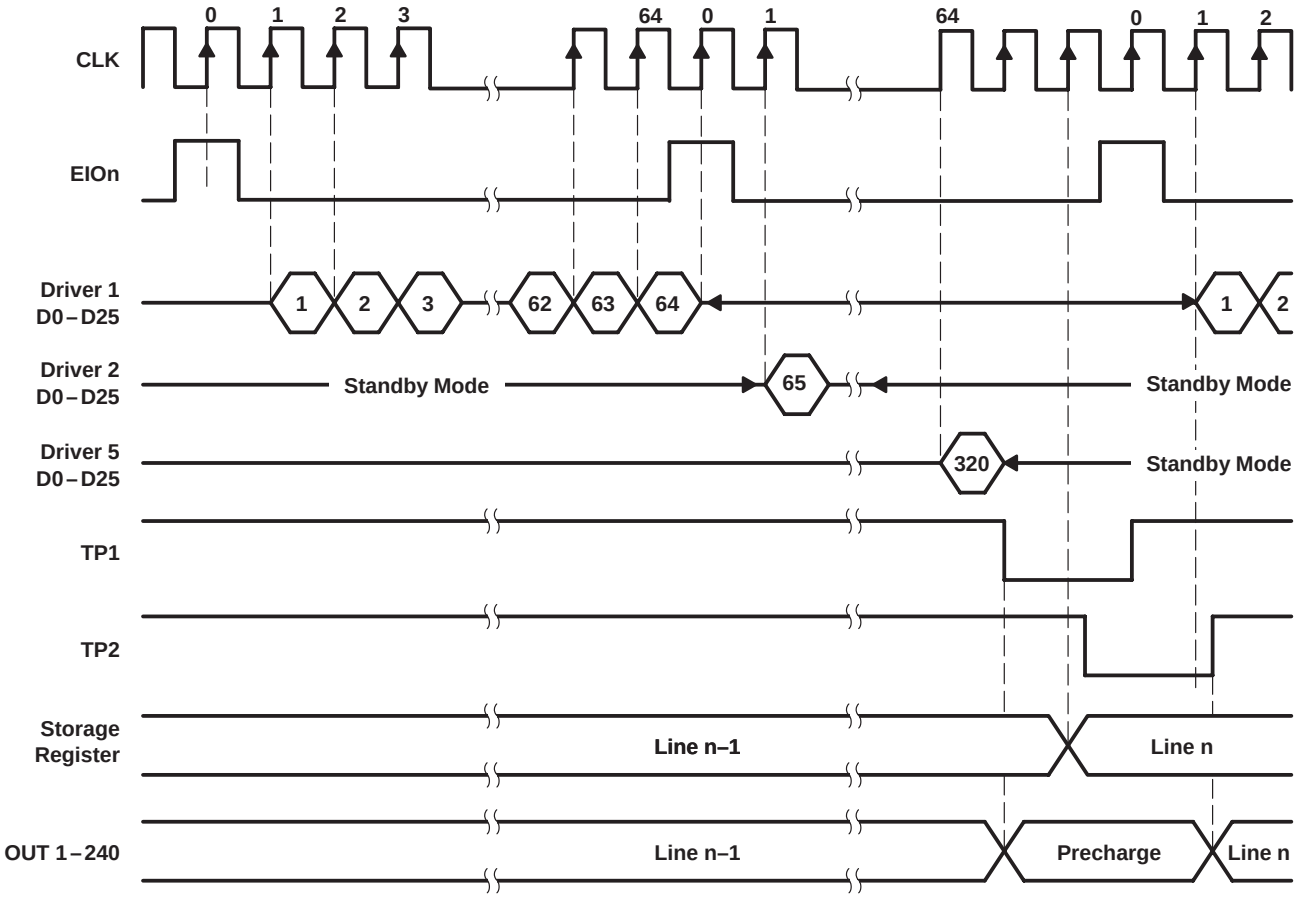


Figure 2.

Terminal Functions

<table>
<tr><th colspan="2">TERMINAL
NAME NO.</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>CLK</td><td></td><td>I</td><td>Shift Clock. CLK synchronizes internal control logic with its rising edge. Also, CLK generates a data clock for the Data Latch, a shift clock for the Address Shift Register, and a write enable for the Storage Register.</td></tr>
<tr><td>D00-D05
D10-D15
D20-D25</td><td></td><td>I</td><td>Data Input. Data inputs consist of 6-bit words for each of three channels (18 bits) for color input data.
● D05..D00 (MSB to LSB) selects one of 64 gray-scale voltages on OUT (3n–2) with n = 1 – 80.
● D15..D10 selects one of 64 gray-scale voltages on OUT (3n–1) with n = 1 – 80.
● D25..D20 selects one of 64 gray-scale voltage on OUT (3n) with n = 1 – 80.</td></tr>
<tr><td>EIO1
EIO2</td><td></td><td>I/O</td><td>Enable I/O. EIO enables the Data Latch and Input Register to load 18-bit RGB data into the input Register on the rising edge of the clocks. The cascade output is for adding additional drivers to extend the length of line data. This helps to accommodate any particular LCD panel being driven.
<table>
<tr><th></th><th>L/$\overline{R}$ = is asserted</th><th>L/$\overline{R}$ is deasserted</th></tr>
<tr><td>EIO1</td><td>Right-shift input</td><td>Left-shift output</td></tr>
<tr><td>EIO2</td><td>Right-shift output</td><td>Left-shift input</td></tr>
</table></td></tr>
<tr><td>GMA1...GMA9</td><td></td><td>I</td><td>Analog circuit bias voltage. GMA supplies the bias voltage to the DAC and the gamma correction voltage adjust reference voltage.</td></tr>
<tr><td>$\overline{L}$/R</td><td></td><td>I</td><td>Shift Direction. $\overline{L}$/R controls the direction in which the data is loaded into the input register. The data is loaded from OUT1 to OUT240 when $\overline{L}/\overline{R}$ is asserted and from OUT240 to OUT1 when $\overline{L}/\overline{R}$ is deasserted.</td></tr>
<tr><td>OUT1-OUT240</td><td></td><td>O</td><td>Subpixel output. Out provides 64 gray-scale signals to the LCD panel.</td></tr>
<tr><td>TP1, TP2</td><td></td><td>I</td><td>Transfer input register contents. The next CLK rising edge after TP1 is deasserted causes the contents of the input register (line n-1) to be transferred to the storage register (line n). After the transfer, the input register receives new line n–1 data from the data inputs. During the period that either TP1, TP2, or both are deasserted, pixel-driver output is in a precharge mode that supplies voltage to all the OUT terminals (LCD pixel drivers)</td></tr>
<tr><td>V_{DD1}</td><td></td><td>I</td><td>Analog supply voltage. The four V_{DD1} terminals supply power for the analog circuitry.</td></tr>
<tr><td>V_{DD2}</td><td></td><td>I</td><td>Power supply for digital circuitry.</td></tr>
<tr><td>VOP</td><td></td><td>I</td><td>Bias voltage. VOP supplies the bias voltage for each DAC.</td></tr>
<tr><td>VSS1</td><td></td><td>I</td><td>Analog circuit ground.</td></tr>
<tr><td>V_{SS2}</td><td></td><td>I</td><td>Digital circuit ground.</td></tr>
<tr><td>WB0, WB1,
WB2</td><td></td><td>I</td><td>Reference voltages. WB0, WB1, WB2 are reference voltages for each third DAC and RGB shift voltage adjust.
● WBO adjusts OUT (3 n - 2) outputs with (n = 1 – 80)
● WB1 adjusts OUT (3 n - 1) outputs with (n = 1 – 80)
● WB2 adjusts OUT (3 n) outputs with (n = 1 – 80)</td></tr>
</table>

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (V_{DD1}, V_{DD2}) (see Note 1) . . . . . –0.3 V to +7 V
Input voltage, V_I (GMA1 – GMA9, VOP, WB0–WB2) . . . . . –0.3 V to V_{DD1}+ 0.3 V
Input voltage, V_I (all other terminals) . . . . . –0.3 V to V_{DD2}+ 0.3 V
Output voltage, V_O (EIO1, EIO2) . . . . . –0.3 V to V_{DD2}+ 0.3 V
Output voltage, V_O (OUT1 – OUT240) . . . . . –0.3 V to V_{DD2}+ 0.3 V
Operating temperature range, T_A . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}, (V_{DD1},V_{DD2}) (See Note 2)	4.5	5	5.5	V
DAC bias supply voltage (VOP)	V_{DD1}/2-0.2	V_{DD1}/2	V_{DD1}/2-0.2	V
DAC reference voltage (GMA1 – GMA9)	0		V_{DD1}	
DAC reference voltage (WB0...WB2)	0		V_{DD}	V
Clock frequency, f_{clk}			55	MHz
Load capacitance for pixel outputs, C_L			150	pF
Operating Free-air Temperature, T_A	–55		125	°C

2. V_{DD1} and V_{DD2} are connected directly together. V_{SS1} and V_{SS2} are connected directly together. Power on sequence: $V_{DD1} \rightarrow V_{DD2} \rightarrow$ GMA1...GMA9 $\rightarrow$ input voltage.

electrical characteristics over recommended operating conditions (unless otherwise noted), V_{DD1}, V_{DD2} = 5 V (see Note 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High level input voltage	Dx0 – Dx5, CLK, TP1, TP2, EIO1, EIO2			2.2			V
		$\overline{L/R}$			0.7 V_{DD2}			
V_{IL}	Low level input voltage	Dx0 – Dx5, CLK, TP1, TP2, EIO1, EIO2					0.8	V
		$\overline{L/R}$					0.3 V_{DD2}	
I_{IK}	Input leakage current	Dx0 – Dx5, CLK, $\overline{TP1}$, TP2, EIO1, EIO2, L/R			–10		10	µA
$I_{O(1)}$	Output current	OUT1 – 240	TP1, TP2 = 0 V,	V_O = 4 V		–1.5		mA
$I_{O(2)}$			TP1, TP2 = 5 V, Dx5 – Dx0 = 00h	V_O = 4 V,		–10		
$I_{O(3)}$			TP1, TP2 = 5 V, Dx5 – Dx0 = 63h	V_O = 4 V,		0.8		
V_O	Subpixel output error (see Note 4)	OUT1 – 240					±30	mV
V_O	Subpixel output voltage range (see Note 5)	OUT1 – 240			V_{SS1} +0.2		V_{DD1}–0.2	V
I_{DD}	Supply current	V_{DD1}	Hsync = 30 µs,	No load		9		mA
			Hsync = 30 µs,	See Note 6		5		
		V_{DD2}	Hsync = 30 µs,	No load		5		

† All typical values are at V_{DD1}, V_{DD2} = 5 V and T_A = 25°C.

NOTES: 3. For this table, the following are true: GMA1 – GMA9 = 0.5 V to 4.5 V in increments of 0.5 V, VOP = 2.5 V and WB0 – WB2 = 2.5 V.
4. V_O is the difference between the highest and the lowest reading across OUT1 – OUT240.
5. This is the range of output voltage between 6-bit input data 00h and 63h.
6. The load consists of a 75-pF capacitor connected from the output to V_{SS} and in parallel with a series combination of a 75-pF capacitor and a 2-kΩ resistor.

timing requirements over recommended operating free-air temperature range, V_{DD1}, V_{DD2} = 5 V, See Note 7

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{c1}	Clock cycle time	See Figure 3	18			ns
t_{w1}	High-level pulse width duration	See Figure 3	5			ns
t_{w2}	Low-level pulse width duration	See Figure 3	5			ns
t_{su1}	Data setup time	See Figure 3, Figure 4, and Figure 5	5			ns
t_{h1}	Data hold time	See Figure 3, Figure 4, and Figure 5	5			ns
t_{su2}	Start pulse setup time	See Figure 3 and Figure 4	5			ns
t_{h2}	Start pulse hold time	See Figure 3 and Figure 4	5			ns
t_{su3}	Enable propagation setup time	See Figure 3	80			CLK
$t_{(pc)}$	Precharge time	See Figure 3	3			µs
t_{h3}	TP1 hold time (with respect to TP2)	See Figure 3	1			µs
t_{su4}	TP1 setup time (with respect to TP2)	See Figure 3	1			µs
t_{h4}	TP2 hold time (with respect to TP1)	See Figure 3	0.5			µs
t_{su5}	TP1 shift input setup time	See Figure 3	1			CLK
t_{dis1}	Data input disable time	See Figure 4	1			CLK
$t_{(last)}$	Last data timing	See Figure 5	1			CLK
t_{su6}	TP1 setup time (with respect to CLK)	See Figure 5	7			ns
t_{h5}	TP1, CLK hold time (with respect to CLK)	See Figure 5	7			ns

NOTE 7: All V_{IH} and V_{IL} input voltage levels are 5 V and 0 V, respectively.

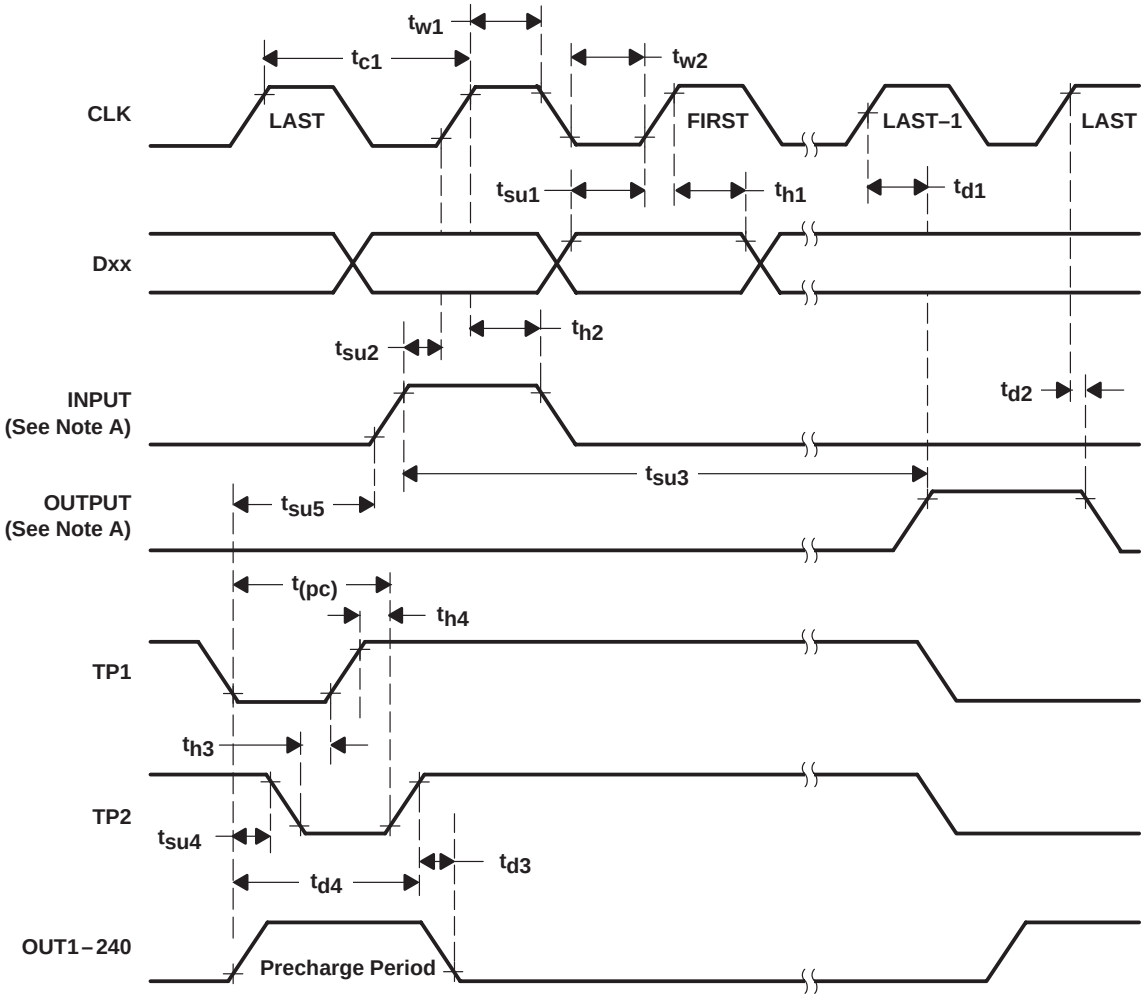
switching characteristics over recommended operating free-air temperature range, V_{DD1}, V_{DD2} = 5 V, See Figure 3 and Note 7

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{d1}	Enable propagation delay time	C_L = 35 pF				11	ns
t_{d2}	Enable propagation delay time	C_L = 35 pF				15	ns
t_{d3}	Output propagation delay time	C_{L1}. C_{L2}= 75 pF, See Note 6	R_L = 2 kΩ,			3	ns
t_{d4}	Output propagation delay time	C_{L1}. C_{L2}= 75 pF, See Note 6	R_L = 2 kΩ,			10	ns

NOTES: 6. The load consists of a 75-pF capacitor connected from the output to V_{SS} and in parallel with a series combination of a 75-pF capacitor and a 2-kΩ resistor.

7. All V_{IH} and V_{IL} input voltage levels are 5 V and 0 V, respectively.

PARAMETER MEASUREMENT INFORMATION



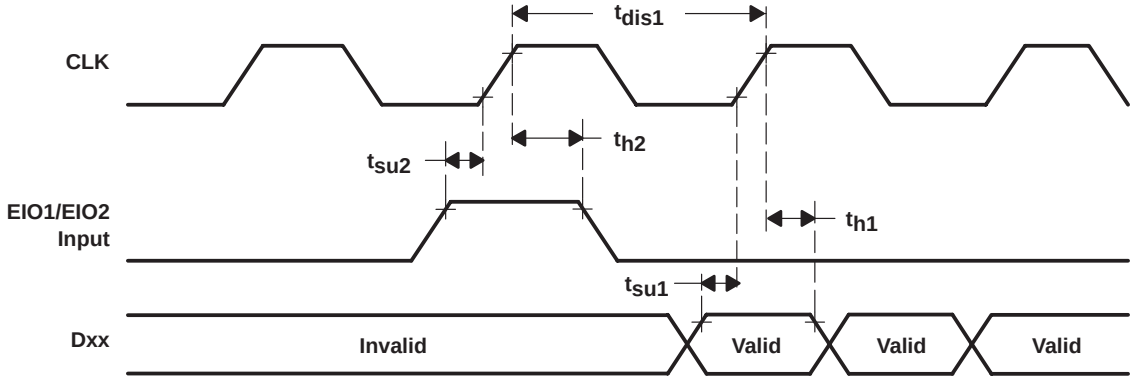
NOTES: A. EIO1 ($\overline{L}/\overline{R}$ is asserted), EIO2 ($\overline{L}/\overline{R}$ is asserted)

B. The input pulse is supplied by a generator having the following characteristics: PRR < 1 MHz, duty cycle < 50%, t_r, $t_f \leq 15$ ns, $z_O = 50\ \Omega$.

C. The trip point for t_{d3} is output voltage + 0.5 V. The trip point for t_{d4} is output voltage ±100 mV.

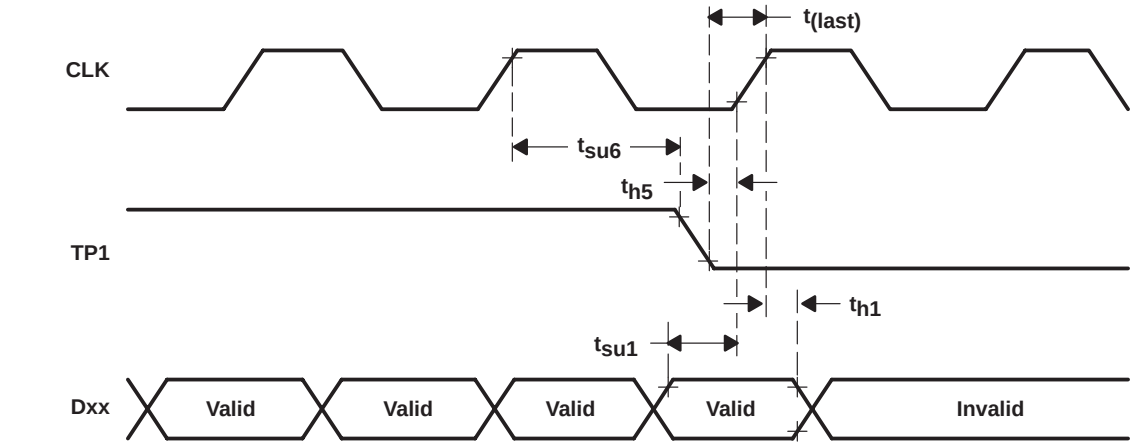
Figure 3. Input, Output, and Precharge Period Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A. The input pulse is supplied by a generator having the following characteristics: PRR < 1 MHz, duty cycle < 50%, t_r, t_f ≤ 15 ns, z_O = 50 Ω.

Figure 4. EIO1/EIO2 Input and Data Valid Timing Waveforms



NOTE A. The input pulse is supplied by a generator having the following characteristics: PRR < 1 MHz, duty cycle < 50%, t_r, t_f ≤ 15 ns, z_O = 50 Ω.

Figure 5. TP1 and Data Valid Timing Waveforms

APPLICATION INFORMATION

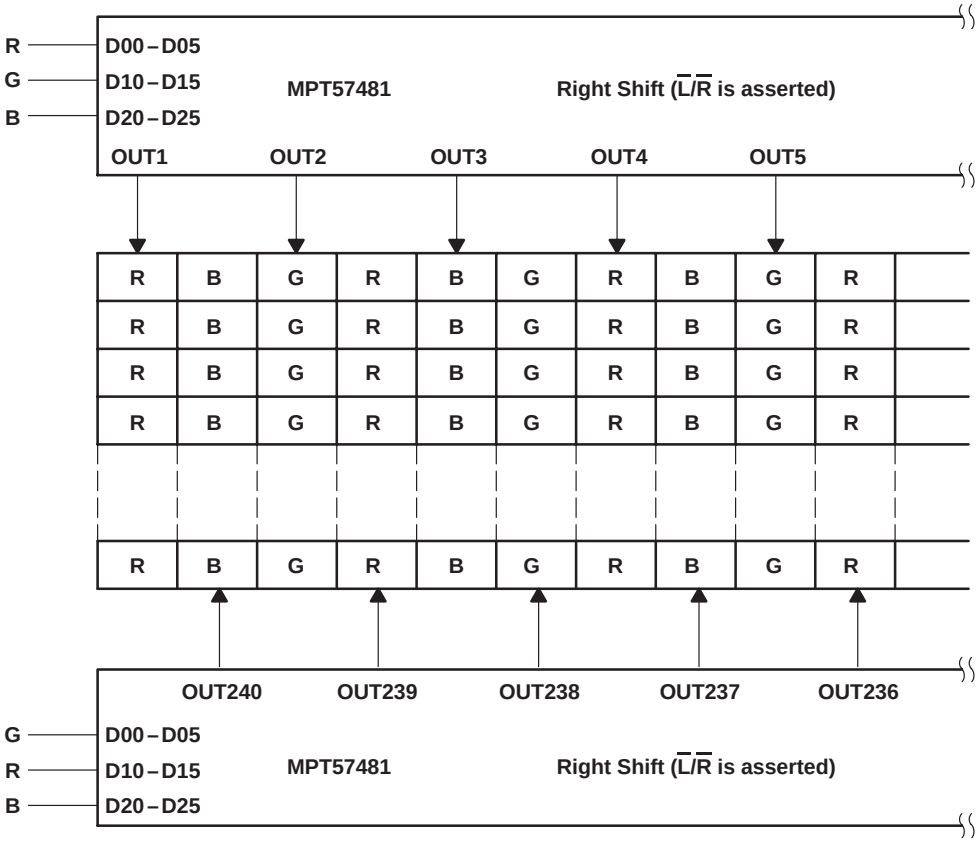


Figure 6. MPT57481 Connections to a Strip-Type Color-Filter Panel

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