



CYPRESS

CY28312B-2

## FTG for VIA™ K7 Series Chipset with Programmable Output Frequency

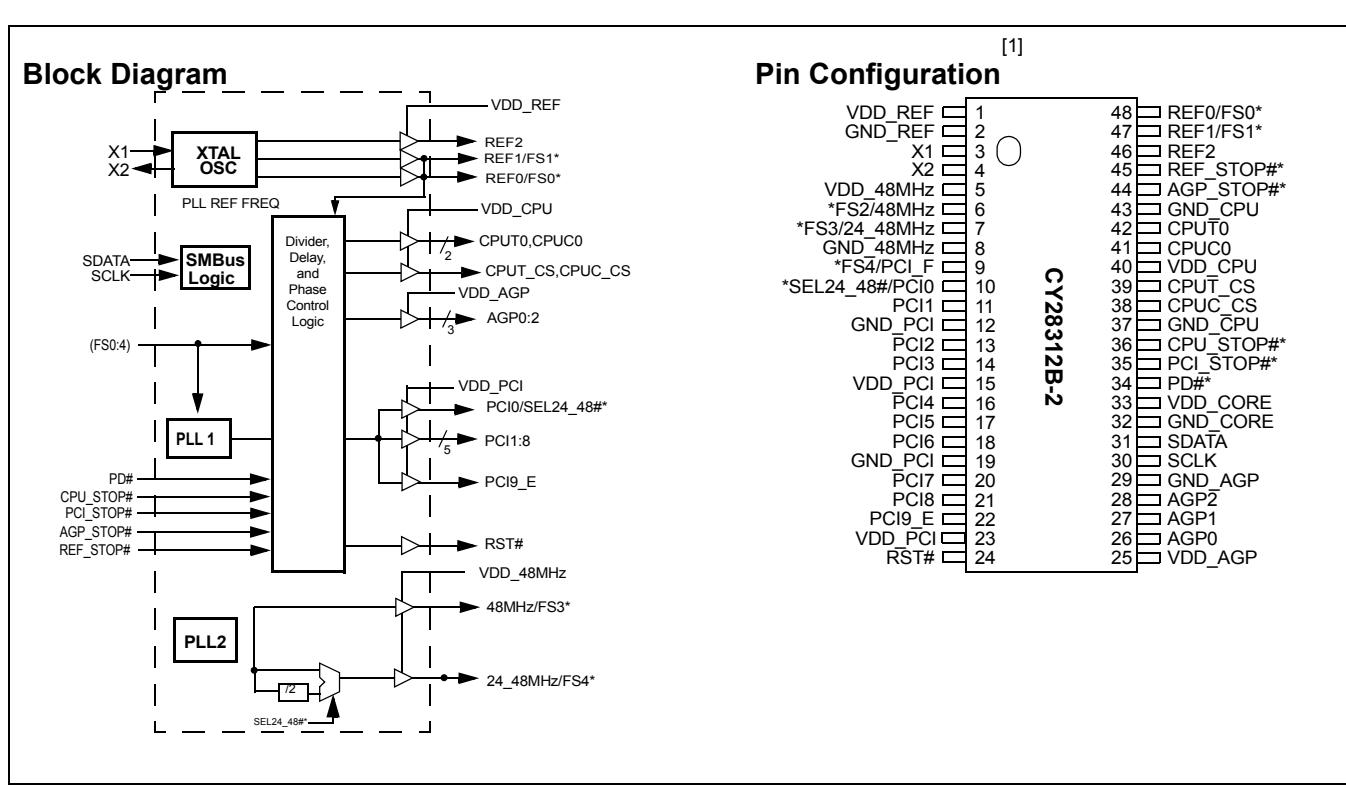
### Features

- Single-chip FTG solution for VIA™ K7 Series chipsets
- Programmable clock output frequency with less than 1-MHz increment
- Integrated fail-safe Watchdog timer for system recovery
- Automatically switch to HW-selected or SW-programmed clock frequency when Watchdog timer time-out
- Capable of generating system RESET after a Watchdog timer time-out occurs or a change in output frequency via SMBus interface
- Support SMBus byte read/write and block read/write operations to simplify system BIOS development
- Vendor ID and Revision ID support
- Programmable drive strength for PCI output clocks
- Programmable output skew between CPU, AGP and PCI
- Maximized electromagnetic interference (EMI) suppression using Cypress's Spread Spectrum technology

- Low jitter and tightly controlled clock skew
- Two pairs of differential CPU clocks
- Eleven copies of PCI clocks
- Three copies of 66-MHz outputs
- Two copies of 48-MHz outputs
- Three copies of 14.31818-MHz reference clocks
- One RESET output for system recovery
- Power management control support

### Key Specifications

|  |        |
|--|--------|
| CPU outputs cycle-to-cycle jitter:               | 250 ps |
| 48-MHz, 3V66, PCI outputs cycle-to-cycle jitter: | 250 ps |
| CPU 3V66 output skew:                            | 200 ps |
| 48-MHz output skew:                              | 250 ps |
| PCI output skew:                                 | 500 ps |



**Note:**

1. Internal 100K pull-up resistors present on inputs marked with \*. Design should not rely solely on internal pull-up resistor to set I/O pins HIGH.

**Pin Definitions**

| Pin Name            | Pin No.                        | Pin Type          | Pin Description  |
|---------------------|--------------------------------|-------------------|--|
| REF0/FS0            | 48                             | I/O               | <b>Reference Clock Output 0/Frequency Select 0.</b> 3.3V 14.318-MHz clock output. REF0 will be disabled when REF_STOP# is active. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 4</i> .                  |
| REF1/FS1            | 47                             | I/O               | <b>Reference Clock Output 0/Frequency Select 1.</b> 3.3V 14.318-MHz clock output. REF1 will be disabled when REF_STOP# is active. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 4</i> .                  |
| REF2                | 46                             | I/O               | <b>Reference Clock Output 2.</b> 3.3V 14.318-MHz clock output. REF2 will be disabled when REF_STOP# is active.   |
| X1                  | 3                              | I                 | <b>Crystal Input.</b> This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.  |
| X2                  | 4                              | I                 | <b>Crystal Output.</b> An input connection for an external 14.318-MHz crystal connection. If using an external reference, this pin must be left unconnected.   |
| PCI_F/FS4           | 9                              | I                 | <b>Free-Running PCI Clock/Frequency Select 4.</b> 3.3V 33-MHz free running PCI clock output. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 4</i> .   |
| PCI_0/SEL24_48#     | 10                             | I/O               | <b>PCI Clock 0/Select 24 or 48 MHz.</b> 3.3V 33-MHz PCI clock outputs. This output will be disabled when PCI_STOP# is active. This pin also serves as the select strap to determine device operating frequency of 24_48MHz output.                                   |
| PCI1:8              | 11, 13, 14, 16, 17, 18, 20, 21 | O                 | <b>PCI Clock 1 through 8.</b> 3.3V 33-MHz PCI clock outputs. PCI1:8 will be disabled when PCI_STOP# is active.   |
| PCI9_E              | 22                             | O                 | <b>Early PCI Clock 9.</b> 3.3V 33-MHz PCI clock outputs. PCI9_E will be disabled when PCI_STOP# is active.   |
| AGP0:2              | 26, 27, 28                     | O                 | <b>AGP Clock 0 through 2.</b> 3.3V 66-MHz clock outputs. The operating frequency is controlled by FS0:4 (see <i>Table 4</i> ). AGP0:2 will be disabled when AGP_STOP# is active.   |
| 48MHz/FS2           | 6                              | I/O               | <b>48-MHz Output/Frequency Selection 3.</b> 3.3V 48-MHz non-spread spectrum output. 48 MHz will be disabled when REF_STOP# is active. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 4</i> .              |
| 24_48MHz/FS3        | 7                              | I/O               | <b>24- or 48-MHz Output/Select 24 or 48 MHz.</b> 3.3V 24 or 48-MHz non-spread spectrum output. 24_48MHz will be disabled when REF_STOP# is active. This pin also serves as the select strap to determine device operating frequency as described in <i>Table 4</i> . |
| RST#                | 24                             | O<br>(open-drain) | <b>Reset#.</b> Open-drain RESET# output.   |
| CPUT0, CPUC0        | 42, 41                         | O<br>(open-drain) | <b>CPU Clock Output 0.</b> CPUT0 and CPUC0 are the differential CPU clock outputs for the K7 processor. They are open-drain outputs.   |
| CPUT_CS,<br>CPUC_CS | 39, 38                         | O                 | <b>CPU Clock Output for Chipset.</b> CPUT_CS and CPUC_CS are the differential CPU clock outputs for the chipset. They are push-pull outputs. These outputs will be disabled when CPU_STOP# is active.  |
| CPU_STOP#           | 36                             | I                 | <b>CPU STOP Input.</b> This input will disable CPUT_CS and CPUC_CS when it is active.  |
| PCI_STOP#           | 35                             | I                 | <b>PCI STOP Input.</b> This input will disable PCI0:8 and PCI9_E when it is active.  |
| AGP_STOP#           | 44                             | I                 | <b>AGP STOP Input.</b> This input will disable AGP0:2 when it is active.   |
| REF_STOP#           | 45                             | I                 | <b>REF STOP Input.</b> This input will disable REF0:2, 24_48MHz and 48 MHz outputs when it is active.  |
| PD#                 | 34                             | I                 | <b>Power-down Input.</b> This input will trigger the clock generator into Power-down mode when it is active.   |

**Pin Definitions** (continued)

| Pin Name  | Pin No.                 | Pin Type | Pin Description   |
|---|-------------------------|----------|---|
| SDATA   | 31                      | I/O      | <b>Data pin for SMBus circuitry.</b>  |
| SCLK  | 30                      | I        | <b>Clock pin for SMBus circuitry.</b>   |
| VDD_CPU   | 40                      | P        | <b>2.5V Power Connection.</b> Power supply for CPU output buffers. Connect to 2.5V.       |
| VDDQ_AGPG   | 25                      | P        | <b>3.3V Power Connection.</b> Power supply for AGP output buffers. Connect to 3.3V.       |
| VDDQ_PCI  | 15, 23                  | P        | <b>3.3V Power Connection.</b> Power supply for PCI output buffers. Connect to 3.3V.       |
| VDDQ_48MHz  | 5                       | P        | <b>3.3V Power Connection.</b> Power supply for 48-MHz output buffers. Connect to 3.3V.    |
| VDD_REF   | 1                       | P        | <b>3.3V Power Connection:</b> Power supply for reference output buffers. Connect to 3.3V. |
| VDD_Core  | 33                      | P        | <b>3.3V Power Connection:</b> Power supply for PLL core. Connect to 3.3V.                 |
| GND_REF,<br>GND_48MHz,<br>GND_PCI,<br>GND_AGPG,<br>GND_Core,<br>GND_CPU | 2, 8, 29, 32, 37,<br>43 | G        | <b>Ground Connections:</b> Connect all ground pins to the common system ground plane.     |

**Serial Data Interface**

The CY28312B-2 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions.

**Data Protocol**

The clock driver serial protocol supports byte/word write, byte/word read, block write and block read operations from the

controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. For byte/word write and byte read operations, system controller can access individual indexed byte. The offset of the indexed byte is encoded in the command code.

The definition for the command code is defined in *Table 1*.

| Bit | Descriptions   |
|-----|--|
| 7   | 0 = Block read or block write operation<br>1 = Byte/Word read or byte/word write operation                                     |
| 6:0 | Byte offset for byte/word read or write operation. For block read or write operations, these bits need to be set at '0000000'. |

**Table 1. Block Read and Block Write Protocol**

| Block Write Protocol |  | Block Read Protocol |  |
|----------------------|--|---------------------|--|
| Bit                  | Description  | Bit                 | Description  |
| 1                    | Start  | 1                   | Start  |
| 2:8                  | Slave address – 7 bits   | 2:8                 | Slave address – 7 bits   |
| 9                    | Write  | 9                   | Write  |
| 10                   | Acknowledge from slave   | 10                  | Acknowledge from slave   |
| 11:18                | Command Code – 8 bits<br>'00000000' stands for block operation | 11:18               | Command Code – 8 bits<br>'00000000' stands for block operation |
| 19                   | Acknowledge from slave   | 19                  | Acknowledge from slave   |
| 20:27                | Byte Count – 8 bits  | 20                  | Repeat start   |
| 28                   | Acknowledge from slave   | 21:27               | Slave address – 7 bits   |
| 29:36                | Data byte 0 – 8 bits   | 28                  | Read   |
| 37                   | Acknowledge from slave   | 29                  | Acknowledge from slave   |
| 38:45                | Data byte 1 – 8 bits   | 30:37               | Byte count from slave – 8 bits                                 |
| 46                   | Acknowledge from slave   | 38                  | Acknowledge  |

**Table 1. Block Read and Block Write Protocol (continued)**

| Block Write Protocol |                                  | Block Read Protocol |                                   |
|----------------------|----------------------------------|---------------------|-----------------------------------|
| Bit                  | Description                      | Bit                 | Description                       |
| ...                  | Data Byte N/Slave Acknowledge... | 39:46               | Data byte from slave – 8 bits     |
| ...                  | Data Byte N – 8 bits             | 47                  | Acknowledge                       |
| ...                  | Acknowledge from slave           | 48:55               | Data byte from slave – 8 bits     |
| ...                  | Stop                             | 56                  | Acknowledge                       |
|                      |                                  | ...                 | Data bytes from slave/Acknowledge |
|                      |                                  | ...                 | Data byte N from slave – 8 bits   |
|                      |                                  | ...                 | Not Acknowledge                   |
|                      |                                  | ...                 | Stop                              |

**Table 2. Word Read and Word Write Protocol**

| Word Write Protocol |  | Word Read Protocol |  |
|---------------------|--|--------------------|--|
| Bit                 | Description  | Bit                | Description  |
| 1                   | Start  | 1                  | Start  |
| 2:8                 | Slave address – 7 bits   | 2:8                | Slave address – 7 bits   |
| 9                   | Write  | 9                  | Write  |
| 10                  | Acknowledge from slave   | 10                 | Acknowledge from slave   |
| 11:18               | Command Code – 8 bits<br>'1xxxxxxx' stands for byte or word operation<br>bit[6:0] of the command code represents the offset of the byte to be accessed | 11:18              | Command Code – 8 bits<br>'1xxxxxxx' stands for byte or word operation<br>bit[6:0] of the command code represents the offset of the byte to be accessed |
| 19                  | Acknowledge from slave   | 19                 | Acknowledge from slave   |
| 20:27               | Data byte low – 8 bits   | 20                 | Repeat start   |
| 28                  | Acknowledge from slave   | 21:27              | Slave address – 7 bits   |
| 29:36               | Data byte high – 8 bits  | 28                 | Read   |
| 37                  | Acknowledge from slave   | 29                 | Acknowledge from slave   |
| 38                  | Stop   | 30:37              | Data byte low from slave – 8 bits  |
|                     |  | 38                 | Acknowledge  |
|                     |  | 39:46              | Data byte high from slave – 8 bits   |
|                     |  | 47                 | NOT acknowledge  |
|                     |  | 48                 | Stop   |

**Table 3. Byte Read and Byte Write Protocol**

| Byte Write Protocol |  | Byte Read Protocol |  |
|---------------------|--|--------------------|--|
| Bit                 | Description  | Bit                | Description  |
| 1                   | Start  | 1                  | Start  |
| 2:8                 | Slave address – 7 bits   | 2:8                | Slave address – 7 bits   |
| 9                   | Write  | 9                  | Write  |
| 10                  | Acknowledge from slave   | 10                 | Acknowledge from slave   |
| 11:18               | Command Code – 8 bits<br>'1xxxxxxx' stands for byte operation<br>bit[6:0] of the command code represents the offset of the byte to be accessed | 11:18              | Command Code – 8 bits<br>'1xxxxxxx' stands for byte operation<br>bit[6:0] of the command code represents the offset of the byte to be accessed |
| 19                  | Acknowledge from slave   | 19                 | Acknowledge from slave   |
| 20:27               | Data byte – 8 bits   | 20                 | Repeat start   |
| 28                  | Acknowledge from slave   | 21:27              | Slave address – 7 bits   |
| 29                  | Stop   | 28                 | Read   |

**Table 3. Byte Read and Byte Write Protocol** (continued)

| Byte Write Protocol |             | Byte Read Protocol |                               |
|---------------------|-------------|--------------------|-------------------------------|
| Bit                 | Description | Bit                | Description                   |
|                     |             | 29                 | Acknowledge from slave        |
|                     |             | 30:37              | Data byte from slave – 8 bits |
|                     |             | 38                 | Not Acknowledge               |
|                     |             | 39                 | Stop                          |

**CY28312B-2 Serial Configuration Map**

The serial bits will be read by the clock driver in the following order:

Byte 0–Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1–Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N–Bits 7, 6, 5, 4, 3, 2, 1, 0

All unused register bits (reserved and N/A) should be written to a “0” level.

All register bits labeled “Initialize to 0” must be written to zero during initialization.

**Byte 0: Control Register 0**

| Bit   | Pin# | Name           | Default | Description  |
|-------|------|----------------|---------|--|
| Bit 7 | –    | Spread Enable  | 0       | 0 = Disabled<br>1 = Enabled  |
| Bit 6 | –    | Spread Select2 | 0       | ‘000’ = ±0.25%   |
| Bit 5 | –    | Spread Select1 | 0       | ‘001’ = –0.5%<br>‘010’ = ±0.5%   |
| Bit 4 | –    | Spread Select0 | 0       | ‘011’ = ±0.38%<br>‘100’ = Reserved<br>‘101’ = Reserved<br>‘110’ = Reserved<br>‘111’ = Reserved |
| Bit 3 | –    | SEL3           | 0       | SW Frequency selection bits. See <i>Table 4</i> .  |
| Bit 2 | –    | SEL2           | 0       |  |
| Bit 1 | –    | SEL1           | 0       |  |
| Bit 0 | –    | SEL0           | 0       |  |

**Byte 1: Control Register 1**

| Bit   | Pin#   | Name                | Default | Description       |
|-------|--------|---------------------|---------|-------------------|
| Bit 7 | 42, 41 | CPUT0, CPUC0        | 1       | (Active/Inactive) |
| Bit 6 | 39, 38 | CPUT_CS,<br>CPUC_CS | 1       | (Active/Inactive) |
| Bit 5 | 6      | 48MHz               | 1       | (Active/Inactive) |
| Bit 4 | 7      | 24_48MHz            | 1       | (Active/Inactive) |
| Bit 3 | –      | Reserved            | 0       | Reserved          |
| Bit 2 | 28     | AGP2                | 1       | (Active/Inactive) |
| Bit 1 | 27     | AGP1                | 1       | (Active/Inactive) |
| Bit 0 | 26     | AGP0                | 1       | (Active/Inactive) |

**Byte 2: Control Register 2**

| Bit   | Pin# | Name | Default | Description       |
|-------|------|------|---------|-------------------|
| Bit 7 | 20   | PCI7 | 1       | (Active/Inactive) |
| Bit 6 | 18   | PCI6 | 1       | (Active/Inactive) |
| Bit 5 | 17   | PCI5 | 1       | (Active/Inactive) |
| Bit 4 | 16   | PCI4 | 1       | (Active/Inactive) |
| Bit 3 | 14   | PCI3 | 1       | (Active/Inactive) |

**Byte 2: Control Register 2 (continued)**

| Bit   | Pin# | Name | Default | Description       |
|-------|------|------|---------|-------------------|
| Bit 2 | 13   | PCI2 | 1       | (Active/Inactive) |
| Bit 1 | 11   | PCI1 | 1       | (Active/Inactive) |
| Bit 0 | 10   | PCI0 | 1       | (Active/Inactive) |

**Byte 3: Control Register**

| Bit   | Pin# | Name     | Default | Description       |
|-------|------|----------|---------|-------------------|
| Bit 7 | 9    | PCI_F    | 1       | (Active/Inactive) |
| Bit 6 | 22   | PCI9_E   | 1       | (Active/Inactive) |
| Bit 5 | —    | Reserved | 0       | Reserved          |
| Bit 4 | 21   | PCI8     | 1       | (Active/Inactive) |
| Bit 3 | 46   | REF2     | 1       | (Active/Inactive) |
| Bit 2 | —    | Reserved | 0       | Reserved          |
| Bit 1 | 47   | REF1     | 1       | (Active/Inactive) |
| Bit 0 | 48   | REF0     | 1       | (Active/Inactive) |

**Byte 4: Watchdog Timer Register**

| Bit   | Pin# | Name          | Default | Description  |
|-------|------|---------------|---------|--|
| Bit 7 | —    | Reserved      | 0       | Reserved   |
| Bit 6 | —    | FS_Override   | 0       | 0 = Select operating frequency by FS[4:0] input pins<br>1 = Select operating frequency by SEL[4:0] settings  |
| Bit 5 | —    | WD_TIMER4     | 1       | These bits store the time-out value of the Watchdog timer. The scale of the timer is determined by the prescaler.  |
| Bit 4 | —    | WD_TIMER3     | 1       |  |
| Bit 3 | —    | WD_TIMER2     | 1       | The timer can support a value of 150 ms to 4.8 sec when the prescaler is set to 150 ms. If the prescaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec. |
| Bit 2 | —    | WD_TIMER1     | 1       |  |
| Bit 1 | —    | WD_TIMER0     | 1       | When the Watchdog timer reaches "0", it will set the WD_TO_STATUS bit.   |
| Bit 0 | —    | WD_PRE_SCALER | 0       | 0 = 150 ms<br>1 = 2.5 sec  |

**Byte 5: Control Register 5**

| Bit   | Pin# | Name              | Default | Description                                       |
|-------|------|-------------------|---------|---|
| Bit 7 | 9    | Latched FS4 input | X       | Latched FS[4:0] inputs. These bits are read-only. |
| Bit 6 | 7    | Latched FS3 input | X       |   |
| Bit 5 | 6    | Latched FS2 input | X       |   |
| Bit 4 | 47   | Latched FS1 input | X       |   |
| Bit 3 | 48   | Latched FS0 input | X       |   |
| Bit 2 | —    | Reserved          | 0       | Reserved  |
| Bit 1 | —    | Reserved          | 0       | Reserved  |
| Bit 0 | —    | SEL4              | 0       | SW Frequency selection bits. See Table 4.         |

**Byte 6: Reserved Register**

| Bit   | Name     | Default | Description |
|-------|----------|---------|-------------|
| Bit 7 | Reserved | 1       | Reserved    |
| Bit 6 | Reserved | 1       | Reserved    |
| Bit 5 | Reserved | 1       | Reserved    |
| Bit 4 | Reserved | 1       | Reserved    |

**Byte 6: Reserved Register (continued)**

| Bit   | Name     | Default | Description |
|-------|----------|---------|-------------|
| Bit 3 | Reserved | 1       | Reserved    |
| Bit 2 | Reserved | 1       | Reserved    |
| Bit 1 | Reserved | 1       | Reserved    |
| Bit 0 | Reserved | 1       | Reserved    |

**Byte 7: Reserved Register**

| Bit   | Name     | Default | Description |
|-------|----------|---------|-------------|
| Bit 7 | Reserved | 1       | Reserved    |
| Bit 6 | Reserved | 1       | Reserved    |
| Bit 5 | Reserved | 1       | Reserved    |
| Bit 4 | Reserved | 1       | Reserved    |
| Bit 3 | Reserved | 1       | Reserved    |
| Bit 2 | Reserved | 1       | Reserved    |
| Bit 1 | Reserved | 1       | Reserved    |
| Bit 0 | Reserved | 1       | Reserved    |

**Byte 8: Vendor ID and Revision ID Register (Read-only)**

| Bit   | Name         | Default | Description   |
|-------|--------------|---------|---|
| Bit 7 | Revision_ID3 | 0       | Revision ID bit[3]                                    |
| Bit 6 | Revision_ID2 | 0       | Revision ID bit[2]                                    |
| Bit 5 | Revision_ID1 | 0       | Revision ID bit[1]                                    |
| Bit 4 | Revision_ID0 | 0       | Revision ID bit[0]                                    |
| Bit 3 | Vendor_ID3   | 1       | Bit[3] of Cypress's Vendor ID. This bit is read-only. |
| Bit 2 | Vendor_ID2   | 0       | Bit[2] of Cypress's Vendor ID. This bit is read-only. |
| Bit 1 | Vendor_ID1   | 0       | Bit[1] of Cypress's Vendor ID. This bit is read-only. |
| Bit 0 | Vendor_ID0   | 0       | Bit[0] of Cypress's Vendor ID. This bit is read-only. |

**Byte 9: System Reset and Watchdog Timer Register**

| Bit   | Name         | Default | Description   |
|-------|--------------|---------|---|
| Bit 7 | Reserved     | 0       | Reserved  |
| Bit 6 | PCI_DRV      | 0       | PCI clock output drive strength<br>0 = Normal<br>1 = High Drive   |
| Bit 5 | Reserved     | 0       | Reserved  |
| Bit 4 | RST_EN_WD    | 0       | This bit will enable the generation of a Reset pulse when a Watchdog timer time-out occurs.<br>0 = Disabled<br>1 = Enabled                      |
| Bit 3 | RST_EN_FC    | 0       | This bit will enable the generation of a Reset pulse after a frequency change occurs.<br>0 = Disabled<br>1 = Enabled                            |
| Bit 2 | WD_TO_STATUS | 0       | Watchdog Timer Time-out Status bit<br>0 = No time-out occurs (READ); Ignore (WRITE)<br>1 = time-out occurred (READ); Clear WD_TO_STATUS (WRITE) |
| Bit 1 | WD_EN        | 0       | 0 = Stop and reload Watchdog timer<br>1 = Enable Watchdog timer. It will start counting down after a frequency change occurs.                   |
| Bit 0 | Reserved     | 0       | Reserved  |

**Byte 10: Skew Control Register**

| Bit   | Name      | Default | Description   |
|-------|-----------|---------|---|
| Bit 7 | CPU_Skew2 | 0       | CPU skew control<br>000 = Normal<br>001 = -150 ps<br>010 = -300 ps<br>011 = -450 ps<br>100 = +150 ps<br>101 = +300 ps<br>110 = +450 ps<br>111 = +600 ps |
| Bit 6 | CPU_Skew1 | 0       |   |
| Bit 5 | CPU_Skew0 | 0       |   |
| Bit 4 | Reserved  | 0       | Reserved  |
| Bit 3 | PCI_Skew1 | 0       | PCI skew control<br>00 = Normal<br>01 = -500 ps<br>10 = Reserved<br>11 = +500 ps  |
| Bit 2 | PCI_Skew0 | 0       |   |
| Bit 1 | AGP_Skew1 | 0       | AGP skew control<br>00 = Normal<br>01 = -150 ps<br>10 = +150 ps<br>11 = +300 ps   |
| Bit 0 | AGP_Skew0 | 0       |   |

**Byte 11: Recovery Frequency N-Value Register**

| Bit   | Name         | Default | Description  |
|-------|--------------|---------|--|
| Bit 7 | ROCV_FREQ_N7 | 0       | If ROCV_FREQ_SEL is set, CY28312B-2 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery CPU output frequency when a Watchdog timer time-out occurs.  |
| Bit 6 | ROCV_FREQ_N6 | 0       |  |
| Bit 5 | ROCV_FREQ_N5 | 0       | The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, CY28312B-2 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28312B-2 will use the frequency ratio stated in the SEL[4:0] register. |
| Bit 4 | ROCV_FREQ_N4 | 0       |  |
| Bit 3 | ROCV_FREQ_N3 | 0       |  |
| Bit 2 | ROCV_FREQ_N2 | 0       | CY28312B-2 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.   |
| Bit 1 | ROCV_FREQ_N1 | 0       | CY28312B-2 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.   |
| Bit 0 | ROCV_FREQ_N0 | 0       |  |

**Byte 12: Recovery Frequency M-Value Register**

| Bit   | Name          | Default | Pin Description  |
|-------|---------------|---------|--|
| Bit 7 | ROCV_FREQ_SEL | 0       | ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.<br>0 = From latched FS[4:0]<br>1 = From the settings of ROCV_FREQ_N[7:0] & ROCV_FREQ_M[6:0] |
| Bit 6 | ROCV_FREQ_M6  | 0       | If ROCV_FREQ_SEL is set, CY28312B-2 will use the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] to determine the recovery CPU output frequency when a Watchdog timer time-out occurs   |
| Bit 5 | ROCV_FREQ_M5  | 0       |  |
| Bit 4 | ROCV_FREQ_M4  | 0       | The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, CY28312B-2 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28312B-2 will use the frequency ratio stated in the SEL[4:0] register.                       |
| Bit 3 | ROCV_FREQ_M3  | 0       |  |
| Bit 2 | ROCV_FREQ_M2  | 0       | CY28312B-2 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.   |
| Bit 1 | ROCV_FREQ_M1  | 0       | CY28312B-2 will change the output frequency whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.   |
| Bit 0 | ROCV_FREQ_M0  | 0       |  |

**Byte 13: Programmable Frequency Select N-Value Register**

| Bit   | Name        | Default | Description  |
|-------|-------------|---------|--|
| Bit 7 | CPU_FSEL_N7 | 0       | If Prog_Freq_EN is set, W300 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated.   |
| Bit 6 | CPU_FSEL_N6 | 0       |  |
| Bit 5 | CPU_FSEL_N5 | 0       |  |
| Bit 4 | CPU_FSEL_N4 | 0       | The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, W312 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28312B-2 will use the frequency ratio stated in the SEL[4:0] register. |
| Bit 3 | CPU_FSEL_N3 | 0       |  |
| Bit 2 | CPU_FSEL_N2 | 0       |  |
| Bit 1 | CPU_FSEL_N1 | 0       | CY28312B-2 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.   |
| Bit 0 | CPU_FSEL_N0 | 0       |  |

**Byte 14: Programmable Frequency Select N-Value Register**

| Bit   | Name        | Default | Description  |
|-------|-------------|---------|--|
| Bit 7 | Pro_Freq_EN | 0       | Programmable output frequencies enabled<br>0 = disabled<br>1 = enabled   |
| Bit 6 | CPU_FSEL_M6 | 0       | If Prog_Freq_EN is set, W300 will use the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] to determine the CPU output frequency. The new frequency will start to load whenever CPU_FSELM[6:0] is updated.   |
| Bit 5 | CPU_FSEL_M5 | 0       |  |
| Bit 4 | CPU_FSEL_M4 | 0       |  |
| Bit 3 | CPU_FSEL_M3 | 0       | The setting of FS_Override bit determines the frequency ratio for CPU, SDRAM, AGP and SDRAM. When it is cleared, CY28312B-2 will use the same frequency ratio stated in the Latched FS[4:0] register. When it is set, CY28312B-2 will use the frequency ratio stated in the SEL[4:0] register. |
| Bit 2 | CPU_FSEL_M2 | 0       |  |
| Bit 1 | CPU_FSEL_M1 | 0       | CY28312B-2 supports programmable CPU frequency ranging from 50 MHz to 248 MHz.   |
| Bit 0 | CPU_FSEL_M0 | 0       |  |

**Byte 15: Reserved Register**

| Bit   | Pin# | Name     | Default | Description              |
|-------|------|----------|---------|--------------------------|
| Bit 7 | –    | Reserved | 0       | Reserved                 |
| Bit 6 | –    | Reserved | 0       | Reserved                 |
| Bit 5 | –    | Reserved | 0       | Reserved                 |
| Bit 4 | –    | Reserved | 0       | Reserved                 |
| Bit 3 | –    | Reserved | 0       | Reserved                 |
| Bit 2 | –    | Reserved | 0       | Reserved                 |
| Bit 1 | –    | Reserved | 1       | Reserved. Write with '1' |
| Bit 0 | –    | Reserved | 1       | Reserved. Write with '1' |

**Byte 16: Reserved Register**

| Bit   | Pin# | Name     | Default | Description |
|-------|------|----------|---------|-------------|
| Bit 7 | –    | Reserved | 0       | Reserved    |
| Bit 6 | –    | Reserved | 0       | Reserved    |
| Bit 5 | –    | Reserved | 0       | Reserved    |
| Bit 4 | –    | Reserved | 0       | Reserved    |
| Bit 3 | –    | Reserved | 0       | Reserved    |
| Bit 2 | –    | Reserved | 0       | Reserved    |
| Bit 1 | –    | Reserved | 0       | Reserved    |

**Byte 17: Reserved Register**

| Bit   | Pin# | Name     | Default | Description |
|-------|------|----------|---------|-------------|
| Bit 7 | –    | Reserved | 0       | Reserved    |
| Bit 6 | –    | Reserved | 0       | Reserved    |
| Bit 5 | –    | Reserved | 0       | Reserved    |
| Bit 4 | –    | Reserved | 0       | Reserved    |
| Bit 3 | –    | Reserved | 0       | Reserved    |
| Bit 2 | –    | Reserved | 0       | Reserved    |
| Bit 1 | –    | Reserved | 0       | Reserved    |

**Table 4. Additional Frequency Selections through Serial Data Interface Data Bytes**

| Input Conditions |      |      |      |      | Output Frequency |          |          | PLL Gear Constants (G) |  |
|------------------|------|------|------|------|------------------|----------|----------|------------------------|--|
| FS4              | FS3  | FS2  | FS1  | FS0  | CPU              | 3V66     | PCI      |                        |  |
| SEL4             | SEL3 | SEL2 | SEL1 | SEL0 |                  |          |          |                        |  |
| 0                | 0    | 0    | 0    | 0    | 156.0            | 78.0     | 39.0     | 48.00741               |  |
| 0                | 0    | 0    | 0    | 1    | 154.0            | 77.0     | 38.5     | 48.00741               |  |
| 0                | 0    | 0    | 1    | 0    | 152.0            | 76.0     | 38.0     | 48.00741               |  |
| 0                | 0    | 0    | 1    | 1    | 147.0            | 73.5     | 36.8     | 48.00741               |  |
| 0                | 0    | 1    | 0    | 0    | 144.0            | 72.0     | 36.0     | 48.00741               |  |
| 0                | 0    | 1    | 0    | 1    | 142.0            | 71.0     | 35.5     | 48.00741               |  |
| 0                | 0    | 1    | 1    | 0    | 138.0            | 69.0     | 34.5     | 48.00741               |  |
| 0                | 0    | 1    | 1    | 1    | 136.0            | 68.0     | 34.0     | 48.00741               |  |
| 0                | 1    | 0    | 0    | 0    | 124.0            | 62.0     | 31.0     | 48.00741               |  |
| 0                | 1    | 0    | 0    | 1    | 122.0            | 61.0     | 30.5     | 48.00741               |  |
| 0                | 1    | 0    | 1    | 0    | 117.0            | 78.0     | 39.0     | 48.00741               |  |
| 0                | 1    | 0    | 1    | 1    | 115.0            | 76.7     | 38.3     | 48.00741               |  |
| 0                | 1    | 1    | 0    | 0    | 113.0            | 75.3     | 37.7     | 48.00741               |  |
| 0                | 1    | 1    | 0    | 1    | 108.0            | 72.0     | 36.0     | 48.00741               |  |
| 0                | 1    | 1    | 1    | 0    | 105.0            | 70.0     | 35.0     | 48.00741               |  |
| 0                | 1    | 1    | 1    | 1    | 102.0            | 68.0     | 34.0     | 48.00741               |  |
| 1                | 0    | 0    | 0    | 0    | Reserved         | Reserved | Reserved | Reserved               |  |
| 1                | 0    | 0    | 0    | 1    | Reserved         | Reserved | Reserved | Reserved               |  |
| 1                | 0    | 0    | 1    | 0    | Reserved         | Reserved | Reserved | Reserved               |  |
| 1                | 0    | 0    | 1    | 1    | 200.0            | 66.6     | 33.3     | 48.00741               |  |
| 1                | 0    | 1    | 0    | 0    | 190.0            | 76.0     | 38.0     | 48.00741               |  |
| 1                | 0    | 1    | 0    | 1    | 180.0            | 72.0     | 36.0     | 48.00741               |  |
| 1                | 0    | 1    | 1    | 0    | 170.0            | 68.0     | 34.0     | 48.00741               |  |
| 1                | 0    | 1    | 1    | 1    | 150.0            | 75.0     | 37.5     | 48.00741               |  |
| 1                | 1    | 0    | 0    | 0    | 140.0            | 70.0     | 35.0     | 48.00741               |  |
| 1                | 1    | 0    | 0    | 1    | 120.0            | 60.0     | 30.0     | 48.00741               |  |
| 1                | 1    | 0    | 1    | 0    | 110.0            | 73.3     | 33.3     | 48.00741               |  |
| 1                | 1    | 0    | 1    | 1    | 66.6             | 66.6     | 33.3     | 48.00741               |  |
| 1                | 1    | 1    | 0    | 0    | 200.0            | 66.6     | 33.3     | 48.00741               |  |
| 1                | 1    | 1    | 0    | 1    | 166.6            | 66.6     | 33.3     | 48.00741               |  |
| 1                | 1    | 1    | 1    | 0    | 100.0            | 66.6     | 33.3     | 48.00741               |  |
| 1                | 1    | 1    | 1    | 1    | 133.3            | 66.6     | 33.3     | 48.00741               |  |

## Programmable Output Frequency, Watchdog Timer and Recovery Output Frequency Functional Description

The Programmable Output Frequency feature allows users to generate any CPU output frequency from the range of 50 MHz to 248 MHz. Cypress offers the most dynamic and the simplest programming interface for system developers to utilize this feature in their platforms.

The Watchdog Timer and Recovery Output Frequency features allow users to implement a recovery mechanism when the system hangs or getting unstable. System BIOS or other control software can enable the Watchdog timer before they attempt to make a frequency change. If the system hangs and a Watchdog timer time-out occurs, a system reset will be generated and a recovery frequency will be activated.

All of the related registers are summarized in *Table 6*.

**Table 5. Register Summary**

| Name                               | Description   |
|------------------------------------|---|
| Pro_Freq_EN                        | Programmable output frequencies enabled<br>0 = Disabled (default)<br>1 = Enabled<br><br>When it is disabled, the operating output frequency will be determined by either the latched value of FS[4:0] inputs or the programmed value of SEL[4:0]. If FS_Override bit is clear, latched FS[4:0] inputs will be used. If FS_Override bit is set, programmed value of SEL[4:0] will be used.<br><br>When it is enabled, the CPU output frequency will be determined by the programmed value of CPUFSEL_N, CPUFSEL_M and the PLL Gear Constant. The program value of FS_Override, SEL[4:0] or the latched value of FS[4:0] will determine the PLL Gear Constant and the frequency ratio between CPU and other frequency outputs   |
| FS_Override                        | When Pro_Freq_EN is cleared or disabled,<br>0 = Select operating frequency by FS input pins (default)<br>1 = Select operating frequency by SEL bits in SMBus control bytes<br><br>When Pro_Freq_EN is set or enabled,<br>0 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the latched value of FS input pins (default)<br>1 = Frequency output ratio between CPU and other frequency groups and the PLL Gear Constant are based on the programmed value of SEL bits in SMBus control bytes  |
| CPU_FSEL_N, CPU_FSEL_M             | When Prog_Freq_EN is set or enabled, the values programmed in CPU_FSEL_N[7:0] and CPU_FSEL_M[6:0] determines the CPU output frequency. The new frequency will start to load whenever there is an update to either CPU_FSEL_N[7:0] or CPU_FSEL_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation.<br><br>The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PIC. When FS_Override is cleared or disabled, the frequency ratio follows the latched value of the FS input pins. When FS_Override is set or enabled, the frequency ratio follows the programmed value of SEL bits in SMBus control bytes.                  |
| ROCV_FREQ_SEL                      | ROCV_FREQ_SEL determines the source of the recover frequency when a Watchdog timer time-out occurs. The clock generator will automatically switch to the recovery CPU frequency based on the selection on ROCV_FREQ_SEL.<br>0 = From latched FS[4:0]<br>1 = From the settings of ROCV_FREQ_N[7:0] & ROCV_FREQ_M[6:0]  |
| ROCV_FREQ_N[7:0], ROCV_FREQ_M[6:0] | When ROCV_FREQ_SEL is set, the values programmed in ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0] will be used to determine the recovery CPU output frequency when a Watchdog timer time-out occurs.<br><br>The setting of FS_Override bit determines the frequency ratio for CPU, AGP and PIC. When it is cleared, the same frequency ratio stated in the Latched FS[4:0] register will be used.<br>When it is set, the frequency ratio stated in the SEL[4:0] register will be used.<br><br>The new frequency will start to load whenever there is an update to either ROCV_FREQ_N[7:0] and ROCV_FREQ_M[6:0]. Therefore, it is recommended to use Word or Block write to update both registers within the same SMBus bus operation. |
| WD_EN                              | 0 = Stop and reload Watchdog timer<br>1 = Enable Watchdog timer. It will start counting down after a frequency change occurs.   |
| WD_TO_STATUS                       | Watchdog Timer Time-out Status bit<br>0 = No time-out occurs (READ); Ignore (WRITE)<br>1 = time-out occurred (READ); Clear WD_TO_STATUS (WRITE)   |

**Table 5. Register Summary** (continued)

| Name          | Description   |
|---------------|---|
| WD_TIMER[4:0] | These bits store the time-out value of the Watchdog timer. The scale of the timer is determined by the prescaler.<br>The timer can support a value of 150 ms to 4.8 sec when the pre-scaler is set to 150 ms. If the pre-scaler is set to 2.5 sec, it can support a value from 2.5 sec to 80 sec.<br>When the Watchdog timer reaches "0", it will set the WD_TO_STATUS bit. |
| WD_PRE_SCALER | 0 = 150 ms<br>1 = 2.5 sec   |
| RST_EN_WD     | This bit will enable the generation of a Reset pulse when a Watchdog timer time-out occurs.<br>0 = Disabled<br>1 = Enabled  |
| RST_EN_FC     | This bit will enable the generation of a Reset pulse after a frequency change occurs.<br>0 = Disabled<br>1 = Enabled  |

### How to Program CPU Output Frequency

When the programmable output frequency feature is enabled (Pro\_Freq\_EN bit is set), the CPU output frequency is determined by the following equation:

$$F_{cpu} = G * (N + 3)/(M + 3)$$

"N" and "M" are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

"G" stands for the PLL Gear Constant, which is determined by the programmed value of FS[4:0] or SEL[4:0]. The value is listed in *Table 4*. The ratio of (N + 3) and (M + 3) needs to be greater than "1"  $[(N + 3)/(M + 3) > 1]$ .

*Table 6* lists set of N and M values for different frequency output ranges. This example use a fixed value for the M-Value Register and select the CPU output frequency by changing the value of the N-Value Register.

**Table 6. Examples of N and M Value for Different CPU Frequency Range**

| Frequency Ranges | Gear Constants | Fixed Value for M-Value Register | Range of N-Value Register for Different CPU Frequency |
|------------------|----------------|----------------------------------|---|
| 50 MHz–129 MHz   | 48.00741       | 93                               | 97–255  |
| 130 MHz–248 MHz  | 48.00741       | 48                               | 127–245   |

**Absolute Maximum Conditions<sup>[2]</sup>**

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter           | Description                            | Rating       | Unit |
|---------------------|--|--------------|------|
| $V_{DD}, V_{IN}$    | Voltage on any pin with respect to GND | -0.5 to +7.0 | V    |
| $T_{STG}$           | Storage temperature                    | -65 to +150  | °C   |
| $T_B$               | Ambient temperature under bias         | -55 to +125  | °C   |
| $T_A$               | Operating temperature                  | 0 to +70     | °C   |
| ESD <sub>PROT</sub> | Input ESD protection                   | 2 (min.)     | kV   |

**DC Electrical Characteristics**  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 5\%$  and  $2.5\text{V} \pm 5\%$ 

| Parameter                         | Description  |                                      | Test Condition                                  | Min.      | Typ. | Max.           | Unit |
|-----------------------------------|--|--------------------------------------|---|-----------|------|----------------|------|
| <b>Supply Current</b>             |  |                                      |   |           |      |                |      |
| $I_{DD}$                          | 3.3V Supply Current  |                                      | CPU =100 MHz<br>Outputs Loaded <sup>[3]</sup>   |           | 260  |                | mA   |
| $I_{DD}$                          | 2.5V Supply Current  |                                      | CPUCS =100 MHz<br>Outputs Loaded <sup>[3]</sup> |           | 25   |                | mA   |
| <b>Logic Inputs</b>               |  |                                      |   |           |      |                |      |
| $V_{IL}$                          | Input Low Voltage  |                                      |   | GND - 0.3 |      | 0.8            | V    |
| $V_{IH}$                          | Input High Voltage   |                                      |   | 2.0       |      | $V_{DD} + 0.3$ | V    |
| $I_{IL}$                          | Input Low Current  |                                      |   |           |      | -25            | μA   |
| $I_{IH}$                          | Input High Current   |                                      |   |           |      | 10             | μA   |
| <b>Clock Outputs</b>              |  |                                      |   |           |      |                |      |
| $V_{OL}$                          | Output Low Voltage   |                                      | $I_{OL} = 1\text{ mA}$                          |           |      | 50             | mV   |
| $V_{OH}$                          | Output High Voltage  |                                      | $I_{OH} = -1\text{ mA}$                         | 3.1       |      |                | V    |
| $V_{OL}$                          | Output Low Voltage   | CPUT_CS,<br>CPUC_CS,<br>CPUTO, CPUC0 | Termination to V pull-up<br>(external)          | 0         |      | 0.3            | V    |
| $V_{OH}$                          | Output High Voltage  | CPUT_CS,<br>CPUC_CS,<br>CPUTO, CPUC0 | Termination to V pull-up<br>(external)          | 1.0       |      | 1.2            | V    |
| $I_{OL}$                          | Output Low Current   | PCI, AGP                             | $V_{OL} = 1.5\text{V}$                          | 70        | 110  | 135            | mA   |
|                                   |  | REF                                  | $V_{OL} = 1.5\text{V}$                          | 50        | 70   | 100            | mA   |
|                                   |  | 48 MHz                               | $V_{OL} = 1.5\text{V}$                          | 50        | 70   | 100            | mA   |
|                                   |  | 24_48 MHz                            | $V_{OL} = 1.5\text{V}$                          | 50        | 70   | 100            | mA   |
| $I_{OH}$                          | Output High Current  | PCI, AGP                             | $V_{OH} = 1.5\text{V}$                          | 70        | 110  | 135            | mA   |
|                                   |  | REF                                  | $V_{OH} = 1.5\text{V}$                          | 50        | 70   | 100            | mA   |
|                                   |  | 48 MHz                               | $V_{OH} = 1.5\text{V}$                          | 50        | 70   | 100            | mA   |
|                                   |  | 24_48 MHz                            | $V_{OH} = 1.5\text{V}$                          | 50        | 70   | 100            | mA   |
| <b>Crystal Oscillator</b>         |  |                                      |   |           |      |                |      |
| $V_{TH}$                          | X1 Input Threshold Voltage                                   |                                      | $V_{DD} = 3.3\text{V}$                          |           | 1.65 |                | V    |
| $C_{LOAD}$                        | Load Capacitance, Imposed on External Crystal <sup>[4]</sup> |                                      |   |           | 18   |                | pF   |
| <b>Pin Capacitance/Inductance</b> |  |                                      |   |           |      |                |      |
| $C_{IN}$                          | Input Pin Capacitance <sup>[5]</sup>                         |                                      | Except X1 and X2                                |           |      | 5              | pF   |

**Notes:**

2. Multiple Supplies: the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. All clock outputs loaded with 6" 600Ω transmission lines with 20-pF capacitors.
4. The CY28312B-2 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 18 pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

**DC Electrical Characteristics**  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 3.3\text{V} \pm 5\%$  and  $2.5\text{V} \pm 5\%$  (continued)

| Parameter | Description            | Test Condition | Min. | Typ. | Max. | Unit |
|-----------|------------------------|----------------|------|------|------|------|
| $C_{OUT}$ | Output Pin Capacitance |                |      |      | 6    | pF   |
| $L_{IN}$  | Input Pin Inductance   |                |      |      | 7    | nH   |

**AC Electrical Characteristics**
 $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DDQ3} = 3.3\text{V} \pm 5\%$ ,  $f_{XTL} = 14.31818\text{ MHz}$ 

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum is disabled.

**CPU Clock Outputs (CPU0, CPUC0, CPU\_CS)<sup>[6]</sup>**

| Parameter | Description  | Test Condition/Comments   | CPU = 100 MHz |      |      | CPU = 133 MHz |      |      | Unit |
|-----------|--|---|---------------|------|------|---------------|------|------|------|
|           |  |   | Min.          | Typ. | Max. | Min.          | Typ. | Max. |      |
| $t_R$     | Output Rise Edge Rate                              | CPU_CS  | 1.0           |      | 4.0  | 1.0           |      | 4.0  | V/ns |
| $t_F$     | Output Fall Edge Rate                              | CPU_CS  | 1.0           |      | 4.0  | 1.0           |      | 4.0  | V/ns |
| $t_D$     | Duty Cycle   | Measured at 50% point   | 45            |      | 55   | 45            |      | 55   | %    |
| $t_{JC}$  | Jitter, Cycle to Cycle                             |   |               | 250  |      |               | 250  |      | ps   |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |               | 3    |      |               | 3    |      | ms   |
| $Z_o$     | AC Output Impedance                                | $V_O = V_X$   |               | 50   |      |               | 50   |      | W    |

**PCI Clock Outputs (Lump Capacitance Test Load = 30 pF)**

| Parameter | Description  | Test Condition/Comments   | Min. | Typ. | Max. | Unit     |
|-----------|--|---|------|------|------|----------|
| $t_P$     | Period   | Measured on rising edge at 1.5V   | 30   |      |      | ns       |
| $t_H$     | High Time  | Duration of clock cycle above 2.4V  | 12   |      |      | ns       |
| $t_L$     | Low Time   | Duration of clock cycle below 0.4V  | 12   |      |      | ns       |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.8V to 2.0V  | 1    |      | 4    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.0V to 0.8V  | 1    |      | 4    | V/ns     |
| $t_D$     | Duty Cycle   | Measured on rising and falling edge at 1.5V   | 45   |      | 55   | %        |
| $t_{JC}$  | Jitter, Cycle-to-Cycle                             | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.                      |      |      | 250  | ps       |
| $t_{SK}$  | Output Skew  | Measured on rising edge at 1.5V   |      |      | 500  | ps       |
| $t_0$     | CPU to PCI Clock Skew                              | Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.                                  | 1.5  |      | 4    | ns       |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |      | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 30   |      | $\Omega$ |

**AGP Clock Outputs (Lump Capacitance Test Load = 30 pF)**

| Parameter | Description            | Test Condition/Comments  | Min. | Typ. | Max. | Unit |
|-----------|------------------------|--|------|------|------|------|
| $t_R$     | Output Rise Edge Rate  | Measured from 0.8V to 2.0V   | 0.5  |      | 2.0  | V/ns |
| $t_F$     | Output Fall Edge Rate  | Measured from 2.0V to 0.8V   | 0.5  |      | 2.0  | V/ns |
| $t_D$     | Duty Cycle             | Measured at 1.5V   | 45   |      | 55   | %    |
| $t_{JC}$  | Jitter, Cycle-to-Cycle | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles. |      |      | 250  | ps   |

**Note:**

6. Refer to Figure 1 for K7 operation clock driver test circuit.

**AGP Clock Outputs (Lump Capacitance Test Load = 30 pF) (continued)**

| Parameter | Description  | Test Condition/Comments   | Min. | Typ. | Max. | Unit     |
|-----------|--|---|------|------|------|----------|
| $t_{SK}$  | Output Skew  | Measured on rising edge at 1.5V   |      |      | 300  | ps       |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |      | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 30   |      | $\Omega$ |

**REF Clock Outputs (Lump Capacitance Test Load = 20 pF)**

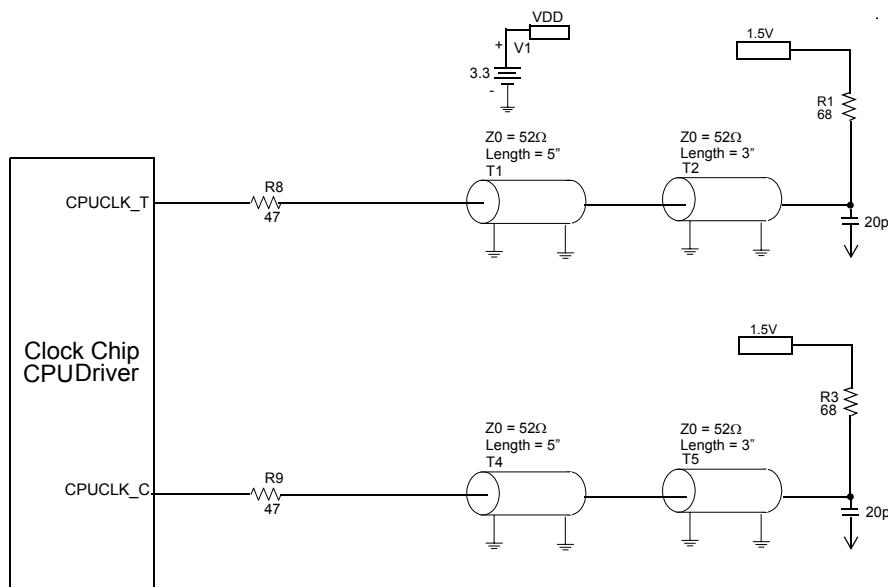
| Parameter | Description  | Test Condition/Comments   | Min. | Typ.   | Max. | Unit     |
|-----------|--|---|------|--------|------|----------|
| $f$       | Frequency, Actual                                  | Frequency generated by crystal oscillator   |      | 14.318 |      | MHz      |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.8V to 2.0V  | 0.5  |        | 2    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.0V to 0.8V  | 0.5  |        | 2    | V/ns     |
| $t_D$     | Duty Cycle   | Measured on rising and falling edge at 1.5V   | 45   |        | 55   | %        |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |        | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 40     |      | $\Omega$ |

**48-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

| Parameter | Description  | Test Condition/Comments   | Min. | Typ.   | Max. | Unit     |
|-----------|--|---|------|--------|------|----------|
| $f$       | Frequency, Actual                                  | Determined by PLL divider ratio (see m/n below)   |      | 48.008 |      | MHz      |
| $f_D$     | Deviation from 48 MHz                              | $(48.008 - 48)/48$  |      | +167   |      | ppm      |
| m/n       | PLL Ratio  | $(14.31818 \text{ MHz} \times 57/17 = 48.008 \text{ MHz})$  |      | 57/17  |      |          |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.8V to 2.0V  | 0.5  |        | 2    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.0V to 0.8V  | 0.5  |        | 2    | V/ns     |
| $t_D$     | Duty Cycle   | Measured on rising and falling edge at 1.5V   | 45   |        | 55   | %        |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |        | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 40     |      | $\Omega$ |

**24-MHz Clock Output (Lump Capacitance Test Load = 20 pF)**

| Parameter | Description  | Test Condition/Comments   | Min. | Typ.   | Max. | Unit     |
|-----------|--|---|------|--------|------|----------|
| $f$       | Frequency, Actual                                  | Determined by PLL divider ratio (see m/n below)   |      | 24.004 |      | MHz      |
| $f_D$     | Deviation from 24 MHz                              | $(24.004 - 24)/24$  |      | +167   |      | ppm      |
| m/n       | PLL Ratio  | $(14.31818 \text{ MHz} \times 57/34 = 24.004 \text{ MHz})$  |      | 57/34  |      |          |
| $t_R$     | Output Rise Edge Rate                              | Measured from 0.8V to 2.0V  | 0.5  |        | 2    | V/ns     |
| $t_F$     | Output Fall Edge Rate                              | Measured from 2.0V to 0.8V  | 0.5  |        | 2    | V/ns     |
| $t_D$     | Duty Cycle   | Measured on rising and falling edge at 1.5V   | 45   |        | 55   | %        |
| $f_{ST}$  | Frequency Stabilization from Power-up (cold start) | Assumes full supply voltage reached within 1 ms from power-up. Short cycles exist prior to frequency stabilization. |      |        | 3    | ms       |
| $Z_o$     | AC Output Impedance                                | Average value during switching transition. Used for determining series termination value.                           |      | 40     |      | $\Omega$ |



**Figure 1. K7 Open Drain Clock Driver Test Circuit**

## Ordering Information

| Ordering Code | Package Type              | Product Flow            |
|---------------|---------------------------|-------------------------|
| CY28312B-2    | 48-pin SSOP               | Commercial, 0°C to 70°C |
| CY28312B-2T   | 48-pin SSOP-Tape and Reel | Commercial, 0°C to 70°C |

## Package Drawing and Dimension

### 48-Lead Shrunk Small Outline Package O48

51-85061-\*C

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**Document History Page**

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| <b>REV.</b> | <b>ECN NO.</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b> |
|-------------|----------------|-------------------|------------------------|------------------------------|
| **          | 130574         | 12/04/03          | RGL                    | New Data Sheet               |