

# SN54HCT573, SN74HCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS176E – MARCH 1984 – REVISED JULY 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- High-Current 3-State Outputs Drive Bus Lines Directly or Up To 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 21$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible
- Bus-Structured Pinout

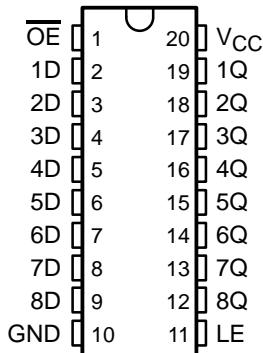
## description/ordering information

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The 'HCT573 devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

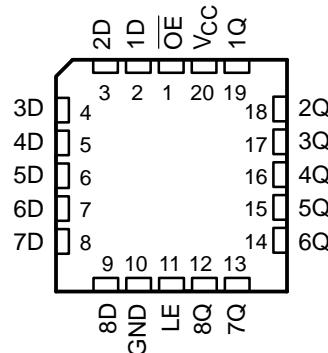
While the latch-enable (LE) input is high, the Q outputs respond to the data (D) inputs. When LE is low, the outputs are latched to retain the data that was set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

SN54HCT573 . . . J OR W PACKAGE  
SN74HCT573 . . . DB, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54HCT573 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74HCT573N	SN74HCT573N
	SOIC – DW	Tube	SN74HCT573DW	HCT573
		Tape and reel	SN74HCT573DWR	
	SOP – NS	Tape and reel	SN74HCT573NSR	HCT573
	SSOP – DB	Tape and reel	SN74HCT573DBR	HT573
	TSSOP – PW	Tube	SN74HCT573PW	HT573
		Tape and reel	SN74HCT573PWR	
-55°C to 125°C	CDIP – J	Tube	SNJ54HCT573J	SNJ54HCT573J
	CFP – W	Tube	SNJ54HCT573W	SNJ54HCT573W
	LCCC – FK	Tube	SNJ54HCT573FK	SNJ54HCT573FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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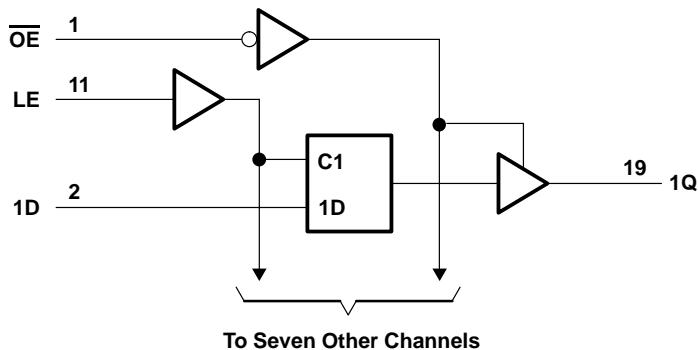
**description/ordering information (continued)**

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

## FUNCTION TABLE (each latch)

INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

## logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

NOTE: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are exceeded.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

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**recommended operating conditions (see Note 3)**

		SN54HCT573			SN74HCT573			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		2	2		V	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		0.8	0.8		V	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V <sub>CC</sub>	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V <sub>CC</sub>	V	
Δt/ΔV	Input transition rise/fall time	500		500	500		ns	
T <sub>A</sub>	Operating free-air temperature	−55	125	−40	85	85	°C	

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT573		SN74HCT573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	4.4	4.499		4.4		4.4		V
			3.98	4.3		3.7		3.84		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	0.001	0.1		0.1		0.1		V
			0.17	0.26		0.4		0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	5.5 V	±0.1	±100		±1000		±1000		nA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0	5.5 V	±0.01	±0.5		±10		±5		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	5.5 V		8		160		80		μA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>	5.5 V	1.4	2.4		3		2.9		mA
C <sub>i</sub>		4.5 V to 5.5 V	3	10		10		10		pF

<sup>†</sup>This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted)**

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HCT573		SN74HCT573		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	4.5 V	20		30		25		ns
		5.5 V	17		27		23		
t <sub>su</sub>	Setup time, data before LE↓	4.5 V	10		15		13		ns
		5.5 V	9		14		12		
t <sub>h</sub>	Hold time, data after LE↓	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

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**SN54HCT573, SN74HCT573  
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WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT573		SN74HCT573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	4.5 V	25	35		53		44		ns
			5.5 V	21	32		48		40		
	LE	Any Q	4.5 V	28	35		53		44		
			5.5 V	25	32		48		40		
t <sub>en</sub>	OE	Any Q	4.5 V	26	35		53		44		ns
			5.5 V	23	32		48		40		
t <sub>dis</sub>	OE	Any Q	4.5 V	23	35		53		44		ns
			5.5 V	22	32		48		40		
t <sub>t</sub>		Any Q	4.5 V	9	12		18		15		ns
			5.5 V	9	11		16		14		

**switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT573		SN74HCT573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	D	Q	4.5 V	32	52		79		65		ns
			5.5 V	27	47		71		59		
	LE	Any Q	4.5 V	38	52		79		65		
			5.5 V	36	47		71		59		
t <sub>en</sub>	OE	Any Q	4.5 V	33	52		79		65		ns
			5.5 V	28	47		71		59		
t <sub>t</sub>		Any Q	4.5 V	18	42		63		53		ns
			5.5 V	16	38		57		48		

**operating characteristics, T<sub>A</sub> = 25°C**

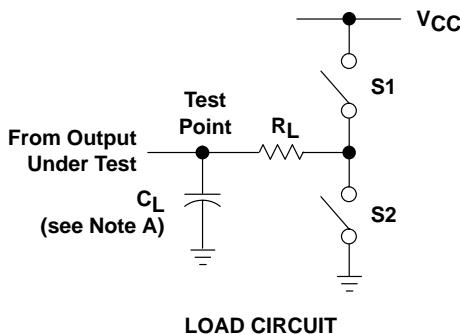
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per latch	No load	50	pF

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

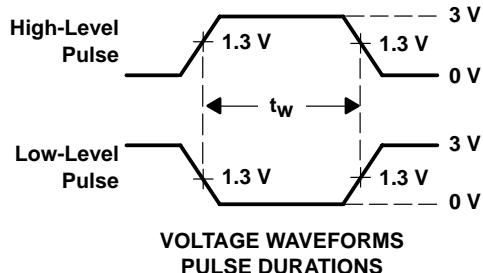


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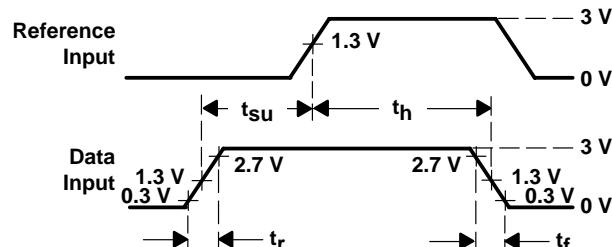
PARAMETER MEASUREMENT INFORMATION



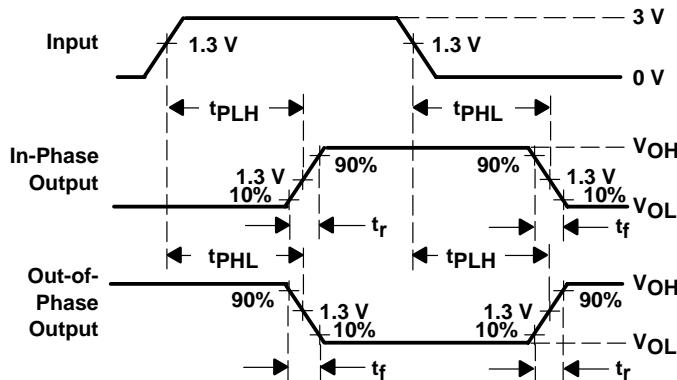
PARAMETER	R <sub>L</sub>	C <sub>L</sub>	S1	S2
t <sub>en</sub>	tpZH tpZL	1 kΩ 150 pF	50 pF or 150 pF	Open Closed
			Closed	Open
t <sub>dis</sub>	tpHZ tpLZ	1 kΩ	50 pF	Open Closed
			Closed	Open
t <sub>pd</sub> or t <sub>t</sub>		—	50 pF or 150 pF	Open Open



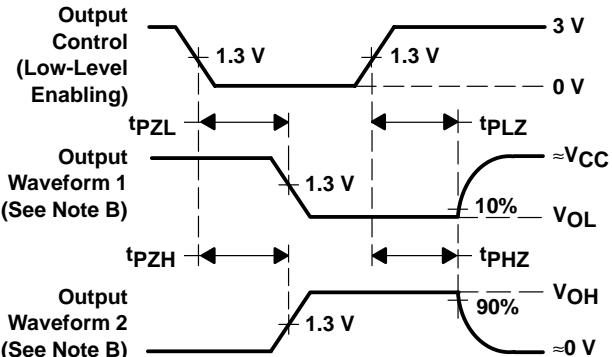
VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C<sub>L</sub> includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> = 6 ns, t<sub>f</sub> = 6 ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.  
 F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.  
 G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74HCT573DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HCT573N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
SN74HCT573NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HCT573PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

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temperature.

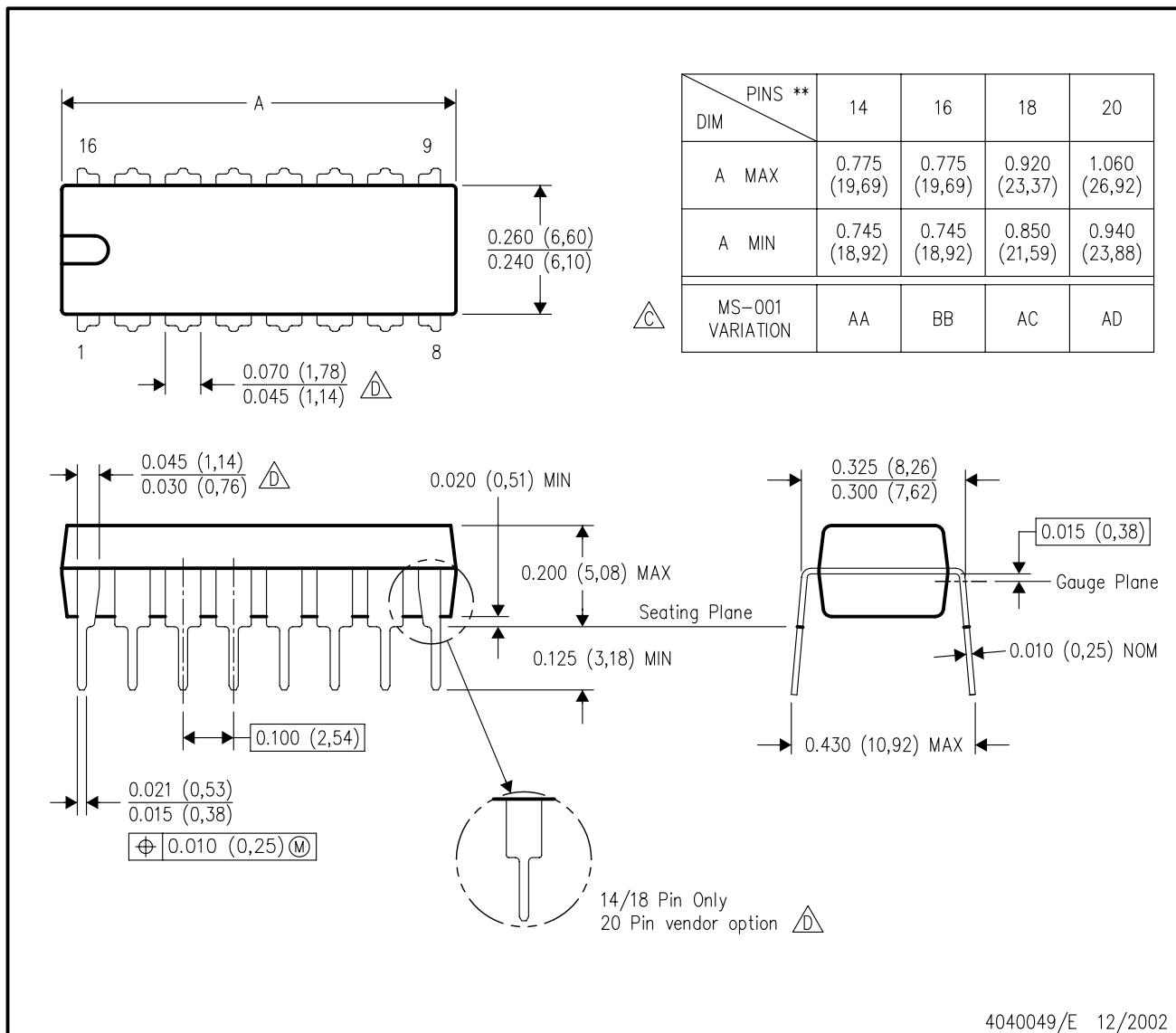
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## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

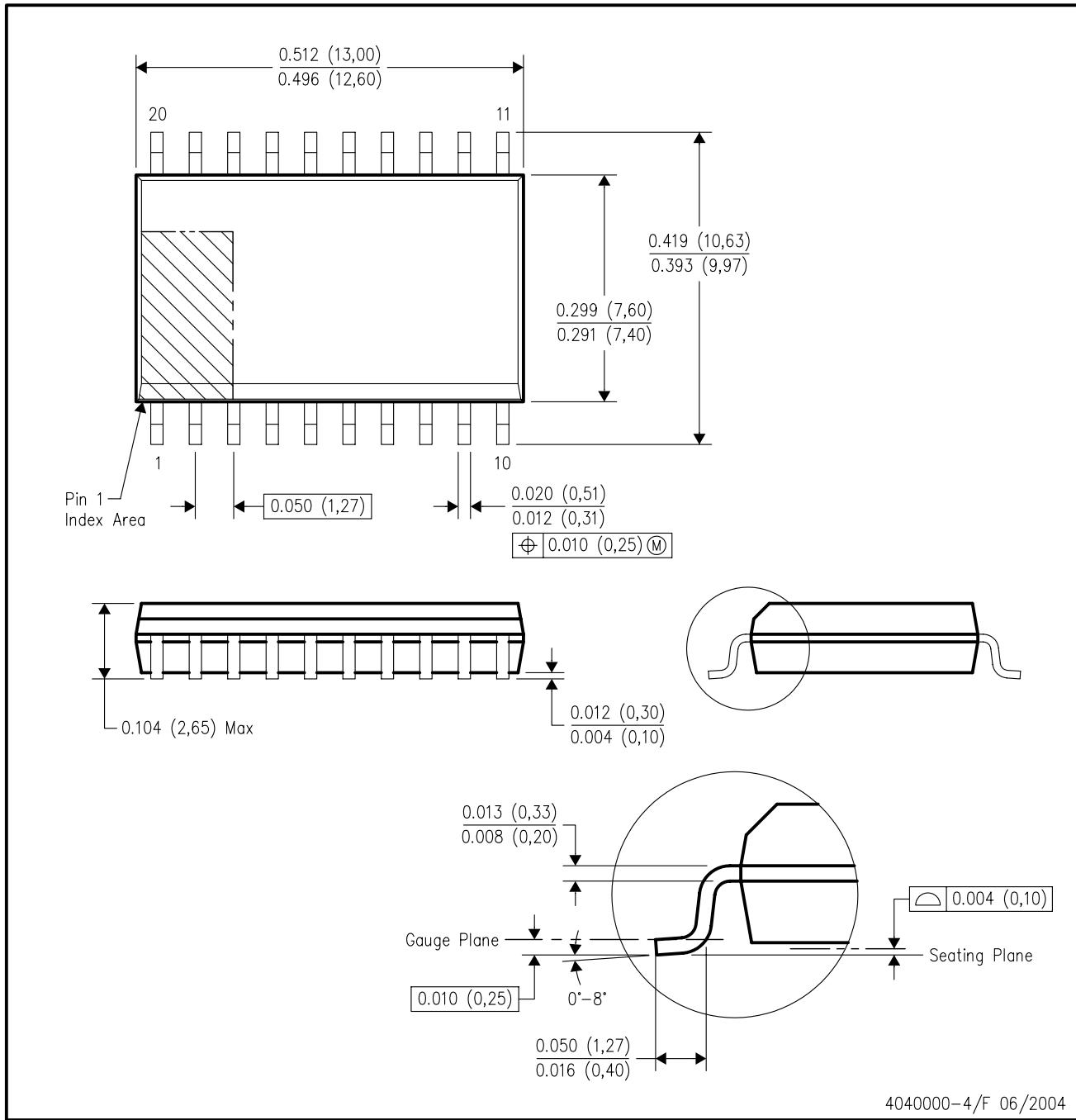
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

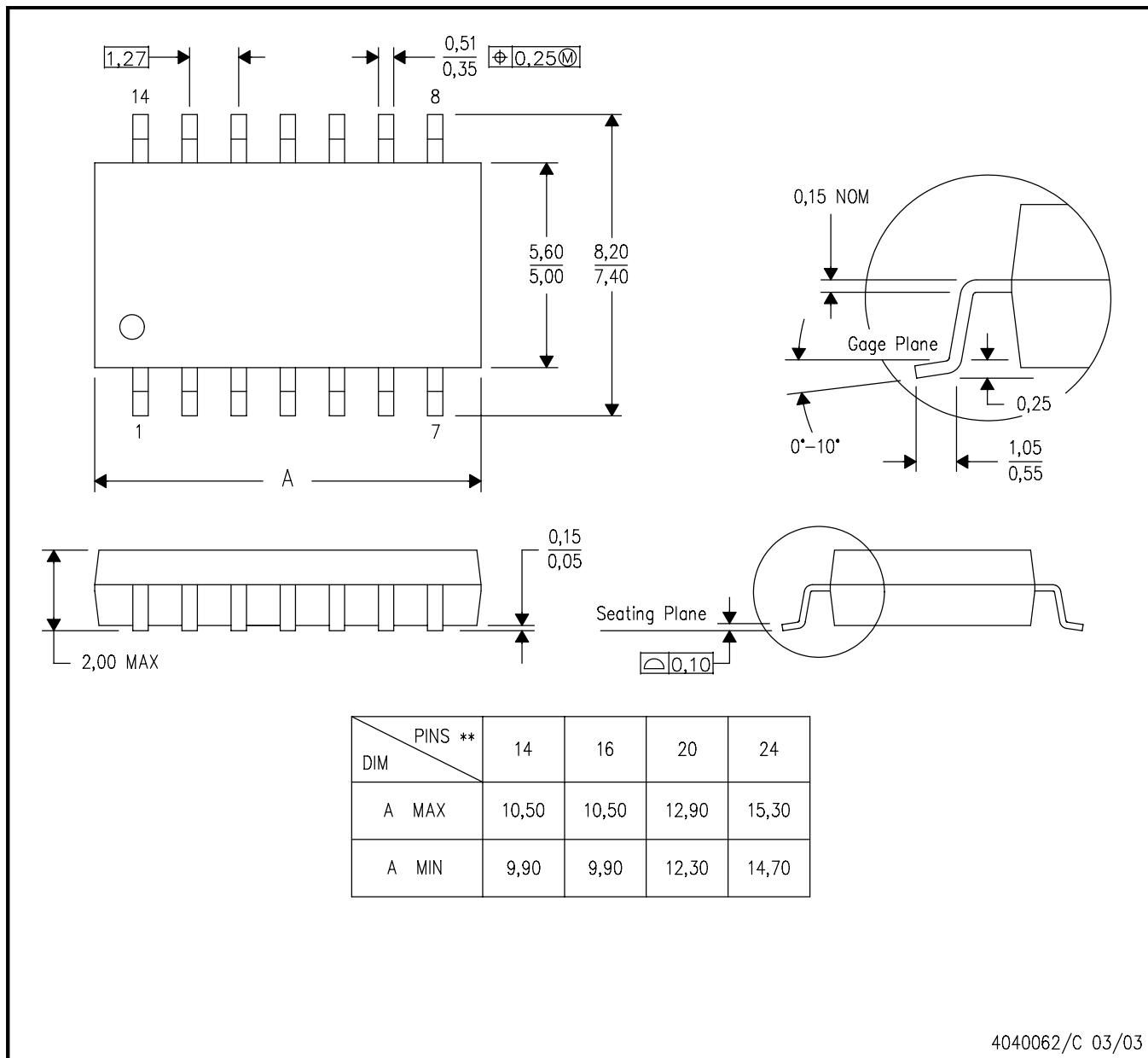
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-013 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



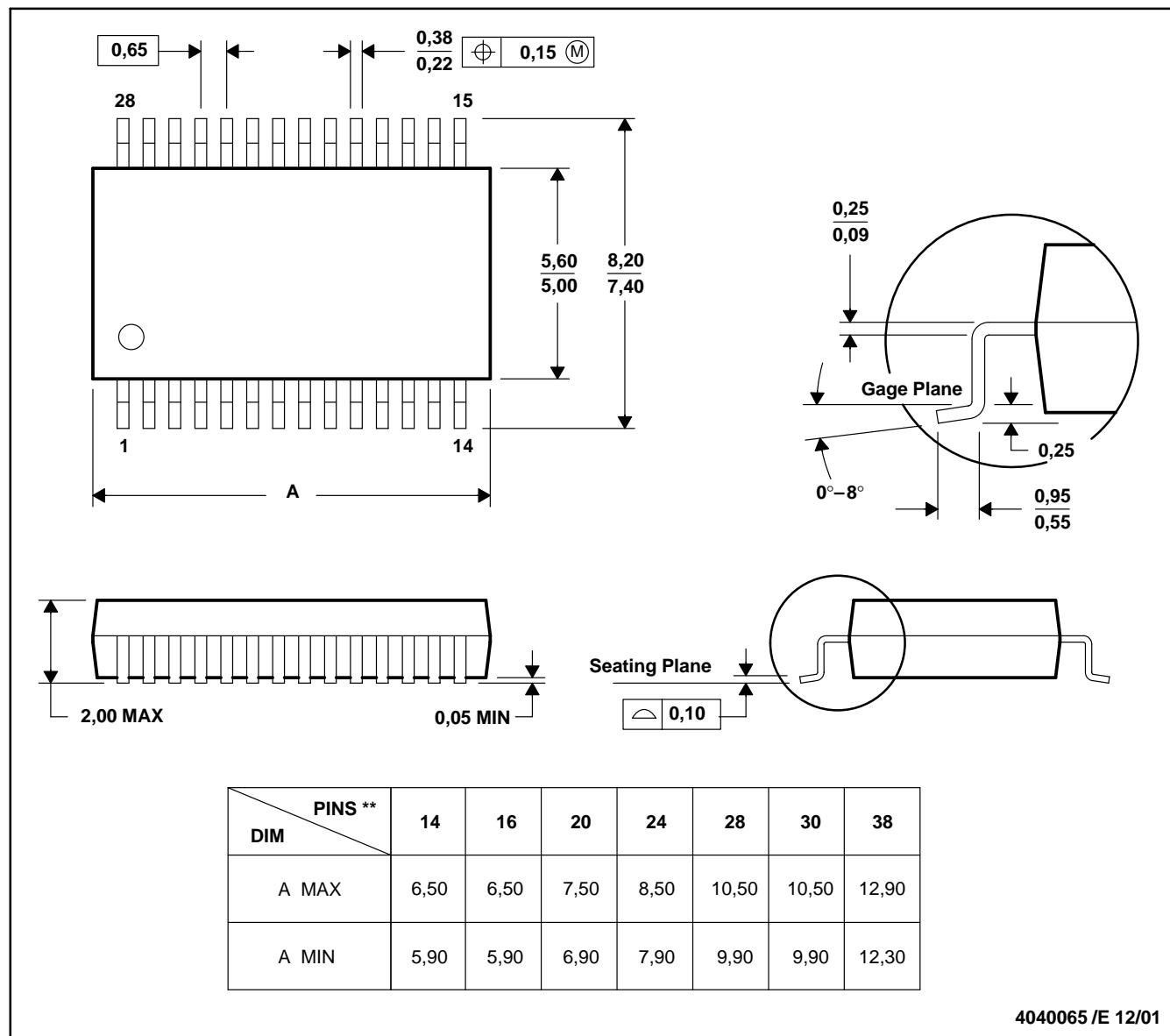
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN

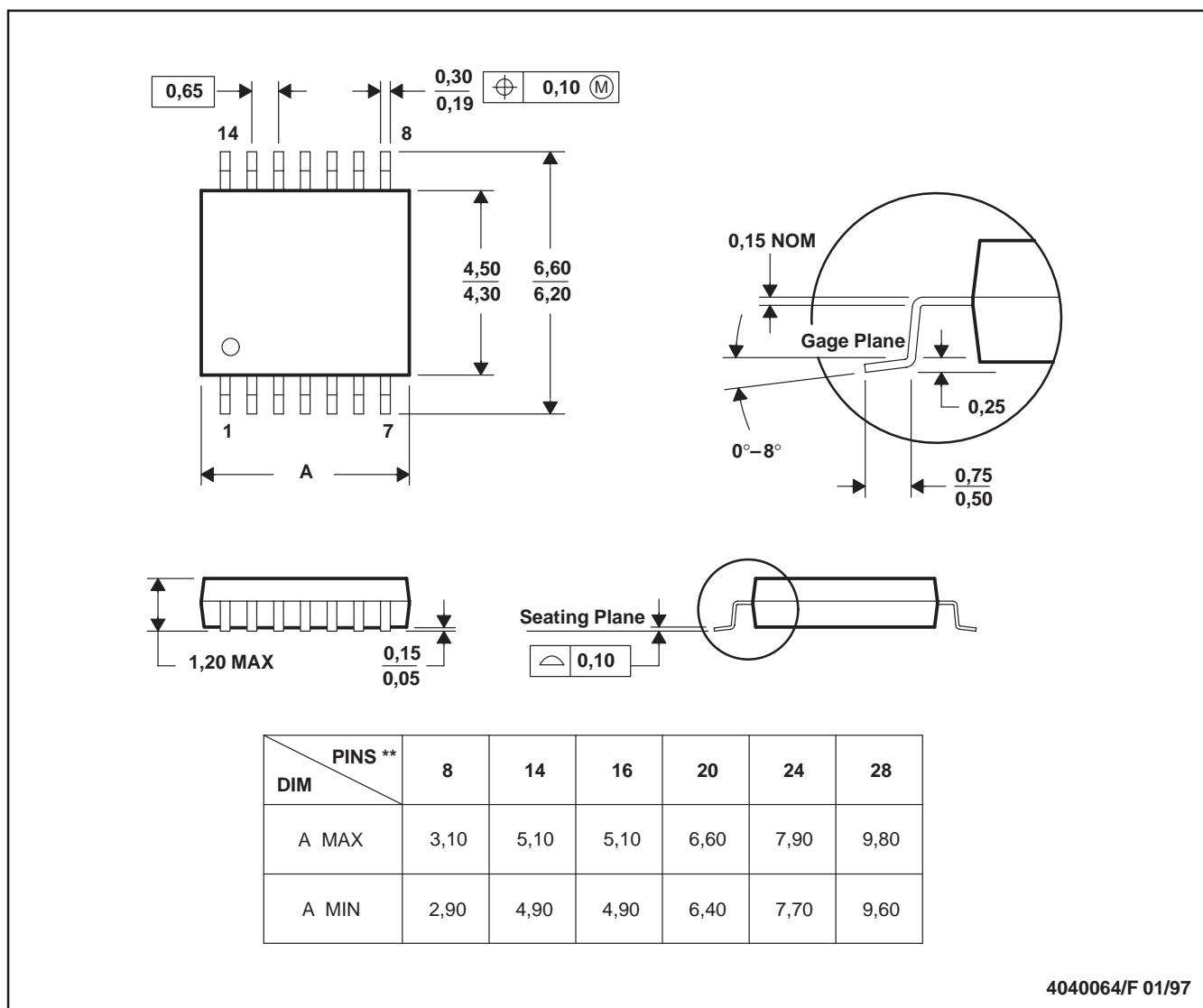


NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- Falls within JEDEC MO-153

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