

Stepping motor driver

BA6343

The BA6343 is a driver designed to drive the stepping motors used in printers and fax machines.

● Applications

Printers and facsimiles

● Features

- 1) Micro-step drive compatible.
- 2) Overheating protection circuit on chip.
- 3) Wide operating voltage range (7V to 33V).

● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage 1	V _M	V _{cc5} ~36	V
Power supply voltage 2	V _{cc5}	-0.01~+7	V
Analog input voltage	V _{analog}	-0.03~+7	V
Logic input voltage	V _{logic}	-0.03~+7	V
Power dissipation	P _d	1700*1	mW
Thermal derating	K _θ	13.6	mW / °C
Junction temperature	T _j	150	°C
Operating temperature	T _{opr}	0~75	°C
Storage temperature	T _{stg}	-55~+150	°C
Allowable output current	I _{out}	±500*2	mA

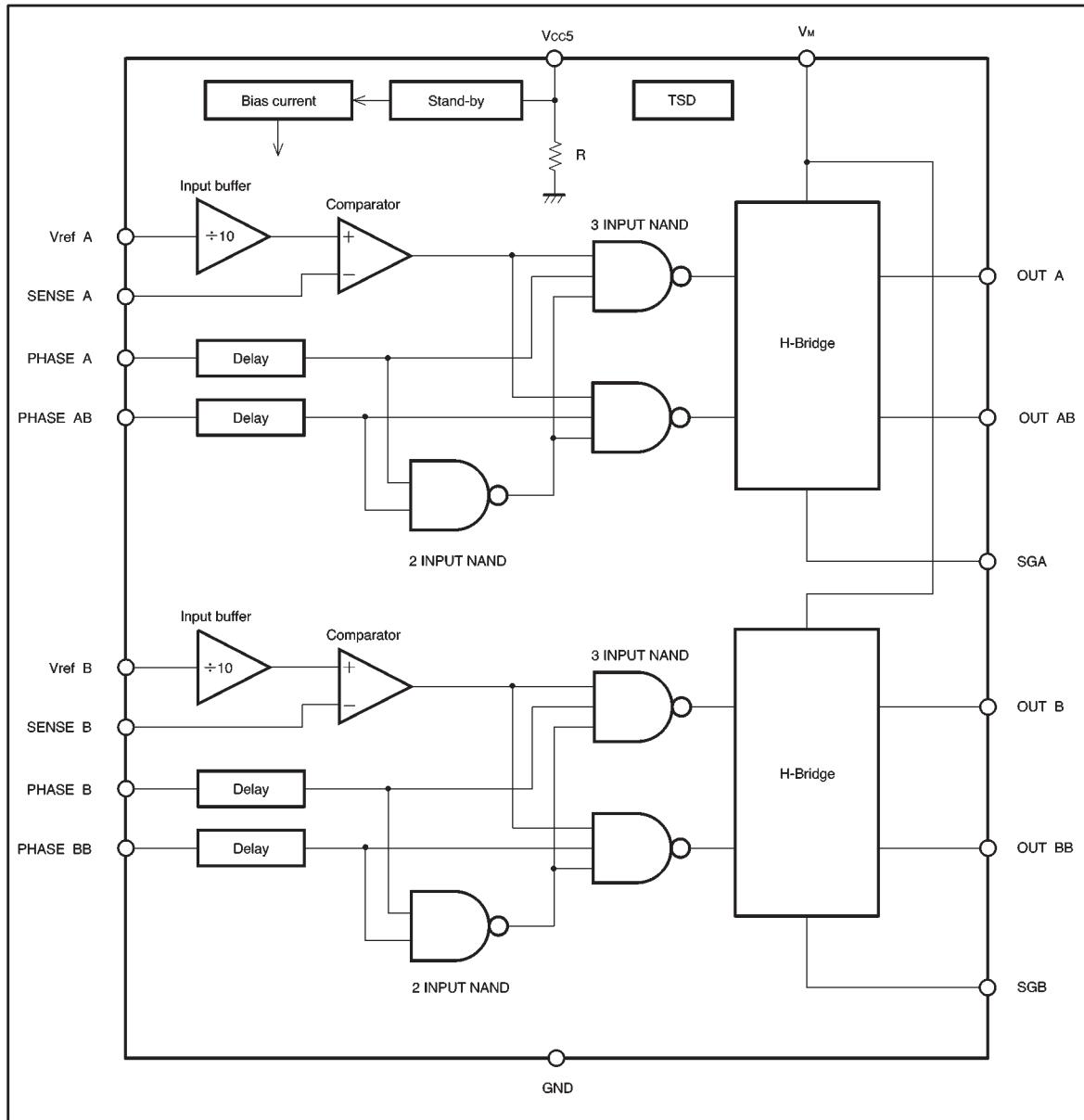
*1 Reduced by 13.6mW for each increase in Ta of 1°C over 25°C
(when mounted on a 70mm × 70mm × 1.6mm glass epoxy board).

*2 Should not exceed P_d or ASO values.

● Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage 1	V _M	7~33	V
Power supply voltage 2	V _{cc5}	5.0±10%	V
Analog input voltage	V _{analog}	-0.03~V _{cc5}	V
Logic input voltage	V _{logic}	-0.03~V _{cc5}	V

● Block diagram



●Pin descriptions

Pin No.	Pin name	Function
1	OUT A	Motor output A
2	OUT AB	Motor output AB
3	SGA	Ground for channel A output block (connect resistor for detecting channel A output current)
4	SENSE A	Channel A detect signal input (channel A output current)
5	GND	GND
6	GND	GND
7	VrefA	Channel A reference voltage input (channel A output current setting)
8	PHASE A	Logic input A
9	PHASE AB	Logic input AB
10	Vcc5	Power supply
11	PHASE BB	Logic input BB
12	PHASE B	Logic input B
13	VrefB	Channel B reference voltage input (channel B output current setting)
14	SENSE B	Channel B detect signal input (channel B output current)
15	GND	GND
16	GND	GND
17	SGB	Ground for channel B output block (connect resistor for detecting channel B output current)
18	OUT BB	Motor output BB
19	OUT B	Motor output B
20	V _M	Motor power supply

● Input / output circuits

(1) Logic and analog inputs

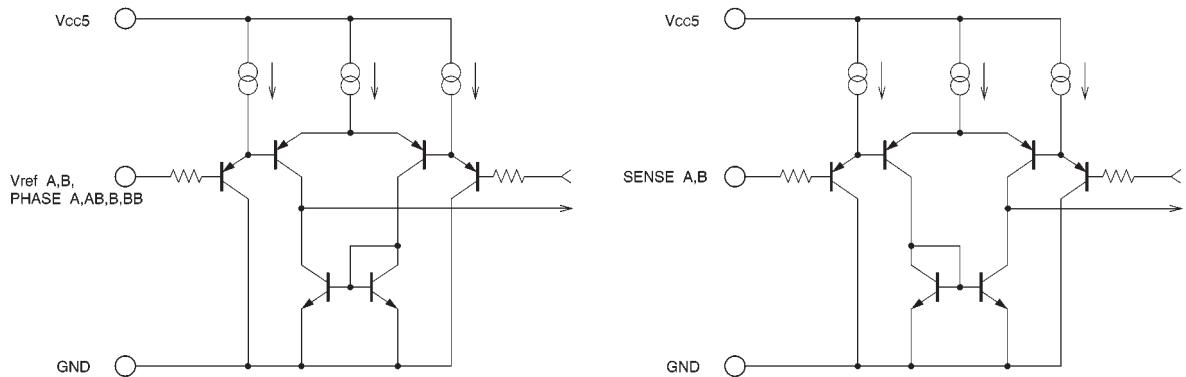


Fig.1 Logic and analog input circuits

(2) H-bridge output

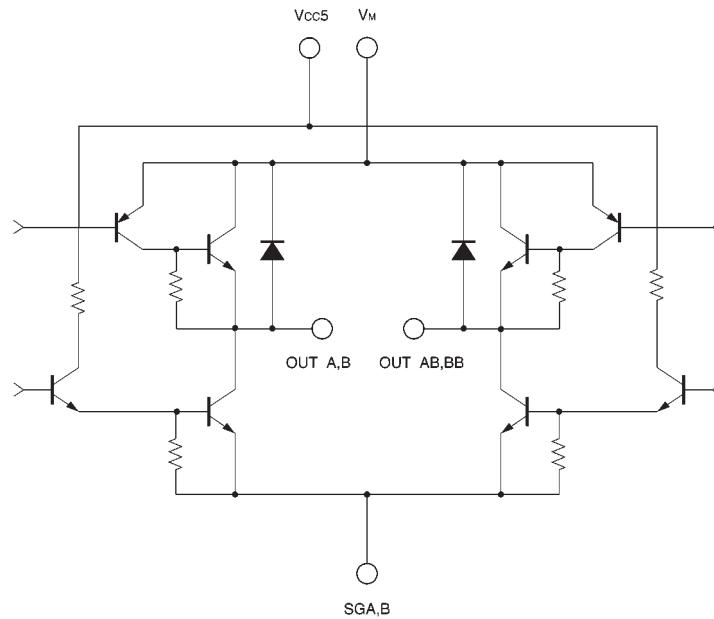


Fig.2 H-bridge output circuit

●Electrical characteristics (unless otherwise noted, $T_a = 25^\circ\text{C}$, $V_M = 13\text{V}$, and $V_{CC} = 5\text{V}$)

(1) DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_M current at standby	I_{Moff}	—	0	10	μA	$V_{CC5}=0\text{V}$
V_M current when operating	I_{Mon}	—	8.0	14.0	mA	$V_{phA}=V_{phB}=\text{"H"}$
Circuit current	I_{CC5on}	—	32	60	mA	$V_{phA}=V_{phB}=\text{"H"}$
V_{CC5} input high level voltage	V_{CC5H}	4.5	5.0	5.5	V	
V_{CC5} input low level voltage	V_{CC5L}	-0.01	—	0.4	V	$I_M \leq 10 \mu\text{A}$
Vref input voltage range	V_{ref}	V_{Coff}	—	$V_{CC5}-2$	V	chA, B
Vref input bias current	I_{ref}	—	—	0.25	μA	$V_{ref}=0\text{V}$, chA, B
Comparator off reference voltage	V_{Coff}	0.1	0.2	0.3	V	$V_{sen}=0\text{V}$, chA, B
SENSE pin threshold voltage	V_{sen}	0.23	0.25	0.27	V	$V_{ref}=2.5\text{V}$, chA, B
SENSE input bias current	I_{sen}	—	—	1.0	μA	$V_{sen}=0\text{V}$, chA, B
Logic input high level voltage	V_{INH}	2.0	—	V_{CC5}	V	phA, AB, B, BB
Logic input low level voltage	V_{INL}	-0.03	—	0.8	V	phA, AB, B, BB
Logic input high level current	I_{INH}	—	—	0.25	μA	$V_{ph}=V_{CC5}$, phA, AB, B, BB
Logic input low level current	I_{INL}	—	—	1.0	μA	$V_{ph}=0\text{V}$, phA, AB, B, BB
Output total saturation voltage	V_{sat}	—	1.2	1.6	V	$I_o=350\text{mA}$, phA, AB, B, BB
Output cutoff current	I_{off}	—	—	0.25	μA	$V_{ph}=\text{"L"}$, chA, B
Output high level clamp voltage	V_{CH}	—	—	1.6	V	$I_o=350\text{mA}$, phA, AB, B, BB
Output low level clamp voltage	V_{CL}	—	—	1.6	V	$I_o=350\text{mA}$, phA, AB, B, BB

(2) AC characteristics (channels A, AB, B, BB, and $R_L = 100\Omega$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output turn on delay	T_{don}	—	—	3.0	μs	$V_{ref}=2.5\text{V}$, $V_{sen}=0.5\text{V} \rightarrow 0\text{V}$
Output turn off delay	T_{doff}	—	—	7.0	μs	$V_{ref}=2.5\text{V}$, $V_{sen}=0\text{V} \rightarrow 0.5\text{V}$
Amp response time for Vref	T_{damp}	—	—	12.0	μs	$V_{sen}=0.25\text{V}$, $V_{ref}=0\text{V} \rightarrow 3\text{V}$
PHASE delay time	T_{dph}	—	—	3.0	μs	$V_{ph}=0\text{V} \rightarrow 5\text{V}$

◎Not designed for radiation resistance.

●Circuit operation

Input / output truth table

Input		Output	
PHASE A, (B)	PHASE A, (BB)	OUT A, (B)	OUT AB, (BB)
L	L	Z	Z
H	L	H	L
L	H	L	H
H	H	Z	Z

Setting: $V_{refA}=V_{refB}=\text{high level}$

SENSE A=SENSE B=low level

Z: high impedance

● Application example

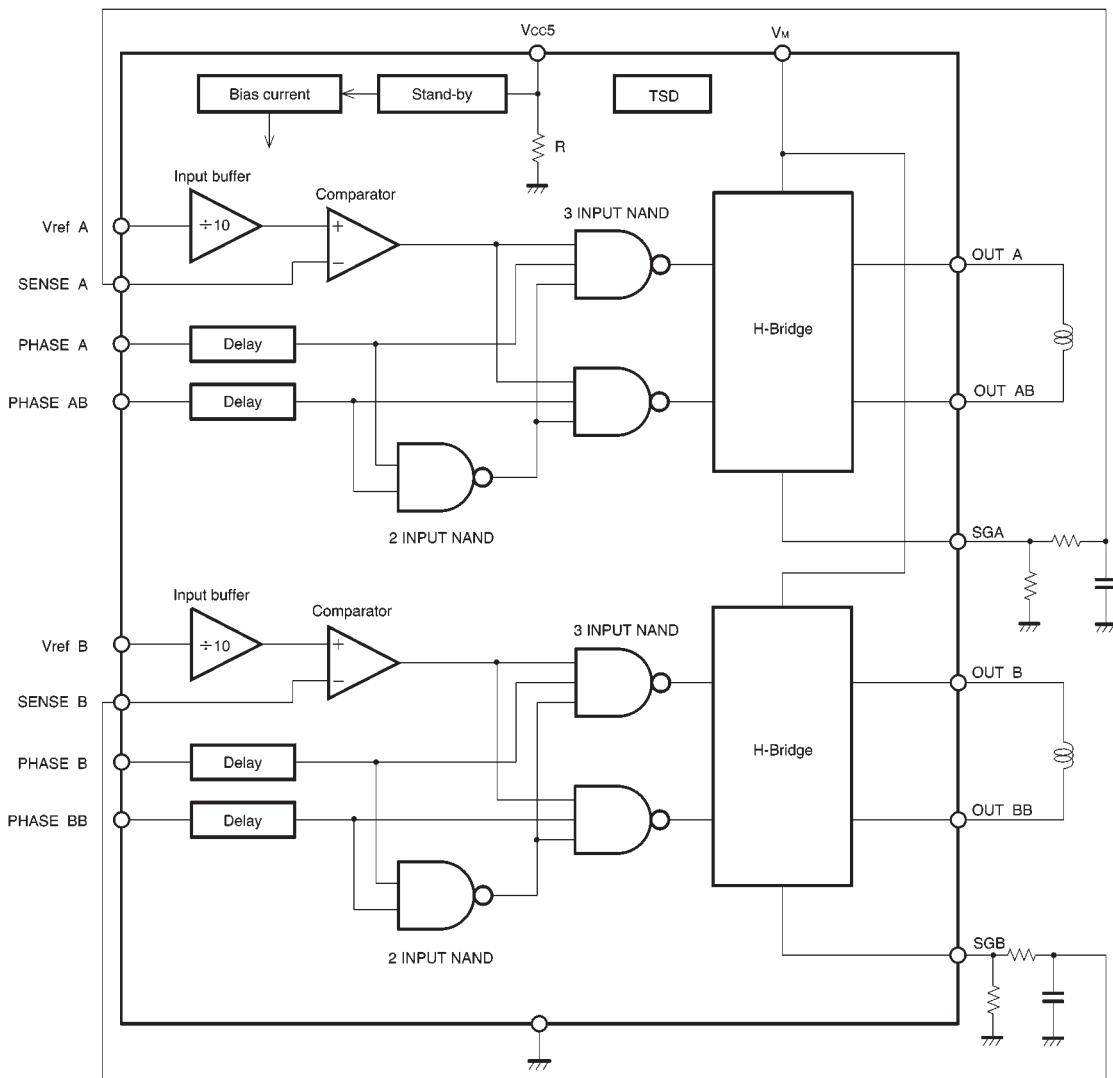


Fig.3

● Operation notes

(1) Power supply voltages 1 and 2 (V_M and V_{CC})
The rise and fall order for the power supply voltages 1 and 2 (V_M and V_{CC5}) is as follows.

Rise: power supply voltage 1 (V_M) on → power supply voltage 2 (V_{CC5}) on

Fall: power supply voltage 2 (V_{CC5}) off → power supply voltage 1 (V_M) off

(2) Logic and analog input pins

Due to the circuit construction, when the logic and analog input pins are open, it is equivalent to a high-level input.

(3) Thermal shutdown (TSD)

● Electrical characteristics curve

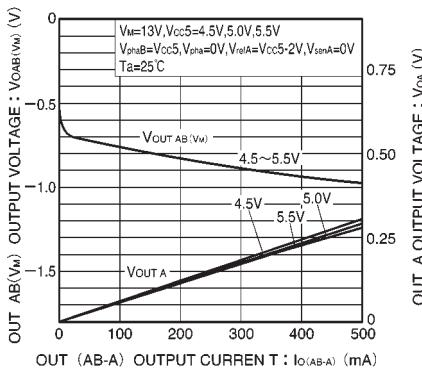
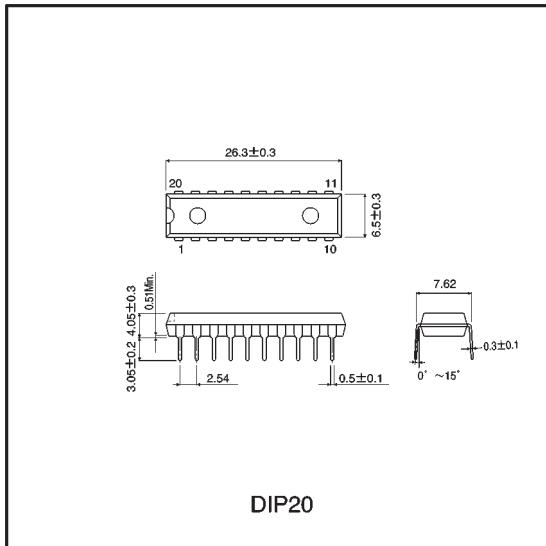


Fig.4 $I_{O(AB-A)}$ vs. $V_{OAB(V_M)}$ and V_{OA}

● External dimensions (Units: mm)



At $T_j = 150^{\circ}C$ (min.), all logic input voltages go low (channels A, AB, B and BB).

Therefore, the outputs (OUTA, AB, B and BB) all go high impedance.

The TSD has approximately $35^{\circ}C$ of hysteresis.

(4) V_{CC5} pin

When V_{CC5} is open, it is internally pulled down to ground via a resistor ($20k\Omega$ (Typ.)).

(5) Heat sink

Be certain to connect the heatsink to GND.