INTERSIL

IH5009 — IH5024 Virtual Ground Analog Switches

FEATURES

- Switches Analog Signals up to 20 Volts Peak-to-Peak
- Each Channel Complete — Interfaces with Most Integrated Logic
- Switching Speeds Less than 0.5μs
- $I_{D(OFF)}$ Less than 500pA Typical at 70°C
- Effective $r_{ds(ON)}$ — 5Ω to 50Ω
- Commercial and Military Temperature Range Operation

GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from T^2L open collector logic (15 volts) while the even numbered devices are driven directly from low level T^2L logic (5 volts). Each channel simulates a SPDT switch. SPST switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

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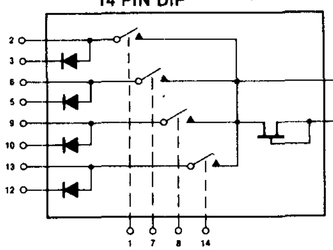
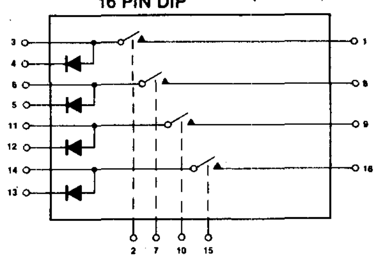
PIN CONNECTIONS

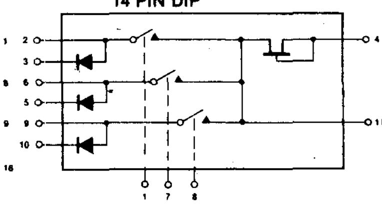
IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP
(OUTLINE DWGS DD, PD, JD)



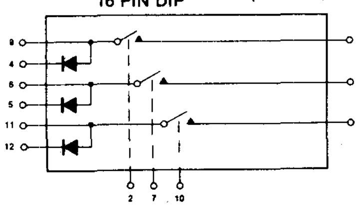
IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP
(OUTLINE DWGS DE, PE, JE)



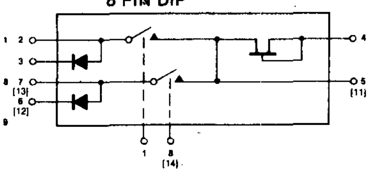
IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP
(OUTLINE DWGS DD, PE, JE)



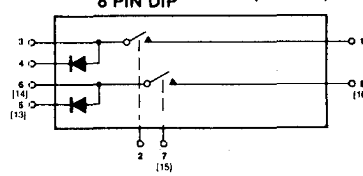
IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP
(OUTLINE DWGS DE, PE, JE)



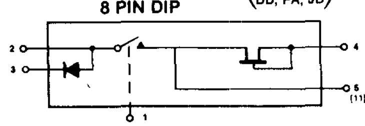
IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DD, PA, JD)



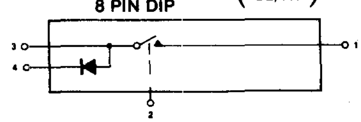
IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DE, PA, JE)



IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DD, PA, JD)



IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP
(OUTLINE DWGS DE, PA)



(Note: Numbers in brackets refer to CERDIP packages.)

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 30V
Negative Analog Signal Voltage .... −15V
Diode Current 10mA
Power Dissipation (Note) 500mW
Storage Temperature .... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

Operating Temperature
5009C Series .... 0°C to +70°C
5009M Series .... −55°C to +125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE (Note 4)	TEST CONDITIONS (Note 2)	SPECIFICATION LIMIT −55°C (M) 0°C (C) MIN/MAX	25°C TYP.	25°C MIN/MAX	+125°C (M) +70°C (C) MIN/MAX	UNITS
$I_{IN(ON)}$	Input Current-ON	All	$V_{IN} = 0V$, $I_D = 2mA$	0.1	.01	0.1	100	μA
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	$V_{IN} = +4.5V$, $V_A = \pm 10V$	0.2	.04	0.1	10	nA
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	$V_{IN} = +11V$, $V_A = \pm 10V$	0.2	.04	0.2	10	nA
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	See Figure 5, Note 3	0.5		0.5	0.5	V
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	See Figure 6, Note 3	1.5		1.5	1.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 5, Note 3	4.5		4.5	4.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 6, Note 3	11.0		11.0	11.0	V
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	$V_{IN} = +4.5V$, $V_A = \pm 10V$	0.2	.02	0.2	10	nA
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	$V_{IN} = +11V$, $V_A = \pm 10V$	0.2	.02	0.2	10	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN} = 0V$, $I_S = 1mA$	1.0	0.30	1.0	1000 (M) 200 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN} = 0V$, $I_S = 1mA$	0.5	0.10	0.5	500 (M) 100 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN} = 0V$, $I_S = 2mA$	1.0		1.0	10	μA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN} = 0V$, $I_S = 2mA$	2.0		2.0	1000	nA
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	$I_D = 2mA$, $V_{IN} = 0.5V$	150	90	150	385 (M) 240 (C)	Ω
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	$I_D = 2mA$, $V_{IN} = 1.5V$	100	60	100	250 (M) 160 (C)	Ω
$t_{(on)}$	Turn-ON Time	All	See Figures 3 & 4		150	500		ns
$t_{(off)}$	Turn-OFF Time	All	See Figures 3 & 4		300	500		ns
CT	Cross Talk	All	f = 100Hz		120			dB

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.
NOTE 2: Refer to Figure 2 for definition of terms.
NOTE 3: $V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the tests of respectively $r_{DS(ON)}$ and $I_{D(OFF)}$.
NOTE 4: "5V Logic CKTS" applies to even-numbered devices.
"15V Logic CKTS" applies to odd-numbered devices.

ORDERING INFORMATION

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IH50XX   M   DE
 │       │   │
 │       │   └──PACKAGE──┬ PA — 8-PIN PLASTIC DIP
 │       │               │ PD — 14-PIN PLASTIC DIP
 │       │               │ PE — 16-PIN PLASTIC DIP
 │       │               │ DD — 14-PIN CERAMIC DIP (Special Order Only)
 │       │               │ DE — 16-PIN CERAMIC DIP (Special Order Only)
 │       │               │ JD — 14-PIN CERDIP
 │       │               └ JE — 16-PIN CERDIP
 │       └──TEMPERATURE RANGE
 │            M = MILITARY (−55°C to +125°C)
 │            C = COMMERCIAL (0°C to +70°C)
 └──BASIC PART NUMBER
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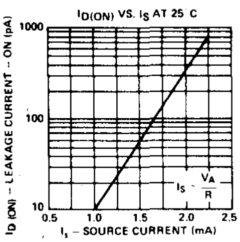
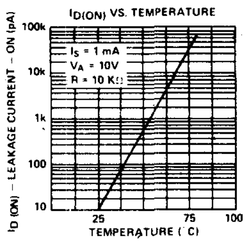
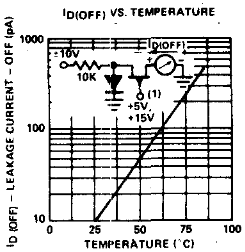
BASIC PART NUMBER	CHANNELS	LOGIC LEVEL	PACKAGES
IH5009	4	+15	JD,DD,PD
IH5010	4	+5	JD,DD,PD
IH5011	4	+15	JE,DE,PE
IH5012	4	+5	JE,DE,PE
IH5013	3	+15	JD,DD,PD
IH5014	3	+5	JD,DD,PD
IH5015	3	+15	JE,DE,PE
IH5016	3	+5	JE,DE,PE
IH5017	2	+15	JD,DD,PA
IH5018	2	+5	JD,DD,PA
IH5019	2	+15	JE,DE,PA
IH5020	2	+5	JE,DE,PA
IH5021	1	+15	JD,DD,PA
IH5022	1	+5	JD,DD,PA
IH5023	1	+15	JE,DE,PA
IH5024	1	+5	JE,DE,PA

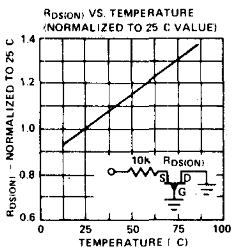
NOTE: Mil-Temperature range (−55°C to +125°C) available ceramic packages only.

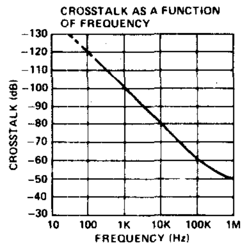
TYPICAL ELECTRICAL CHARACTERISTICS (per channel)



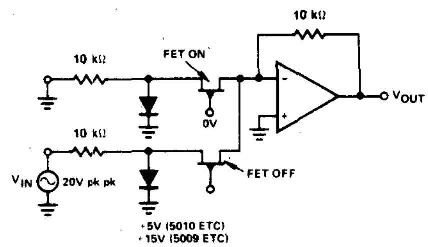








CROSSTALK MEASUREMENT CIRCUIT

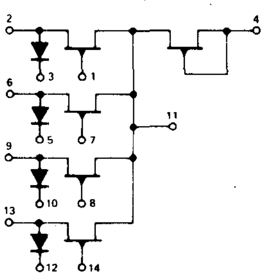


3

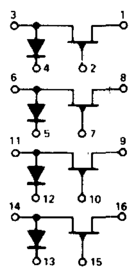
DEVICE SCHEMATICS AND PIN CONNECTIONS

FOUR CHANNEL

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

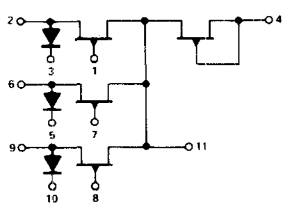


IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

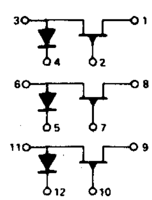


THREE CHANNEL

IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

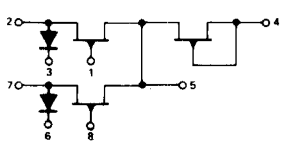


IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

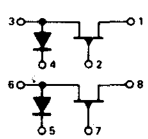


TWO CHANNEL

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

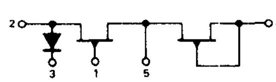


IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

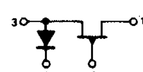


SINGLE CHANNEL

IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



THEORY OF OPERATION

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories; those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to ±200mV, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that $V_{GS} = 0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 1) the gain is given by

$$\text{GAIN} = \frac{10\text{k}\Omega + r_{DS(ON)}\ (\text{compensator})}{10\text{k}\Omega + r_{DS}\ (\text{switch})}$$

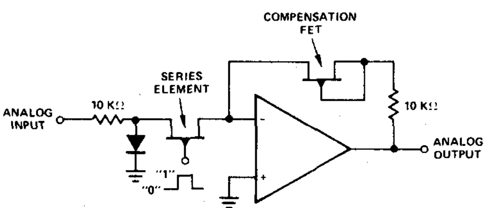


Figure 1. Use of Compensation FET

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. Contact factory for details. Since the absolute value of $r_{DS(ON)}$ is guaranteed only to be less than 100Ω or 150Ω, a substantial improvement in gain accuracy can be obtained by using the compensating FET.

DEFINITION OF TERMS

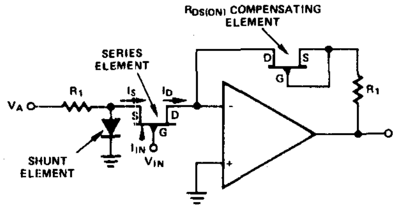


Figure 2.

NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series elements is OFF. For example, if a ±10V analog input is being switched by T²L open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time, the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

When switching a negative voltage, the input further increases the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

SWITCHING CHARACTERISTICS

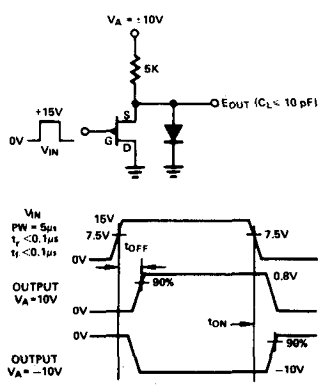


Figure 3. High Level Logic

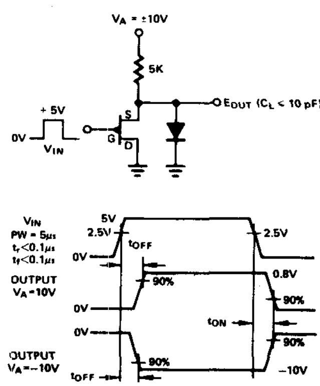


Figure 4. Standard DTL, TTL, RTL

LOGIC INTERFACE CIRCUITS

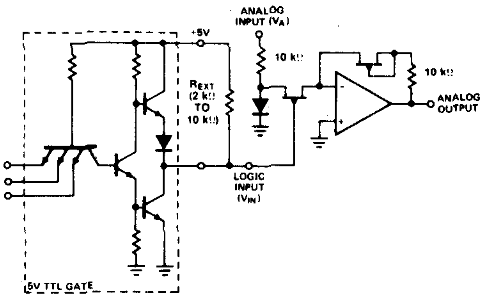


Figure 5. Interfacing with +5V Logic

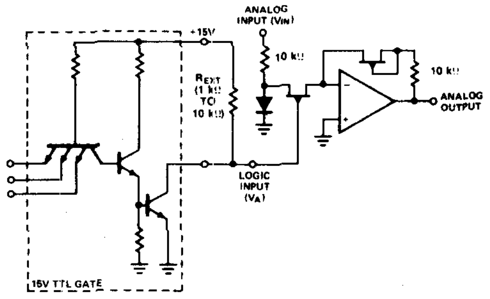


Figure 6. Interfacing with +15V Open Collector Logic

APPLICATIONS (Note)

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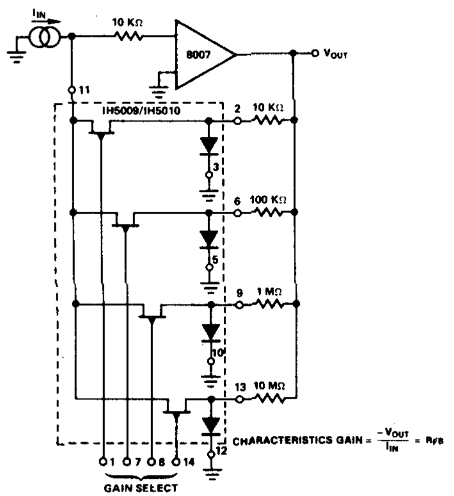

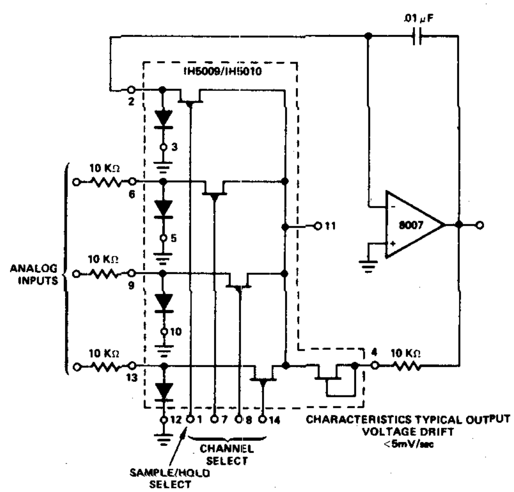

NOTE: Additional applications information is given in Application Bulletins A003 "Understanding and Applying the Analog Switch" and A004 "The 5009 Series of Low Cost Analog Switches". See also September '79 issue of Product Engineering "Analog Switching" by Paresh Maniar.