

EB52F4D50CN-33.000M

[Click part number to visit Part Number Details page](#)

REGULATORY COMPLIANCE (Data Sheet downloaded on Oct 23, 2016)



ITEM DESCRIPTION

Temperature Compensated Quartz Crystal Clock Oscillators TCXO LVCMOS (CMOS) 3.3Vdc 14-Pin DIP Metal Thru-Hole 33.000MHz $\pm 2.5\text{ppm}$ Maximum $\pm 5.0\text{ppm}$ Maximum -20°C to +70°C

ELECTRICAL SPECIFICATIONS

Nominal Frequency	33.000MHz
Initial Tolerance	$\pm 2.5\text{ppm}$ Maximum (Measured at Nominal Vdd and Vc)
Frequency Stability	$\pm 5.0\text{ppm}$ Maximum
Frequency Stability vs. Input Voltage	$\pm 0.3\text{ppm}$ Maximum (Vdd $\pm 5\%$)
Frequency Stability vs. Load	$\pm 0.2\text{ppm}$ Maximum ($\pm 10\%$)
Frequency Stability vs. Aging	$\pm 1\text{ppm/Year}$ Maximum (at 25°C)
Operating Temperature Range	-20°C to +70°C
Supply Voltage	3.3Vdc $\pm 5\%$
Input Current	25mA Maximum (Measured at Steady State at 25°C)
Output Voltage Logic High (Voh)	90% of Vdd Minimum
Output Voltage Logic Low (Vol)	10% of Vdd Maximum
Rise/Fall Time	6nSec Maximum (Measured at 20% to 80% of waveform)
Duty Cycle	50 $\pm 5\%$ (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Control Voltage	None (No Connect on Pin 1)
Input Impedance	10kOhms Typical
Phase Noise	-70dBc/Hz at 10Hz Offset -100dBc/Hz at 100Hz Offset -130dBc/Hz at 1kHz Offset -140dBc/Hz at 10kHz Offset -145dBc/Hz at 100kHz Offset (Typical Values at 19.440MHz)
Storage Temperature Range	-55°C to +125°C

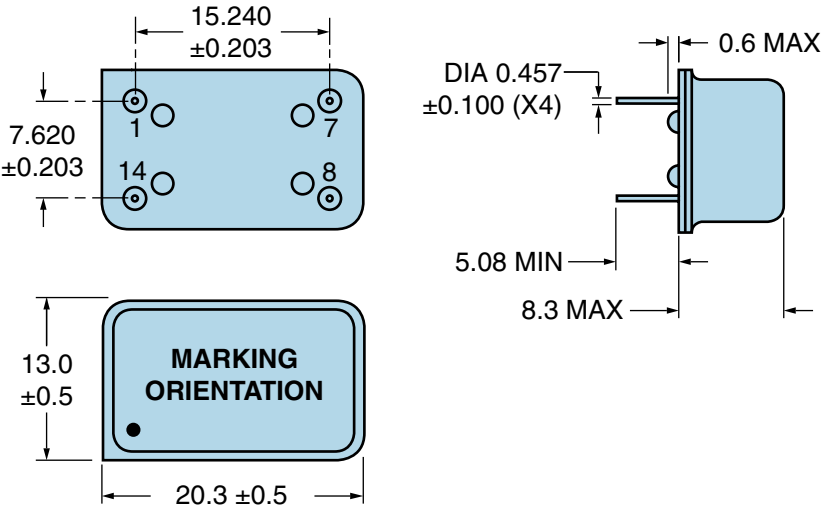
ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

Fine Leak Test	MIL-STD-883, Method 1014 Condition A
Gross Leak Test	MIL-STD-883, Method 1014 Condition C
Lead Integrity	MIL-STD-883, Method 2004
Mechanical Shock	MIL-STD-202, Method 213 Condition C
Resistance to Soldering Heat	MIL-STD-202, Method 210
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003
Temperature Cycling	MIL-STD-883, Method 1010
Vibration	MIL-STD-883, Method 2007 Condition A

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MECHANICAL DIMENSIONS (all dimensions in millimeters)



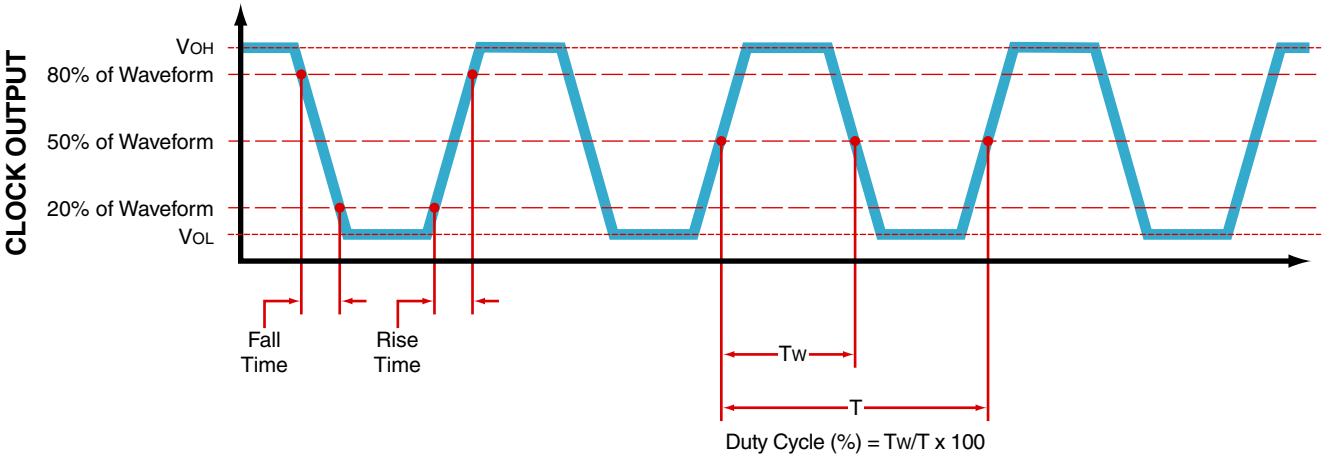
PIN	CONNECTION
1	No Connect
7	Case Ground
8	Output
14	Supply Voltage

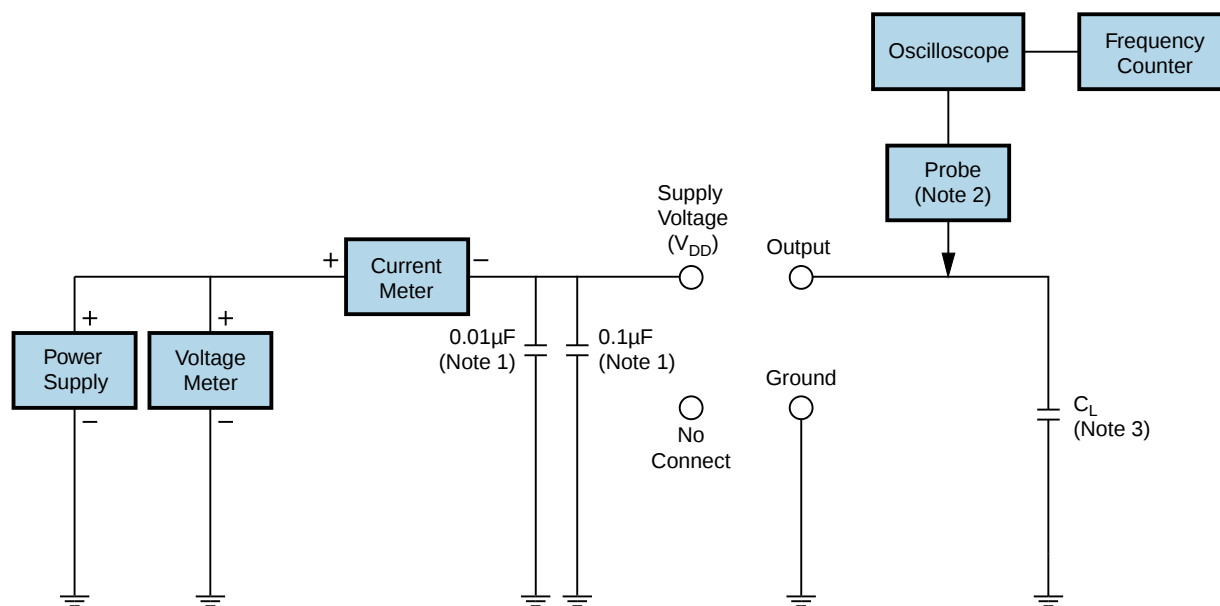
LINE	MARKING
1	ECLIPTEK
2	33.000M
3	XXXXXX XXXXXX=Ecliptek Manufacturing Identifier

EB52F4D50CN-33.000M [Click part number to visit Part Number Details page](#)



OUTPUT WAVEFORM



EB52F4D50CN-33.000M
[Click part number to visit Part Number Details page](#)
Test Circuit for No Connect Option

Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

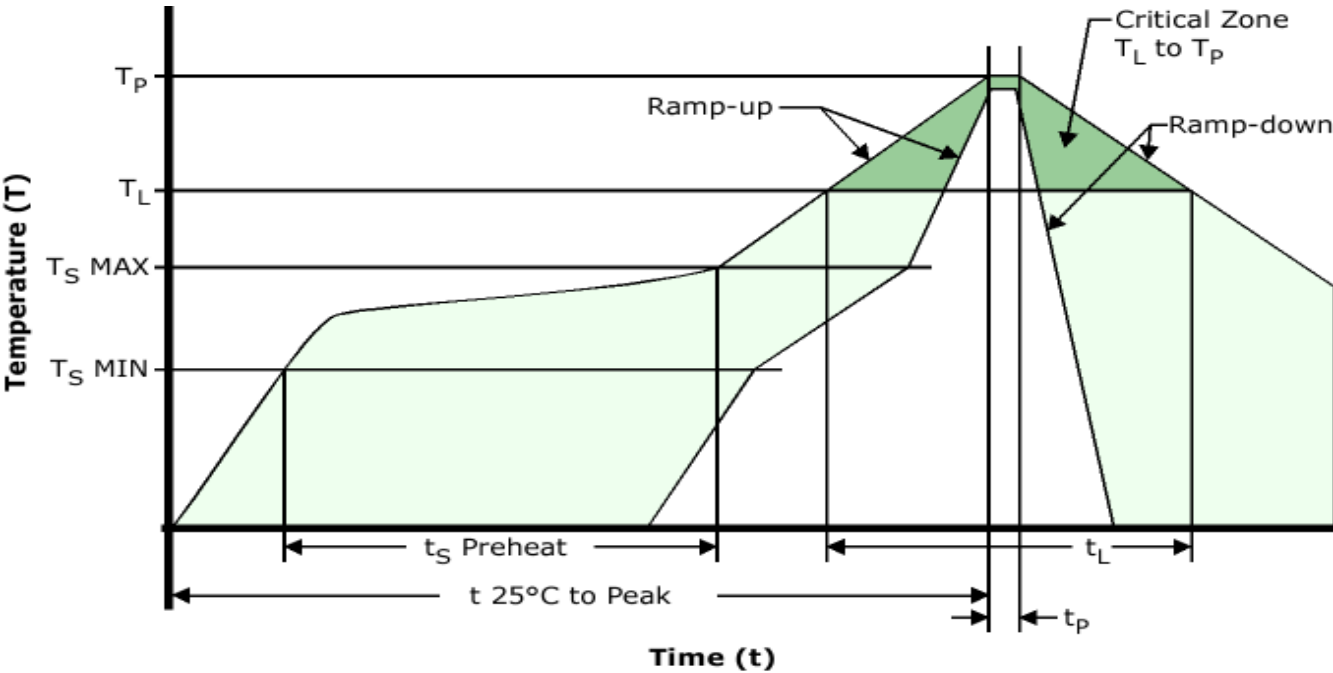
Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value C_L includes sum of all probe and fixture capacitance.

EB52F4D50CN-33.000M [Click part number to visit Part Number Details page](#)



Recommended Solder Reflow Methods



Low Temperature Solder Bath (Wave Solder)

$T_S \text{ MAX}$ to T_L (Ramp-up Rate)	5°C/Second Maximum
Preheat	
- Temperature Minimum ($T_S \text{ MIN}$)	N/A
- Temperature Typical ($T_S \text{ TYP}$)	150°C
- Temperature Maximum ($T_S \text{ MAX}$)	N/A
- Time ($t_s \text{ MIN}$)	30 - 60 Seconds
Ramp-up Rate (T_L to T_P)	5°C/Second Maximum
Time Maintained Above:	
- Temperature (T_L)	150°C
- Time (t_L)	200 Seconds Maximum
Peak Temperature (T_P)	245°C Maximum
Target Peak Temperature ($T_P \text{ Target}$)	245°C Maximum 1 Time / 235°C Maximum 2 Times
Time within 5°C of actual peak (t_p)	5 Seconds Maximum 1 Time / 15 Seconds Maximum 2 Times
Ramp-down Rate	5°C/Second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 Seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 Seconds Maximum, 2 times Maximum.