270-441

TELEDYNE COMPONENTS

TC7106/7106A
TC7107/7107A

3-1/2 DIGIT A/D CONVERTER

FEATURES

- Internal Reference with Low Temperature Drift ..... 20 ppm/°C Typical 50 ppm/°C Maximum
- Drives LCD (TC7106) or LED (TC7107) Display Directly
- Guaranteed Zero Reading With Zero Input
- Low Noise for Stable Display
- Auto-Zero Cycle Eliminates Need for Zero Adjustment
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TC7106A)
- High Impedance CMOS Differential Inputs .... $10^{12}\Omega$
- Differential Reference Inputs Simplify Ratiometric Measurements
- Low Power Operation ..... 10 mW
- Available in 60-Pin Plastic Flat Package

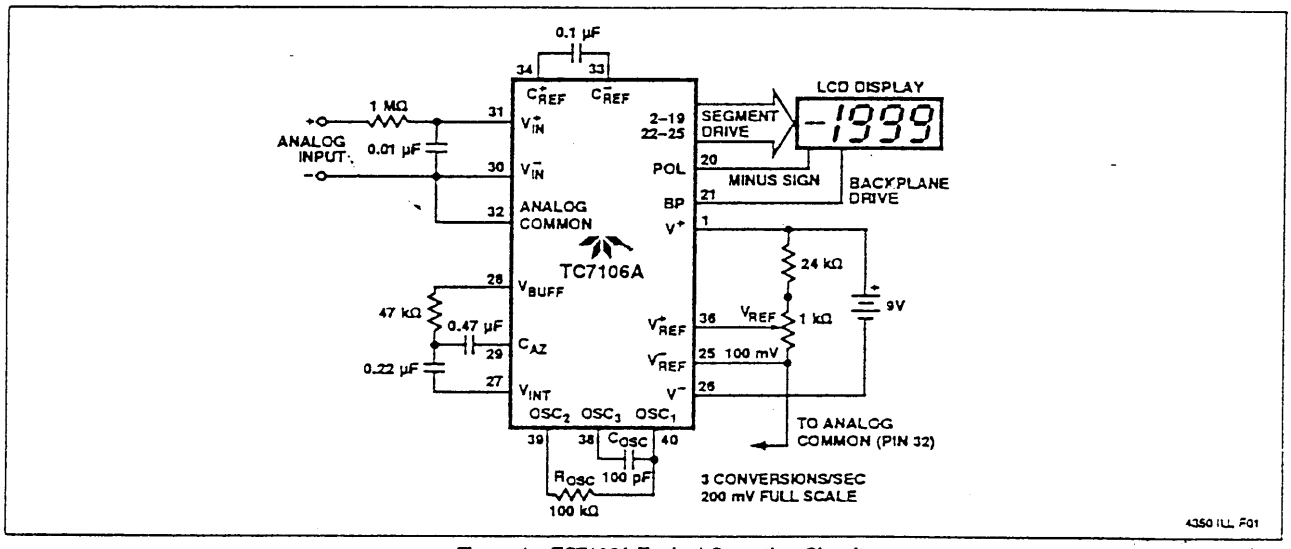


Figure 1 TC7106A Typical Operating Circuit

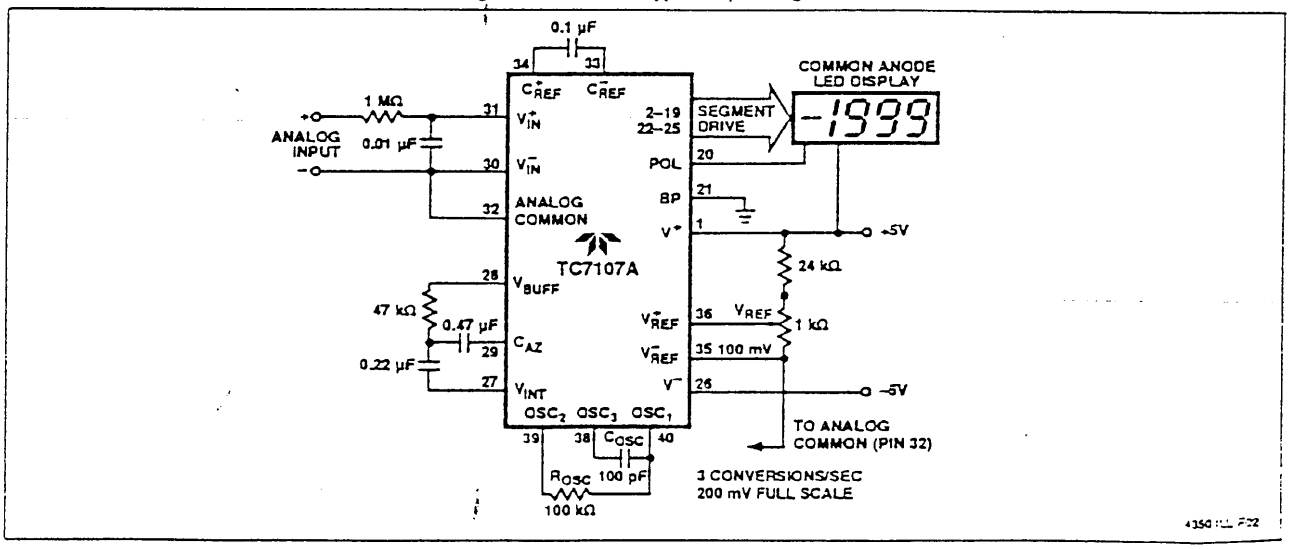


Figure 2 TC7107A Typical Operating Circuit

TC7106/7106A
TC7107/7107A

GENERAL DESCRIPTION

The TC7106A and TC7107A 3-1/2 digit direct display drive analog-to-digital converters allow existing 7106/7107 based systems to be upgraded. Each device offers a precision internal voltage reference featuring a 20 ppm/°C maximum temperature drift coefficient. This represents a 4 to 7 times improvement over similar 3-1/2 digit converters. Existing 7106 and 7107 based systems may be upgraded without changing external passive component values. The need for a costly, space consuming external reference is removed. The TC7107A drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment. A low cost, high resolution indicating meter requires only a display, four resistors, and four capacitors. The TC7106A low power drain and 9 V battery operation make it suitable for portable applications.

The TC7106A/TC7107A reduces linearity error to less than 1 count. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals—is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{P-P} noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

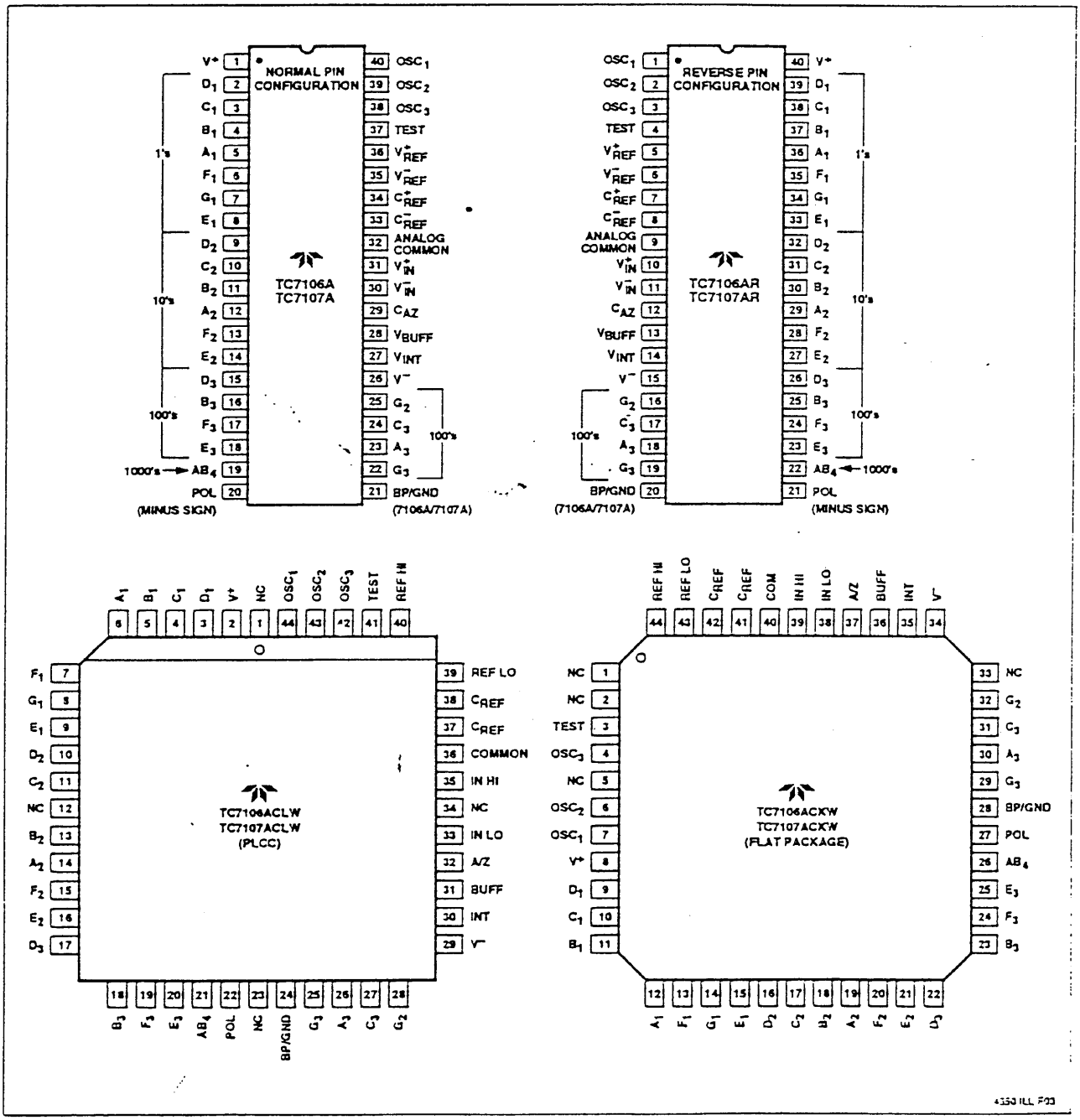
The TC7106A/TC7107A dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TC7106A/TC7107A are available in a small 60-pin flat package for compact designs. DIP devices are offered in an industrial temperature range.

ORDERING INFORMATION

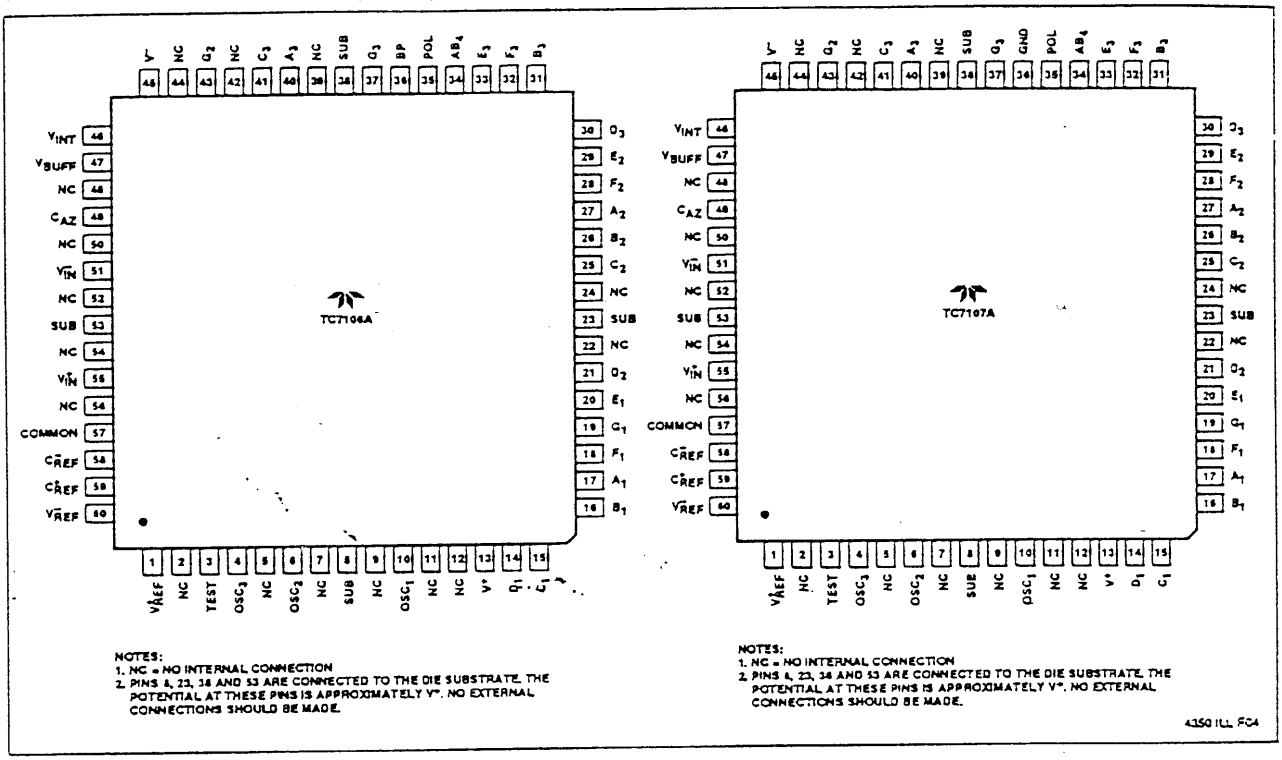
Part No.	Package	Pin Layout	Temperature Range	Display Drive
TC7106CPL	40-Pin Plastic DIP	Normal	0°C to +70°C	LCD
TC7106RCPL	40-Pin Plastic DIP	Reverse	0°C to +70°C	LCD
TC7106IJL	40-Pin CerDIP	Normal	–25°C to +85°C	LCD
TC7106CSQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TC7106CKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LCD
TC7106CLW	44-Pin PLCC	—	0°C to +70°C	LCD
TC7107CPL	40-Pin Plastic DIP	Normal	0°C to +70°C	LED
TC7107RCPL	40-Pin Plastic DIP	Reverse	0°C to +70°C	LED
TC7107IJL	40-Pin CerDIP	Normal	–25°C to +85°C	LED
TC7107CSQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TC7107CKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LED
TC7107CLW	44-Pin PLCC	—	0°C to +70°C	LED
TC7106ACPL	40-Pin Plastic DIP	Normal	0°C to +70°C	LCD
TC7106ARCPL	40-Pin Plastic DIP	Reverse	0°C to +70°C	LCD
TC7106AIJL	40-Pin CerDIP	Normal	–25°C to +85°C	LCD
TC7106ACSQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TC7106ACKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LCD
TC7106ACLW	44-Pin PLCC	—	0°C to +70°C	LCD
TC7107ACPL	40-Pin Plastic DIP	Normal	0°C to +70°C	LED
TC7107ARCPL	40-Pin Plastic DIP	Reverse	0°C to +70°C	LED
TC7107AIJL	40-Pin CerDIP	Normal	–25°C to +85°C	LED
TC7107ACSQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TC7107ACKW	44-Pin Plastic Flat	Formed Leads	0°C to +70°C	LED
TC7107ACLW	44-Pin PLCC	—	0°C to +70°C	LED

PIN CONFIGURATIONS



TC7106/7106A
TC7107/7107A

PIN CONFIGURATIONS (Cont.)



ABSOLUTE MAXIMUM RATINGS*

TC7106A

Supply Voltage (V+ to V−) ..... 15 V
Analog Input Voltage (either input) (Note 1) ..... V+ to V−
Reference Input Voltage (either input) ..... V+ to V−
Clock Input ..... Test to V+
Power Dissipation (Note 2)
- CerDIP Package ..... 1000 mW
- Plastic Package ..... 800 mW

Operating Temperature
- "C" Devices ..... 0°C to +70°C
- "I" Devices ..... −25°C to +85°C

Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

TC7107A

Supply Voltage
- V+ ..... +6 V
- V− ..... −9 V

Analog Input Voltage (either input) (Note 1) ..... V+ to V−
Reference Input Voltage (either input) ..... V+ to V−
Clock Input ..... GND to V+
Power Dissipation (Note 2)
- CerDIP PAckage ..... 1000 mW
- Plastic Package ..... 800 mW

Operating Temperature
- "C" Devices ..... 0°C to +70°C
- "I" Devices ..... −25°C to +85°C

Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

Characteristics	Conditions	TC811 Min	TC811 Typ	TC811 Max	Unit
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \equiv$ 200 mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200.0 mV	—	50	—	µV/V
Noise (Pk – Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	µV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C	—	0.2	1	µV/°C
	V_{IN} = 0 V "I" Device = -25°C to +85°C	—	1.0	2	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm°C)	—	1	5	ppm/°C
	V_{IN} = 199.0 mV "I" Device = -25°C to +85°C	—	—	20	ppm/°C
Supply Current (Does Not Include LED Current For TC7107A)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25kΩ Between Common and Pos. Supply	2.7	3.05	3.35	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25kΩ Between Common and Pos. Supply 0°C ≤ T_A ≤ 70°C "C," Industrial Temp. Range Devices	—	20	50	ppm/°C
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25kΩ Between Common and Pos. Supply 0°C ≤ T_A ≤ 85°C "I," Industrial Temp. Range Devices	—	—	75	ppm/°C
TC7106A ONLY Pk – Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TC7106A ONLY Pk – Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TC7107A ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TC7107A ONLY Segment Sinking Current (Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ±100 µA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply to both the TC7106A and TC7107A at TA = 25°, f_{CLOCK} = 48 kHz. TC7106A is tested in the circuit of Figure 1. TC7107A is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.

TC7106/7106A
TC7107/7107A

PIN DESCRIPTION

40-Pin DIP Pin Number (Normal)	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the tens display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP GND	LCD Backplane drive output (TC7106A). Digital ground (TC7107A).
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for more details
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ resistor for a 200 mV full-scale range and a 470 kΩ resistor for 2V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences system noise. Use a 0.47-μF capacitor for 200 mV full scale, and a 0.047-μF capacitor for 2V full scale. See Paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The analog low input is connected to this pin.
31	(10)	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. It also acts as a reference voltage source. See paragraph on ANALOG COMMON for more details.
33	(8)	58	C_{REF}^-	See pin 34.

PIN DESCRIPTION (Cont.)

40-Pin DIP Pin Number (Normal)	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
34	(7)	59	C^{+}_{REF}	A 0.1-μF capacitor is used in most applications. If a large common-mode voltage exists (for example, the V_{IN} pin is not at analog common), and a 200-mV scale is used, a 1-μF capacitor is recommended and will hold the roll-over error to 0.5 count.
35	(6)	60	V^{-}_{REF}	See pin 36.
36	(5)	1	V^{+}_{REF}	The analog input required to generate a full-scale output (1999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1V between pins 35 and 36 for 2V full scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V+) all segments will be turned on and the display should read −1888. It may also be used as a negative supply for externally-generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48-kHz clock (3 readings per section), connect pin 40 to the junction of a 100-kΩ resistor and a 100-pF capacitor. The 100-kΩ resistor is tied to pin 39 and the 100-pF capacitor is tied to pin 38.

General Theory of Operation
Dual Slope Conversion Principles

The TC7106A and TC7107A are dual slope, integrating analog-to-digital converters. An understanding of the dual slope conversion technique will aid in following the detailed operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 3A).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_{0}^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

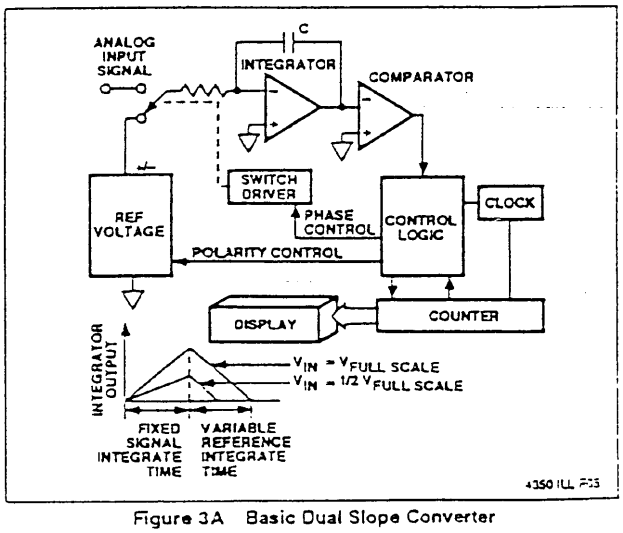


Figure 3A Basic Dual Slope Converter

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environment. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period. (Figure 3B)

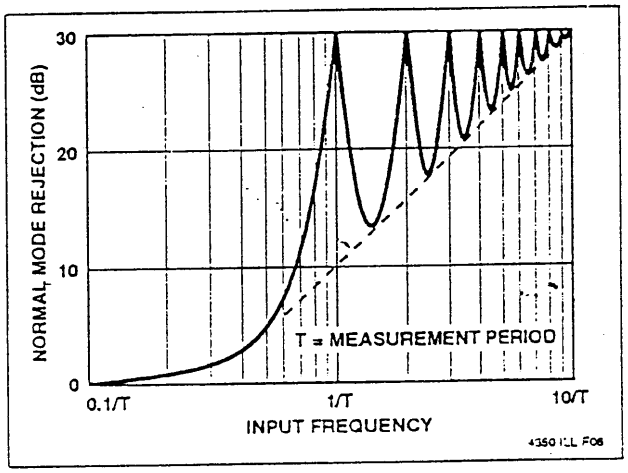


Figure 3B Normal-Mode Rejection of Dual Slope Converter

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed, the circuit incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto zero, signal integrate and reference integrate cycle.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The offset error referred to the input is less than 10 μV.

The auto-zero cycle length is 1000 to 3000 counts.

Signal Integrate Cycle

The auto-zero loop in opened, the internal differential inputs connect to V_{IN}^{+} and V_{IN}^{-}. The differential input signal is integrated for a fixed time period. The signal integration period is 1000 counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

where:

f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range (1 V of either supply) when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^{-} should be tied to analog common.

Polarity is determined at the end of signal integrate phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Cycle

The final phase is reference integrate or de-integrate. V_{IN}^{-} is internally connected to analog common and V_{IN}^{+} is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Digital Section (TC7106A)

The TC7106A (Figure 5) contains all the segment drivers necessary to directly drive a 3 1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^{+} and V_{IN}^{-} are reversed this indicator would reverse.

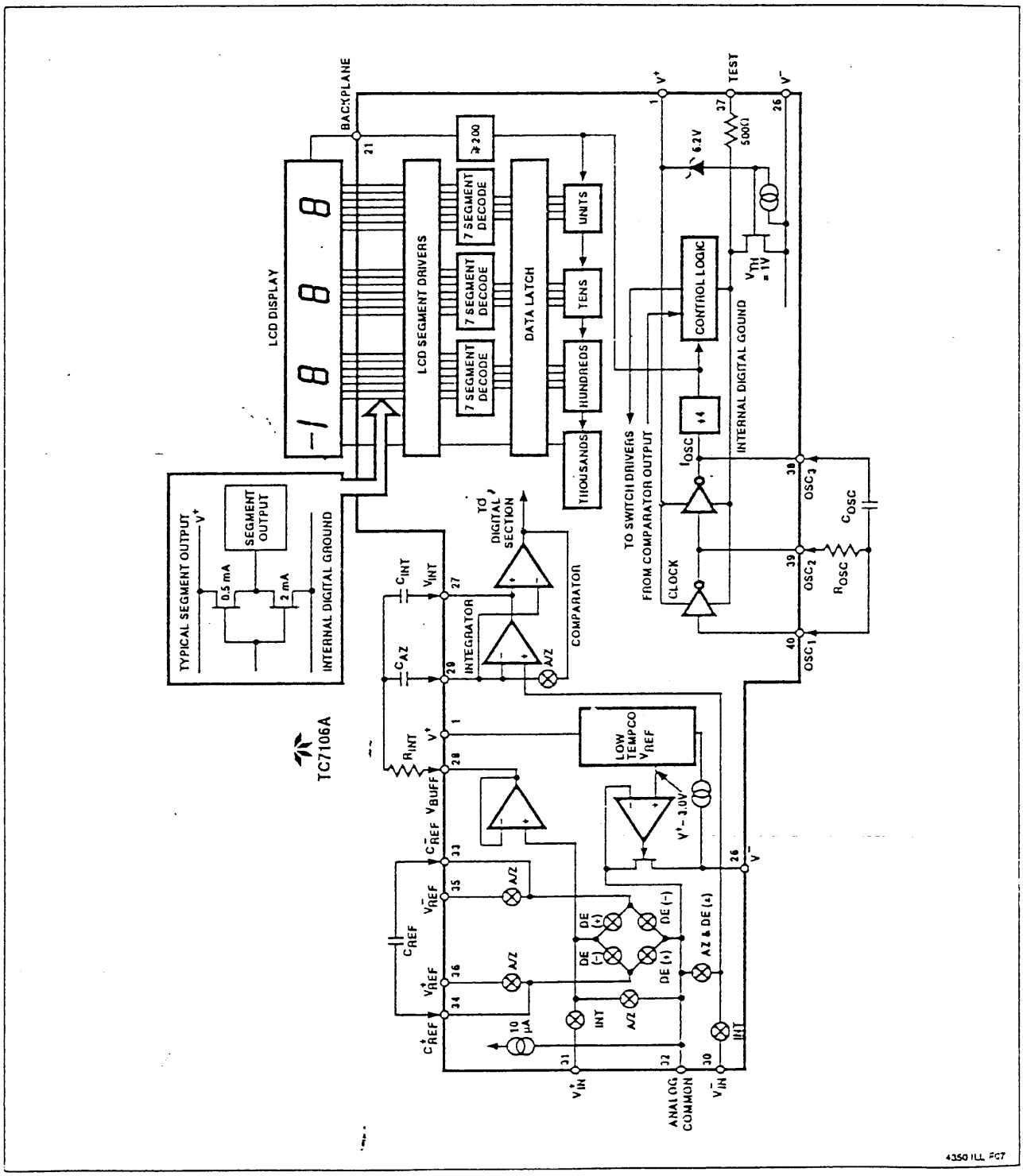


Figure 5 TC7106A Block Diagram

On the TC7106A when the test pin is pulled to V+ all segments are turned "ON." The display reads −1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and the segment drive assignment are shown in Figure 6.

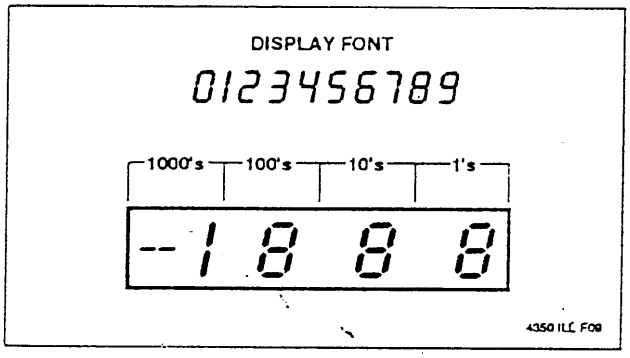


Figure 6 Display FONT and Segment Assignment

In the TC7106A an internal digital ground is generated from a 6 volt zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the backplane voltage is switched.

Digital Section (TC7107A)

Figure 7 shows the TC7107A. It is identical to the TC7106A except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TC7107A is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

The display font is the same as the TC7106A.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The three phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1000 to 3000 Counts
  (4000 to 12000 Clock Pulses)
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 1000 Counts
  (4000 Clock Pulses)
  This time period is fixed. The integration period is:

$$T_{SI} = 4000 \left[\frac{1}{f_{OSC}} \right]$$

  Where f_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 2000 Counts
  (0 to 8000 Clock Pulses)

The TC7106A/7107A are drop in replacements for the 7106/7107 parts. External component value changes are not required to benefit from the low drift internal reference.

Clock Circuit

Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

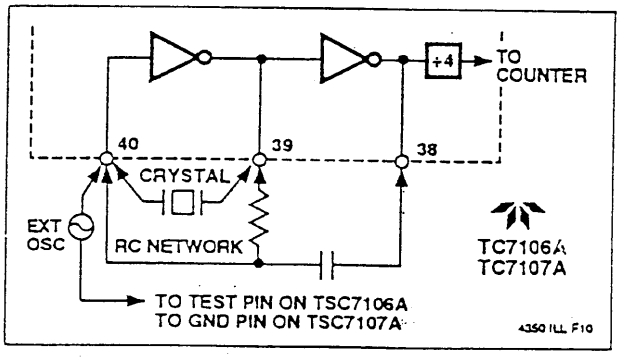


Figure 8 Clock Circuits

Component Value Selection
Auto-Zero Capacitor – C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.47 µF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 µV. A 0.047 µF capacitor is adequate for 2.0 V full-scale applications. A mylar type dielectric capacitor is adequate.

Reference Voltage Capacitor – C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 µF capacitor is acceptable when V_{IN}^- is tied to analog common. If a large common-mode voltage exists (V_{REF}^- ≠ analog common) and the application requires a 200 mV full-scale increase C_{REF} to 1.0 µF. Rollover error will be held to less than 0.5 count. A mylar type dielectric capacitor is adequate.

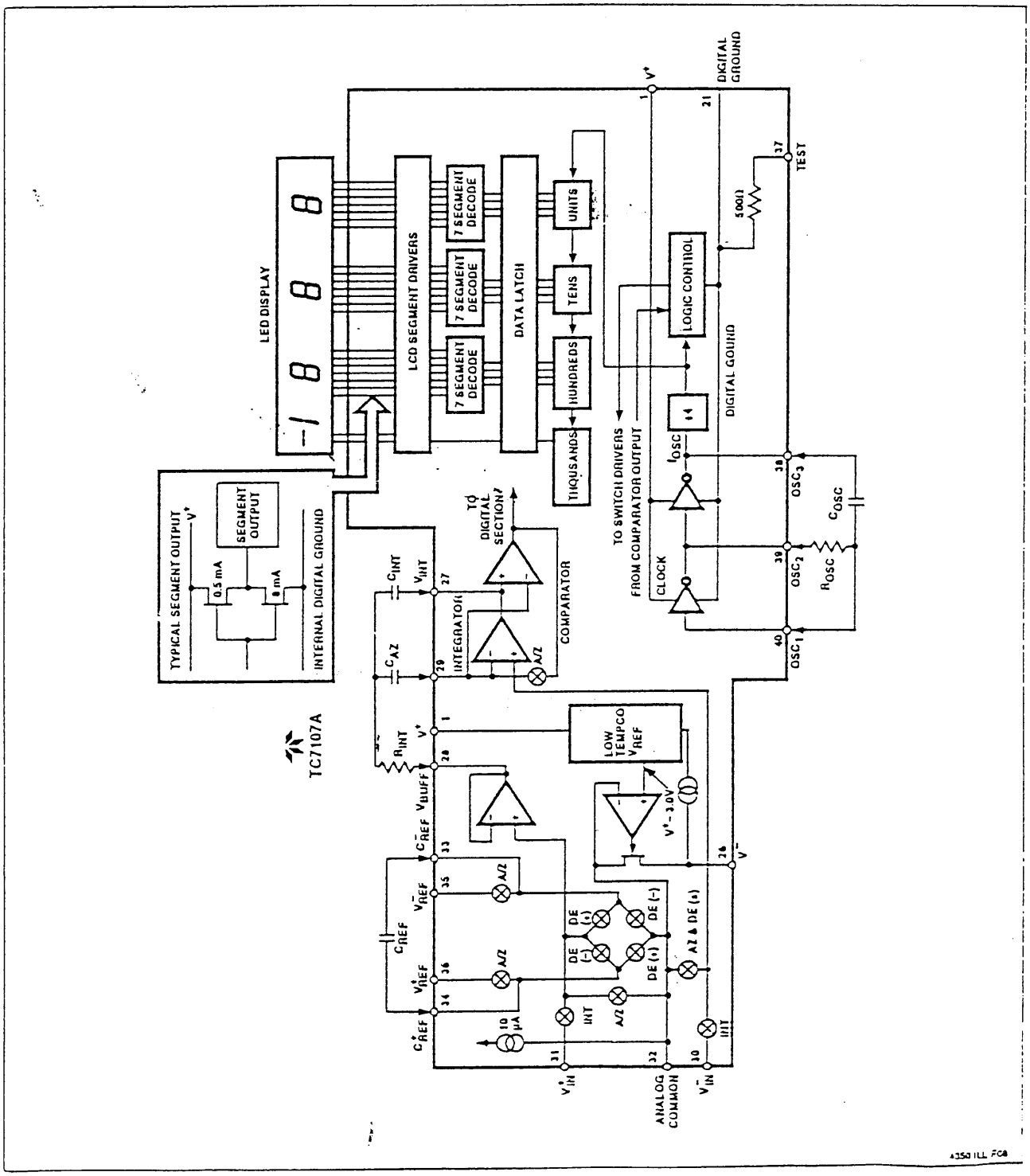


Figure 7 TC7107A Block Diagram

Integrating Capacitor – C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TC7106A/7107A superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.22 µF value is suggested. If a different oscillator frequency is used C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize rollover error. An inexpensive polypropylene capacitor is recommended.

INTEGRATING RESISTOR – R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100 µA. The integrator and buffer can supply 20 µA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale R_{INT} is 47 kΩ. A 2.0 V full-scale requires 470 kΩ.

Component	Nominal Full-Scale Voltage	
Value	200.0 mV	2.000 V
C_{AZ}	0.47 µF	0.047 µF
R_{INT}	47 kΩ	470 kΩ
C_{INT}	0.22 µF	0.22 µF

Note: 1. f_{OSC} = 48 kHz (3 readings/sec)

Oscillator Components

R_{OSC} (Pin 40 to Pin 39) should be 100 kΩ. C_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

For f_{OSC} of 48 kHz, C_{OSC} is 100 pF nominally.

Note that f_{OSC} is divided by four to generate the TC7106A internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 Khz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	V_{REF}
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\ V_{REF}$

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in^2. Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and $V_{\overline{IN}}$. The transducer output is connected between $V_{\overline{IN}}$ and analog common.

The internal voltage reference potential available at analog common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where externally generated reference voltage is desired refer to Figure 9.

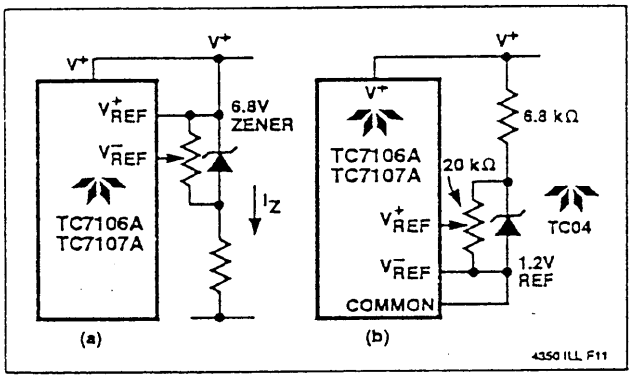


Figure 9 External Reference

Device Pin Functional Description

Differential Signal Inputs (V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TC7106A/7017A is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (V_{CM}). The typical range is $V^+ -1.0$ to $V^- +1$ V. Common-mode voltages are removed from the system when the TC7106A/TC7107A operates from a battery or floating power source (isolated from measured system) and V_{IN}^- is connected to analog common (V_{COM}): See Figure 10.

In systems where common-mode voltages exist in 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 11). For such applications the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increasing linearity errors.

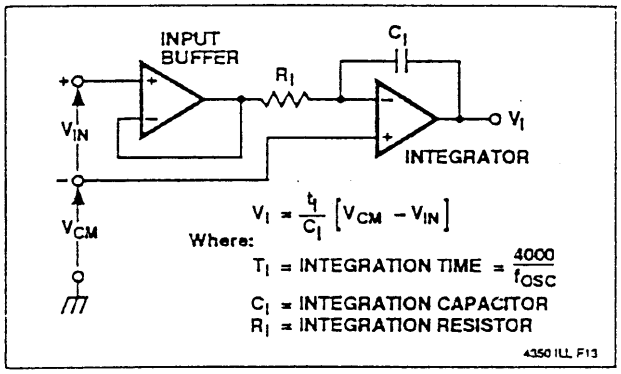


Figure 11 Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} = V_{IN}$)

Differential Reference (V_{REF}^+ (Pin 36), V_{REF}^- (Pin 35))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors being induced by large common-mode voltages C_{REF} should be large compared to stray node capacitance.

The TC7106A/TC7107A circuits have significantly lower analog common temperature coefficient. This potential gives a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is 20 ppm/°C typically.

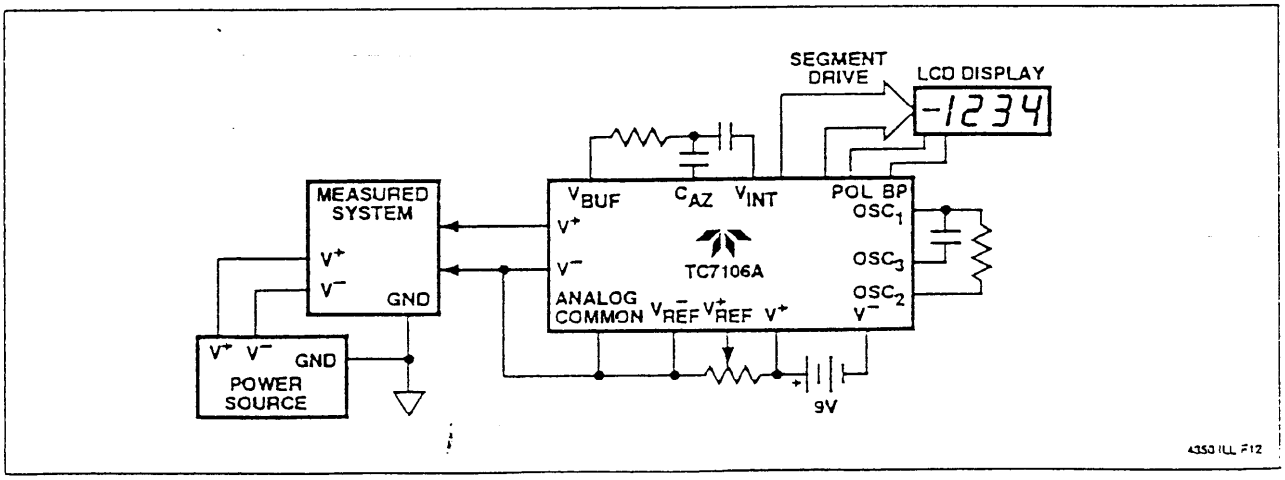


Figure 10 Common-Mode Voltage Removed in Battery Operation with V_{IN}^- = Analog Common

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to the N channel FET capable of sinking 20 mA. This FET will hold the common line at 3.0 V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 µA. Analog common is therefore easily pulled to a more negative voltage (i.e., below $V^+ -3.0$ V).

The TC7106A connects the internal V_{IN}^+ and V_{IN}^- inputs to analog common during the auto-zero cycle. During the reference integrate phase V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converters 86 dB common-mode rejection ratio. In battery operation analog common and V_{IN}^- are usually connected removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference or common point. The TC7106A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TC7106A power source. The analog common potential of $V^+ -3.0$ V gives a 6 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15 Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- >$ 7.0 V) analog common is a very stable potential with excellent temperature stability—typically 20 ppm/°C. This potential can be used to generate the reference voltage. An external voltage reference will be unnecessary in most cases because of the 50 ppm/°C maximum temperature coefficient. See Internal Voltage Reference discussion.

Test (Pin 37)

The test pin potential is 5 V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally generated negative logic supply (Internal Logic Ground) through a 500Ω resistor in the TC7106A. The test pin load should be no more than 1mA .

If test is pulled to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes with the TC7106A. With Test = V^+ the LCD Segments are impressed with a DC voltage which will destroy the LCD.

The test pin will sink about 10 mA when pulled to V^+.

Internal Voltage Reference Stability

The analog common voltage temperature stability has been significantly improved (Figure 12). The "A" version of the industry standard circuits allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 13 shows analog common supplying the necessary voltage reference for the TC7106A/TC7107A.

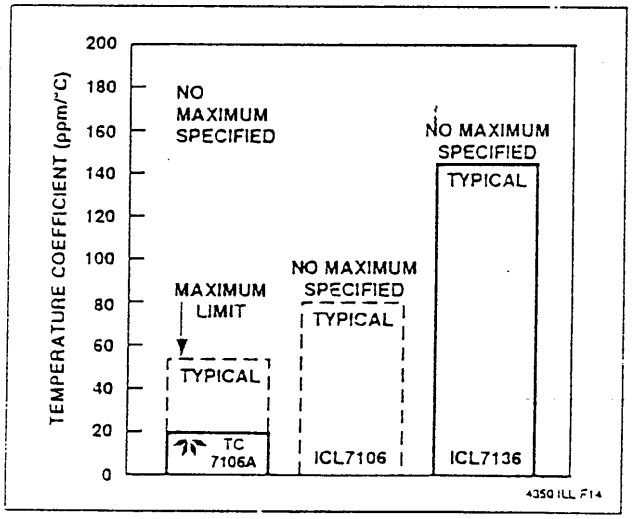


Figure 12 Analog Common Temperature Coefficient

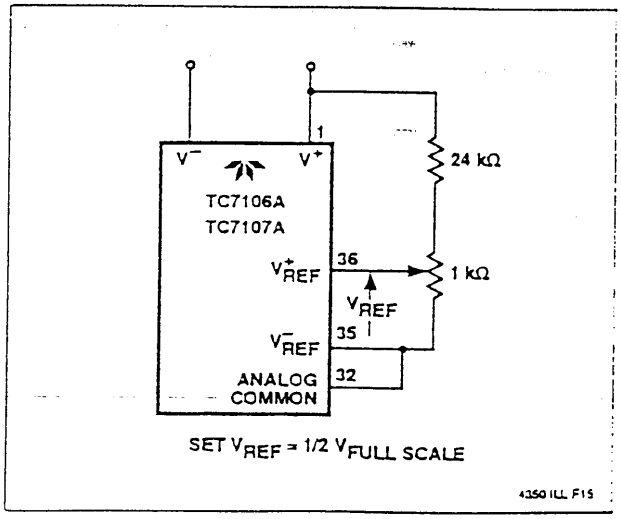


Figure 13 Internal Voltage Reference Connection

Power Supplies

The TC7107A is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors, and an inexpensive IC. (Figure 14)

In selected applications a negative supply is not required. The conditions to use a single +5V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5V.
- An external reference is used.

The TSC7660 DC to DC converter may be used to generate –5 V from +5 V (Figure 15).

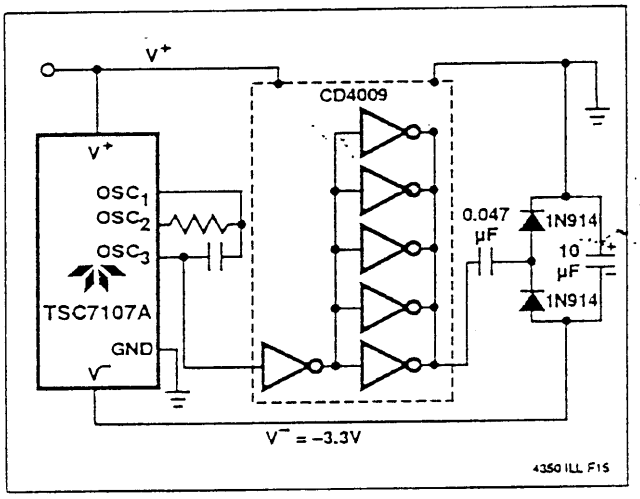


Figure 14 Generating Negative Supply From +5 V

TC7107 Power Dissipation Reduction

The TC7107A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TC7107A package power dissipation is reduced.

Figure 16 is a photograph of a curve-trace display showing the relationship between output current and output voltage for a typical TC7107CPL. Since a typical LED has 1.8 volts across it at 7 mA, and its common anode is connected to +5 V, the TC7107A output is at 3.2 V. (point A on Figure 15). Maximum power dissipation is 8.1 mA x 3.2 V x 24 segments = 622 mW.

Notice, however, that once the TC7107A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B in Figure 16) results in 7.7 mA of LED current,

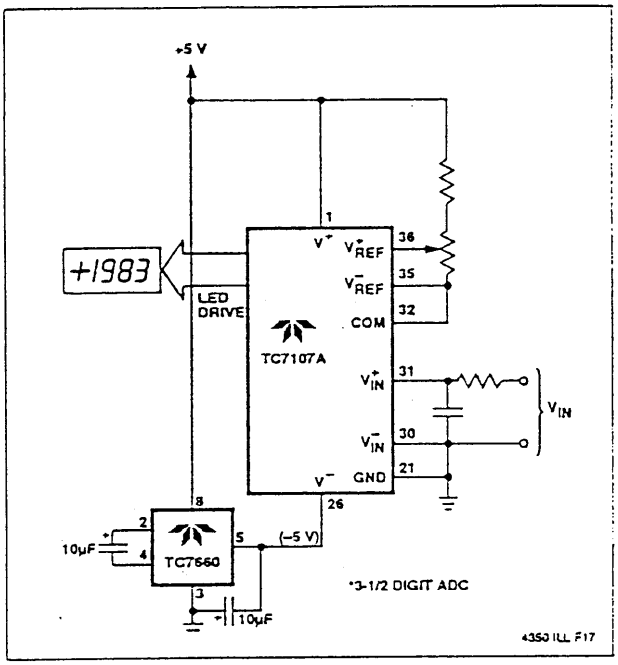


Figure 15 Negative Power Supply Generation with TC7660

only a 5 percent reduction. Maximum power dissipation is only 7.7 mA x 2.5 V x 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA x 2.2 V x 24 = 385 mW).

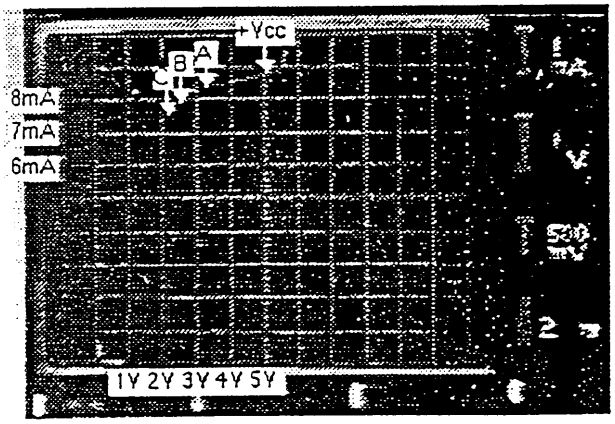


Figure 16 TC7107A Output Current vs Output Voltage

Reduced power dissipation is very easy to obtain. Figure 17 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TC7107A). The resistor will reduce the TC7107A output voltage, when all 24 segments are "ON," to point "C" of Figure 16. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

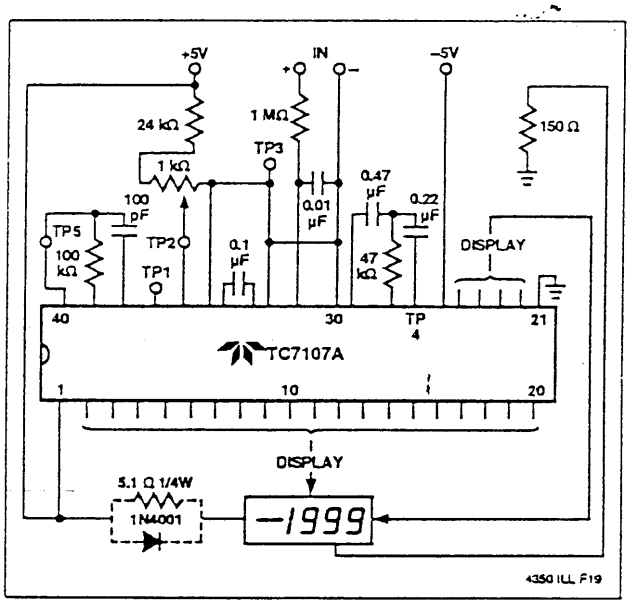


Figure 17 Diode or Resistor Limits Package Power Dissipation

APPLICATIONS INFORMATION
LIQUID CRYSTAL DISPLAY SOURCES

Several LCD manufacturers supply standard LCD displays to interface with the TC7106A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B7098Z LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note: 1. Contact LCD manufacturer for full product listing/specifications.

Light Emitting Diode Display Sources

Several LED manufacturers supply seven segment digits with and without decimal point annunciators for the TC7107A.

Manufacturer	Address	Display Type
Hewlett-Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
And	770 Airport Blvd. Burlingame, CA 94010	LED

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5 V below V^+.

Ratiometric Resistance Measurements

The true differential input and differential reference make ratiometric reading possible. Typically in a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

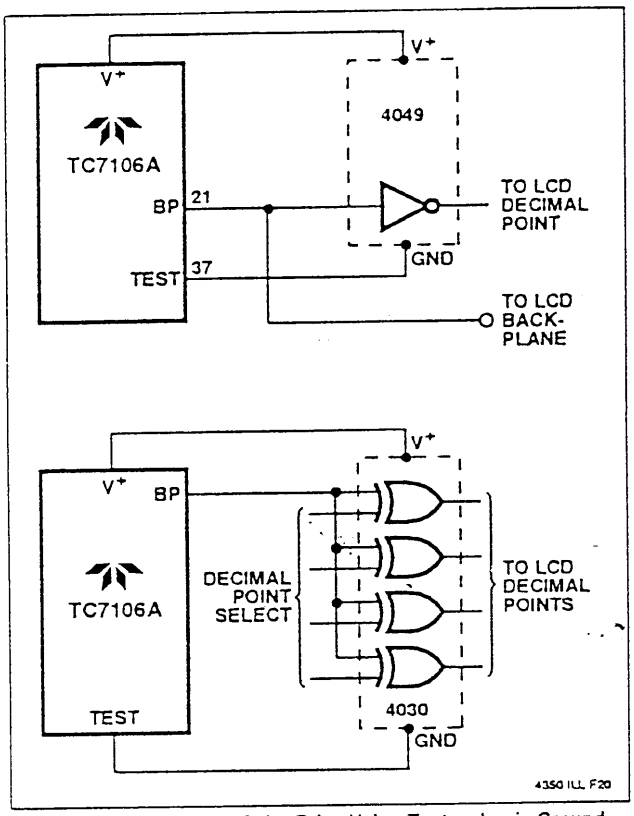


Figure 18 Decimal Point Drive Using Test as Logic Ground

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor is applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥ 2 x R standard.

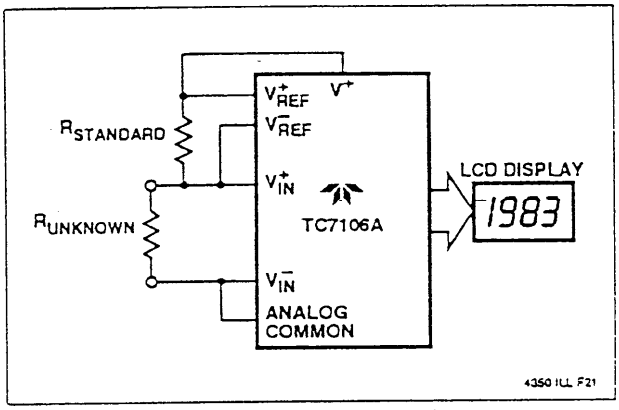


Figure 19 Low Parts Count Ratiometric Resistance Measurement

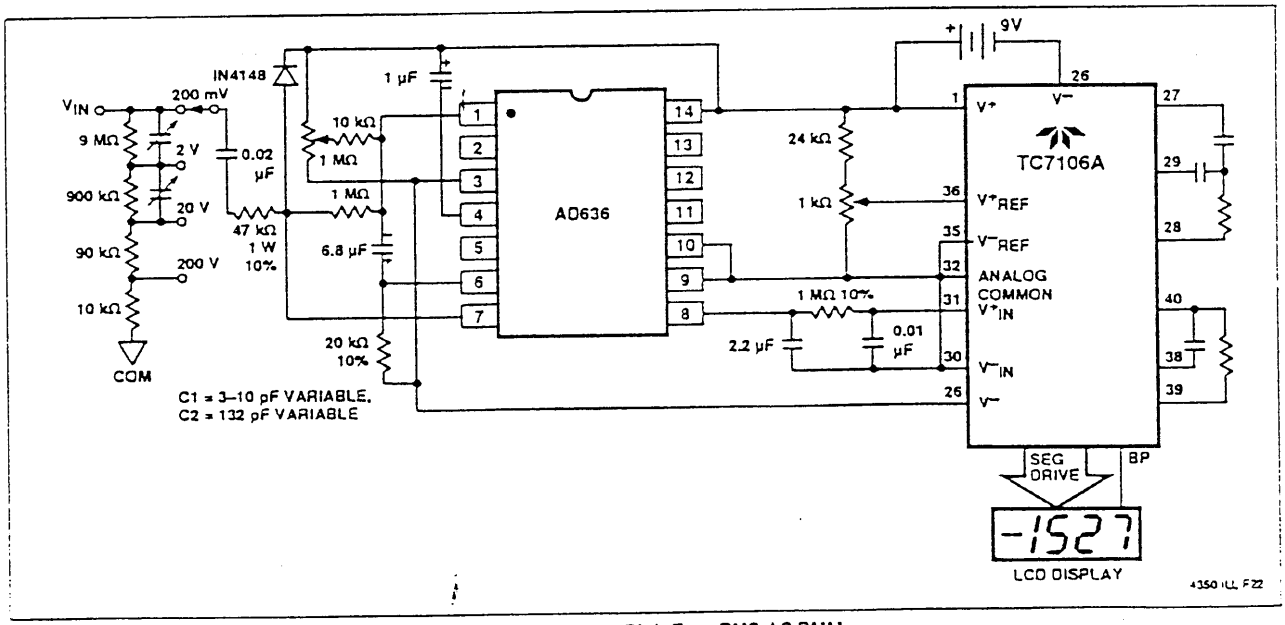


Figure 20 3 1/2 Digit True RMS AC DMM

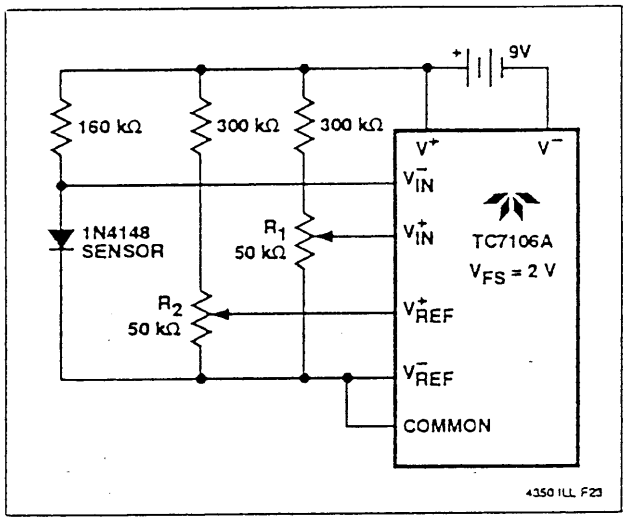


Figure 21 Temperature Sensor

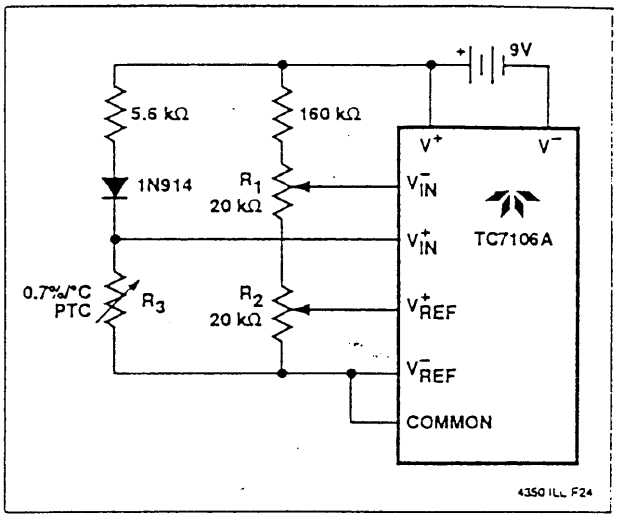


Figure 22 Positive Temperature Coefficient Resistor Temperature Sensor

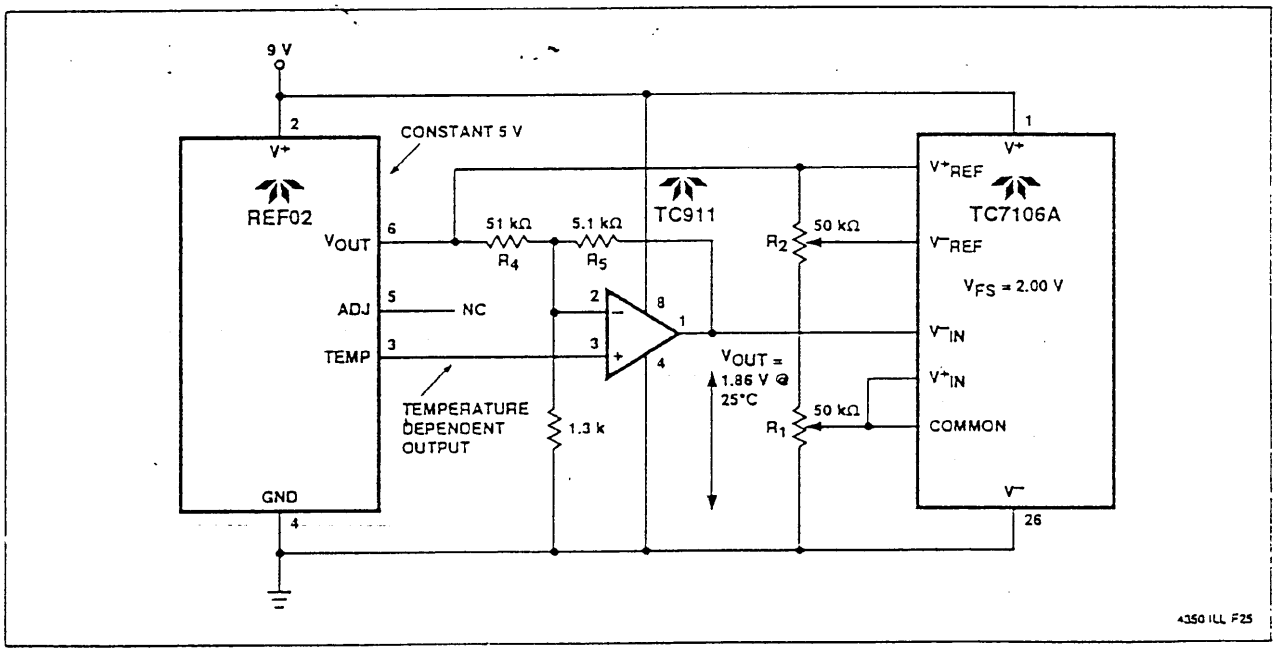


Figure 23 Integrated Circuit Temperature Sensor

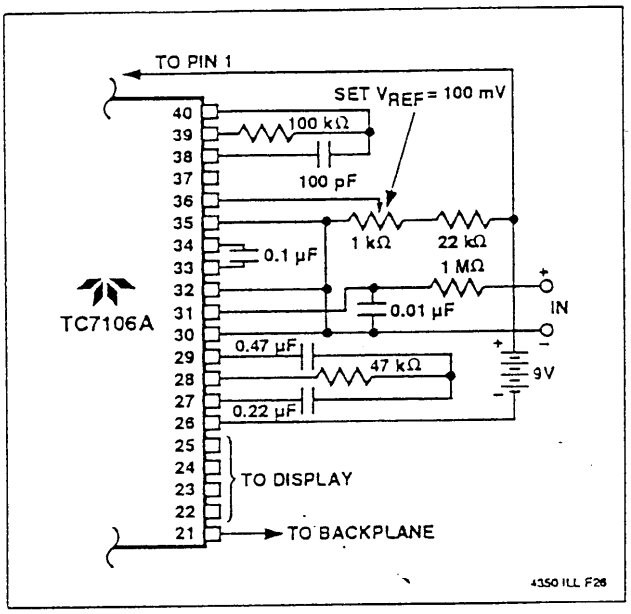


Figure 24 TC7106A Using the Internal Reference. (200 mV Full-Scale, 3 RPS).

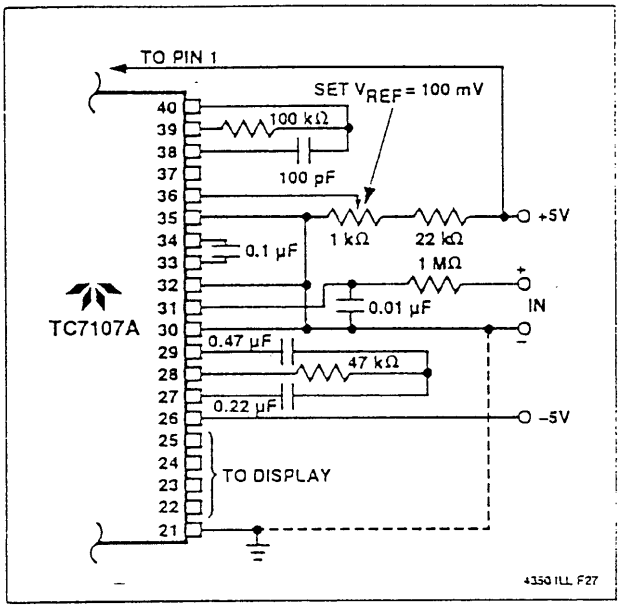


Figure 25 TC7107A Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^- Tied to GND for Single Ended Inputs).

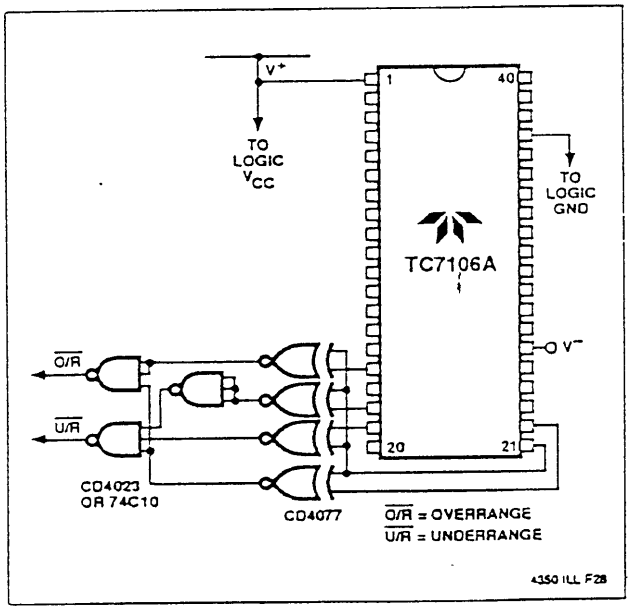


Figure 26 Circuit for Developing Underrange and Overrange Signals from TC7106A Outputs.

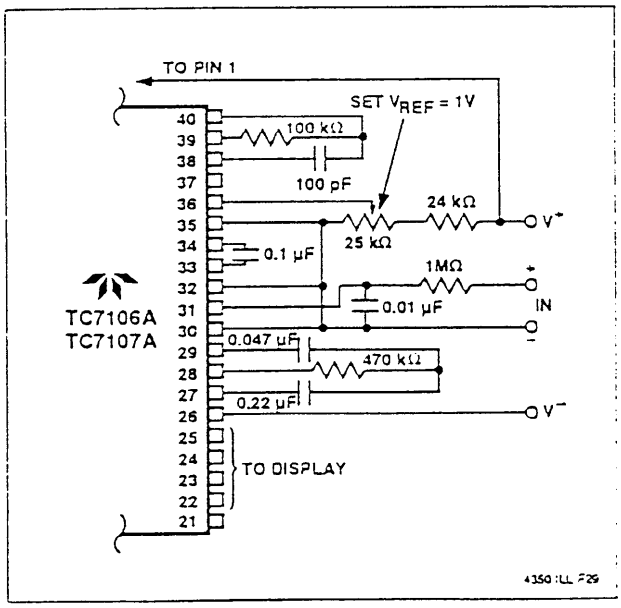


Figure 27 TC7106A/TC7107A: Recommended Component Values for 2.00 V Full-Scale

TC7106/7106A
TC7107/7107A

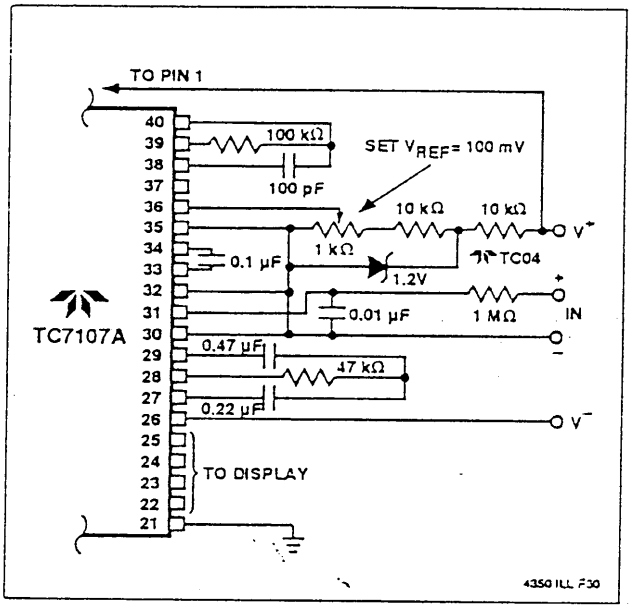


Figure 28 TC7107A With a 1.2 V External Band-Gap Reference. (V^-_{IN} Tied to Common.)

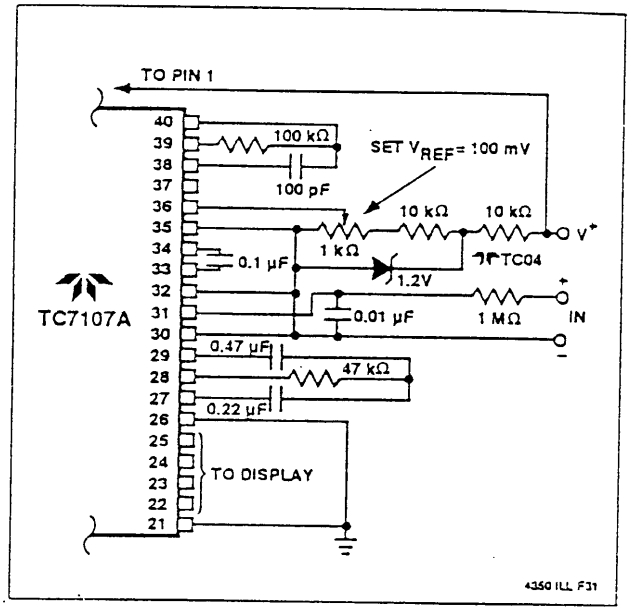


Figure 29 TC7107A Operated from Single +5 V Supply An External Reference Must Be Used in This Application.