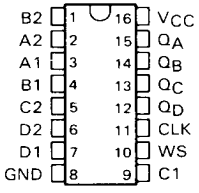
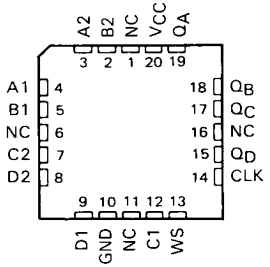
D2661, DECEMBER 1983—REVISED MAY 1986

- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock
- Applications:
  - Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data
  - Implements Separate Registers Capable of Parallel Exchange of Contents, yet Retains External Load Capability
  - Has Universal-Type Register for Implementing Various Shift Patterns, including Compound Left-Right Capability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54AS298 . . . J PACKAGE
SN74AS298 . . . D OR N PACKAGE
(TOP VIEW)



SN54AS298 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

This quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (SN54AS157/SN74AS157 and SN54AS175/SN74AS175) in a single 16-pin package.

When the word-select (WS) input is low, Word 1 (A1, B1, C1, D1 is applied to the flip-flops. A high input to the word-select (WS) will cause the selection of Word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

The SN54AS298 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS298 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

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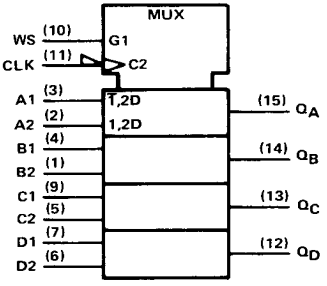
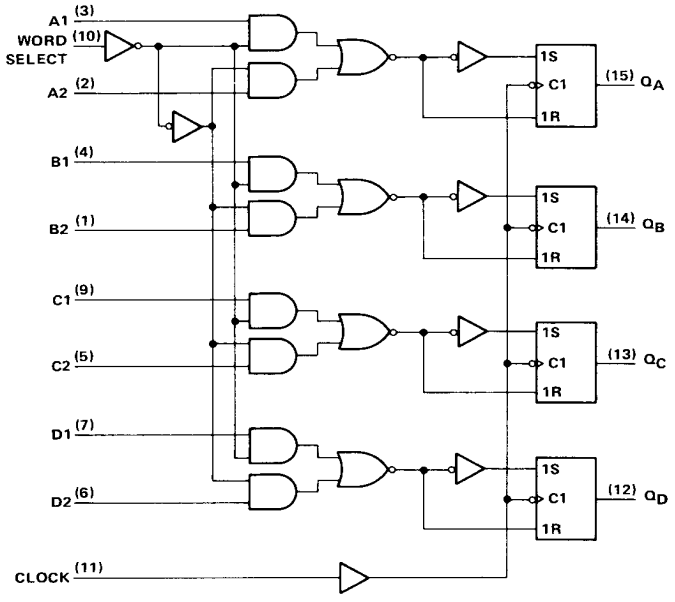
logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS298 . . . . . −55°C to 125°C
SN74AS298 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS298			SN74AS298			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		100	0		100	MHz
t_w	Pulse duration, CLK high or low		5			5			ns
t_{su}	Setup time before CLK ↓	Data	4.5			4.5			ns
		Word Select	13			13			
t_h	Hold time after CLK ↓	Data	3.5			3.5			ns
		Word Select	1			1			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS298			SN74AS298			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1			−1	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	WS	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All other					20			20	
I_{IL}	WS	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.75			−0.75	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	33		21	33	mA
I_{CCL}		V_{CC} = 5.5 V			22	36		22	36	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characterisitcs (see Note 1)

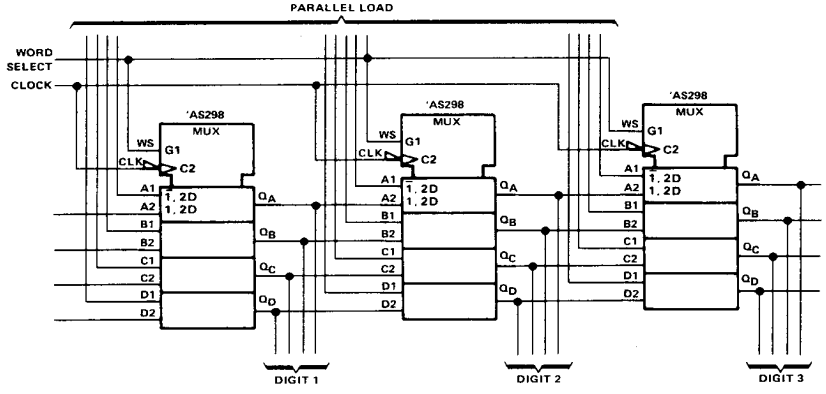
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS298		SN74AS298		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	CLK	Q	2	16	2	9	ns
t_{PHL}			1	12	1	11	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

TYPICAL APPLICATION DATA

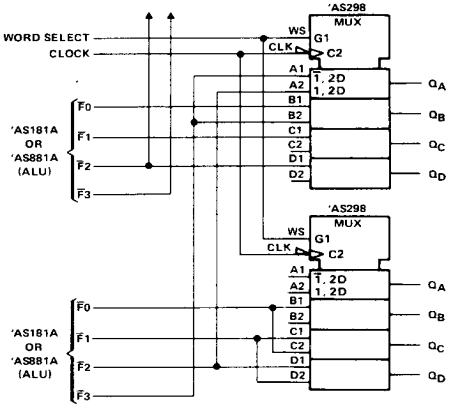
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the 'AS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one-place/two-place shift register.



When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALUs) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

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