

## HIGH FREQUENCY NPN TRANSISTOR ARRAY

## FEATURES

- **TWO BUILT-IN DIFFERENTIAL AMPLIFIER CIRCUITS:** (Each Transistor has  $f_T$  9 GHz)
- **OUTSTANDING  $h_{FE}$  LINEARITY**
- **TWO PACKAGE OPTIONS:**
  - $\mu$ PA102B: Superior thermal dissipation due to studded 14-pin ceramic package
  - $\mu$ PA102G: Reduced circuit size due to 14-pin plastic SOP package for surface mounting

## DESCRIPTION AND APPLICATIONS

The  $\mu$ PA102 is a user configurable Silicon bipolar transistor array consisting of two separate differential amplifiers. It is available in a surface mount (14-pin plastic SOP) package and a 14-pin ceramic package. Typical applications include: pulse pattern generators, oscillators, differential amps, high speed comparators, electro-optic signal processing up to 1 Gigabits/second, and advanced cellular phone systems.

## ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA102B-E1	14-pin ceramic package
$\mu$ PA102G-E1	14-pin plastic SOP (225 mil)

ABSOLUTE MAXIMUM RATINGS ( $T_A = +25^\circ\text{C}$ )

SYMBOLS	PARAMETERS	UNITS	RATINGS
$V_{CBO}^*$	Collector to Base Voltage	V	15
$V_{CEO}^*$	Collector to Emitter Voltage	V	6
$V_{EBO}^*$	Emitter to Base Voltage	V	2.5
$I_C^*$	Collector Current	mA	40
$P_T$	Power Dissipation		
	$\mu$ PA102B $\mu$ PA102G	mW mW	650 350
$T_J$	Junction Temperature		
	$\mu$ PA102B $\mu$ PA102G	$^\circ\text{C}$ $^\circ\text{C}$	200 125
$T_{STG}$	Storage Temperature		
	$\mu$ PA102B $\mu$ PA102G	$^\circ\text{C}$ $^\circ\text{C}$	-55 to +200 -55 to +125

\* Absolute maximum ratings for each transistor.

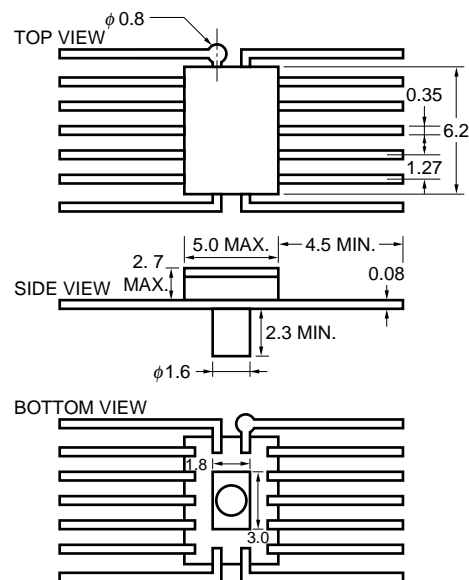
## Caution electro-static sensitive devices

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

PACKAGE DIMENSIONS (UNIT: mm)

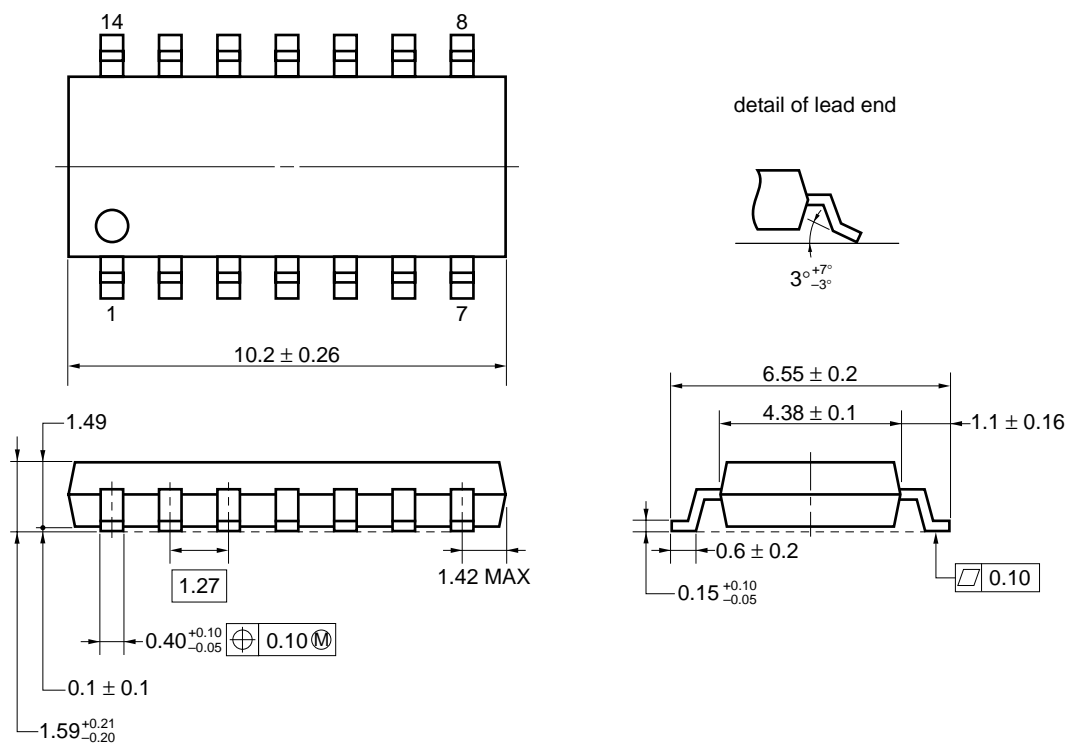
μPA102B

14 PIN CERAMIC PACKAGE



μPA102G

★ 14 PIN PLASTIC SOP (225 mil)



**NOTE** Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

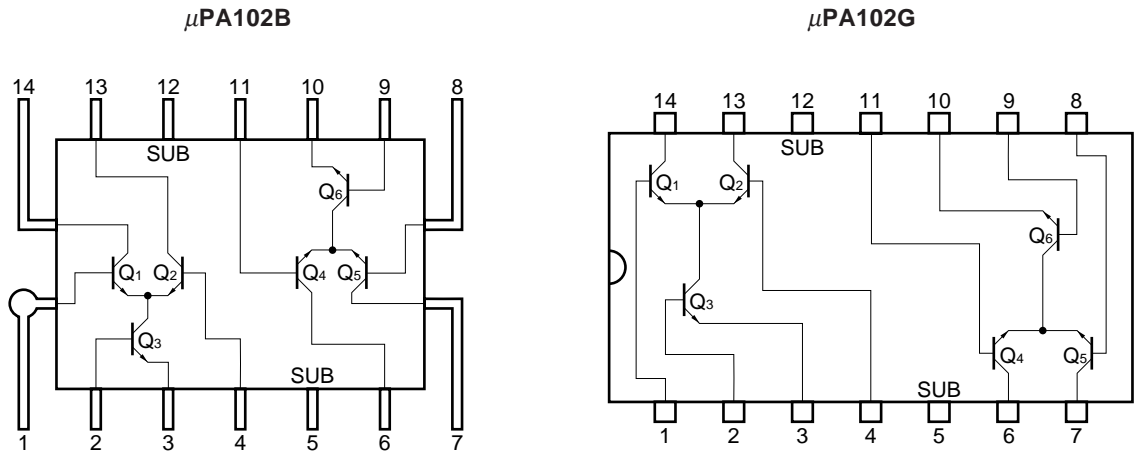
See connection diagram for description of leads.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise specified T<sub>A</sub> = +25 °C μPA102B, μPA102G common)

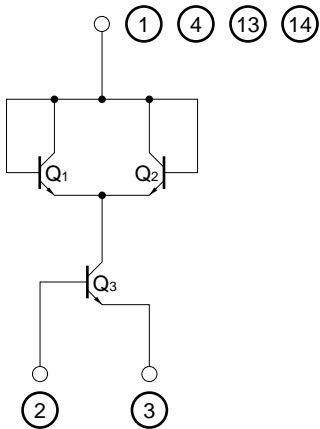
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN.	TYP.	MAX.
I <sub>CBO</sub>	Collector Cutoff Current at V <sub>CB</sub> = 5 V, I <sub>E</sub> = 0 (Q1, Q2, Q4, Q5)	μA			1.0
I <sub>EBO</sub>	Emitter Cutoff Current at V <sub>EB</sub> = 1 V, I <sub>C</sub> = 0 (Q3, Q6)	μA			1.0
h <sub>FE</sub>	Direct Current Amplification at V <sub>CE</sub> = 3 V, I <sub>C</sub> = 1 mA (Q3, Q6)		40	100	250
h <sub>FE1</sub> /h <sub>FE2</sub>	Direct Current Amplification Ratio at V <sub>CE</sub> = 3 V, I <sub>C</sub> = 1 mA, (Q3, Q6)		0.9	1.0	1.1
C <sub>CB</sub>	Collector to Base Capacitance at V <sub>CB</sub> = 3 V, f = 1 MHz (Q1, Q2, Q4, Q5)	pF		0.9	1.8
C <sub>EB</sub>	Emitter to Base Capacitance at V <sub>EB</sub> = 0, f = 1 MHz (Q3, Q6)	pF		1.4	2.8
C <sub>CS</sub>	Collector/Substrate Capacitance at V <sub>CS</sub> = 3 V, f = 1 MHz (Q1, Q2, Q4, Q5)	pF		1.4	2.8
f <sub>T</sub>	Gain Bandwidth Product* at V <sub>CE</sub> = 3 V, I <sub>C</sub> = 10 mA	GHz		9.0	

\* Measured by installing a single transistor in a Micro-X package: the value shown is a reference value.

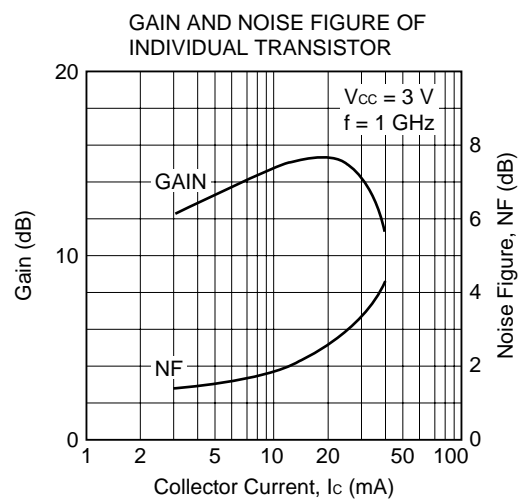
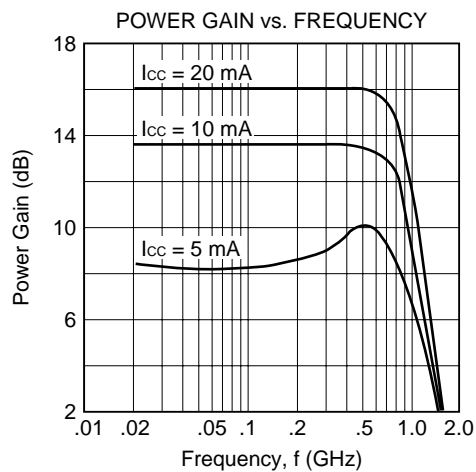
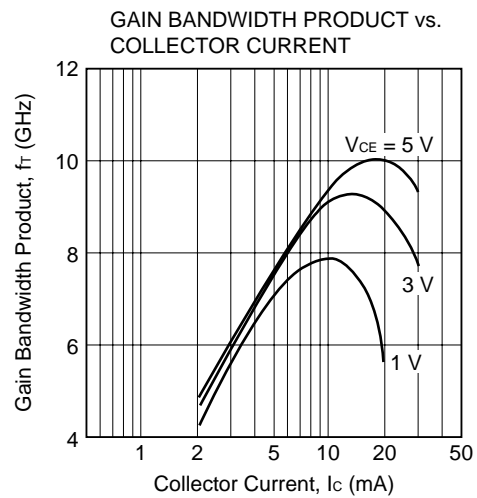
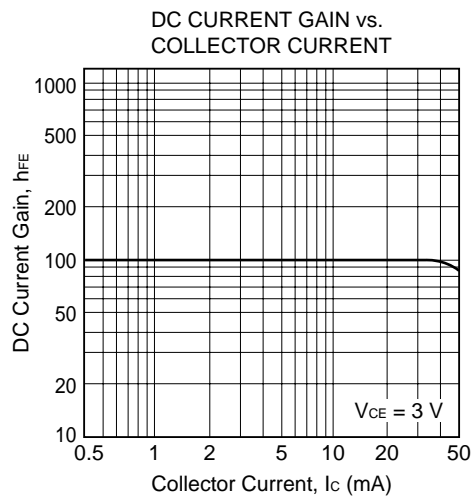
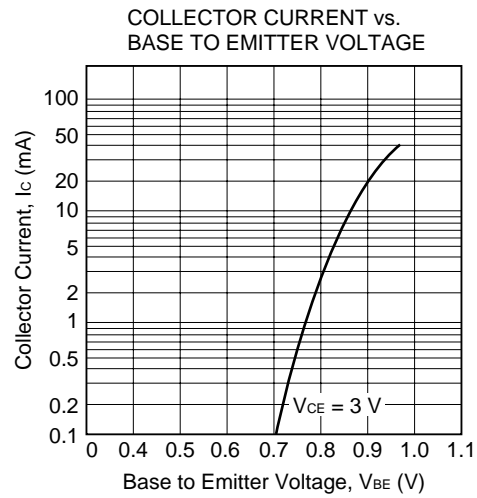
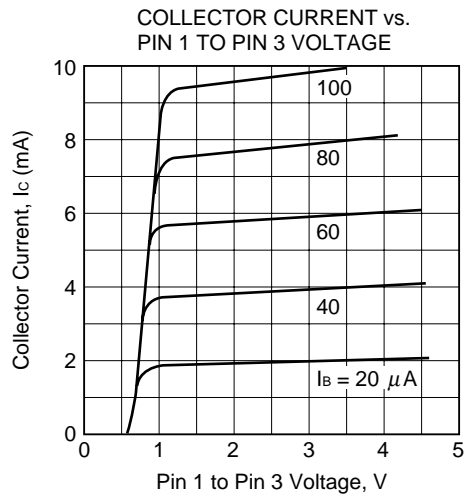
**CONNECTION DIAGRAM** (Top View)



**TEST CIRCUIT SCHEMATIC\*** (For Electrical Characteristics Measurements excluding f<sub>T</sub>)



\* See performance characteristics for voltage.

TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A = +25^\circ\text{C}$ )

**NOTES ON CORRECT USE**

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired operation).
- (3) Design circuits connected Sub pin to the lowest voltage to prevent latch-up.
- (4) Design circuits as each pin voltage difference within 15 V maximum.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

 **$\mu$ PA102G**

Soldering process	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C), Time: 2 times, Limited days: no. <sup>Note</sup>	IR35-00-2
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 2 times, Limited days: no. <sup>Note</sup>	VP15-00-2
Wave soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no. <sup>Note</sup>	WS60-00-1
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 3 s./pin Limited days: no. <sup>Note</sup>	

 **$\mu$ PA102B**

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 10 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: None	
Partial heating method	Terminal temperature: 260 °C or below, Flow time: 10 seconds or below, Exposure limit*: None	

**Note** It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

**Caution** The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]

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