TS4305

Synchronous FET Controller

POWER MANAGEMENT

Features

- Current-sense control for low or high-side synchronous rectifiers
- Rectifier turn on/off thresholds set with external resistors
- Minimum ON and OFF time to minimize GATE turn-on oscillation
- UVLO configurable to 9V or 4V
- Wide supply range 4.5V to 24V
- Gate drive internally limited to 5V or 10V
- 2A sink, 1A source gate drive
- 2mm x 2mm DFN-8 & 4mm x 5mm SOIC-8 packages
- Product is lead-free, Halogen Free, RoHS / WEEE compliant

Applications

- LLC converters
- Flyback converters

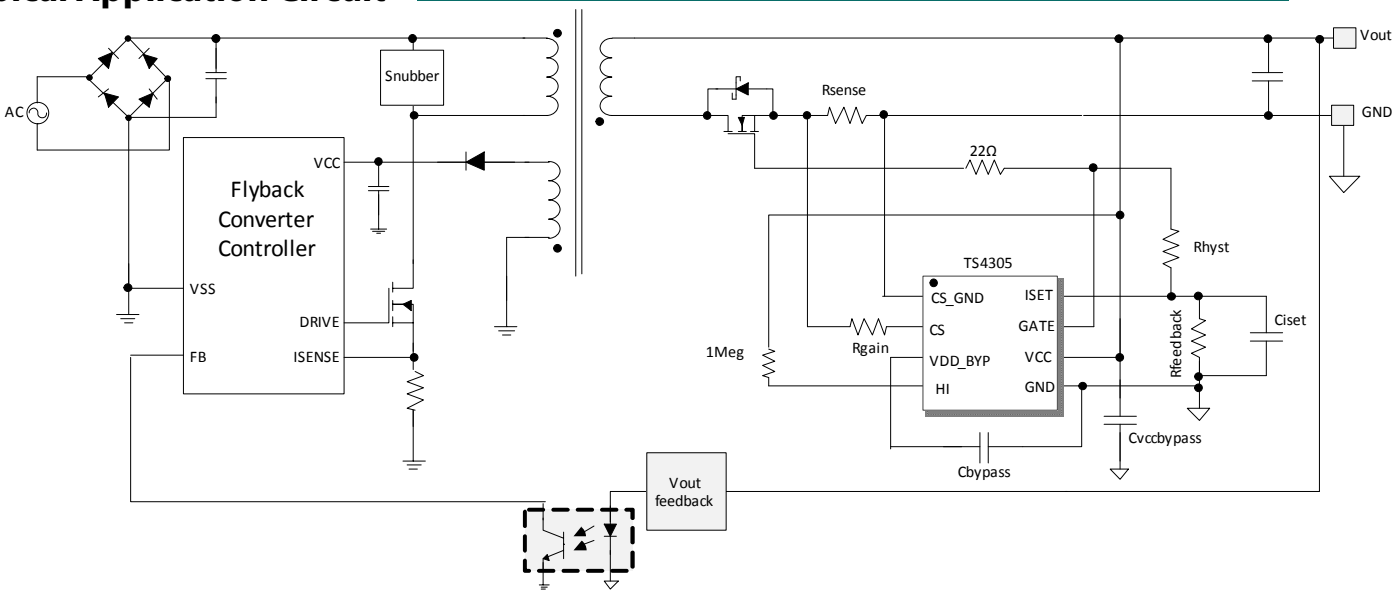
Description

TS4305 is a synchronous rectifier controller for AC-DC power supply's secondary side rectification.

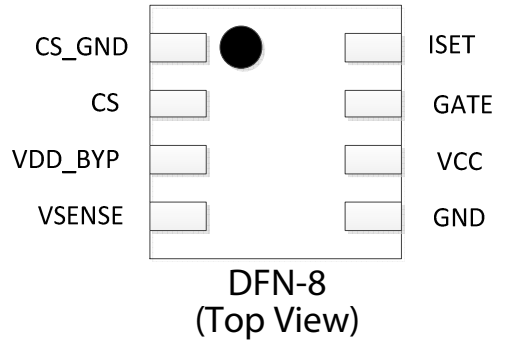
Specifications

- Drives low or high side N-channel MOSFET
- Sync-FET control based on current sensing in low or high-side sense resistor
- -40°C to +125°C T_J operation
- Operation to 24V
- 2A/1A sink/source gate drive
- 5 V or 10V gate drive capability
- 100ns propagation delay between current sense to GATE drive
- 180µA (typical) quiescent current in low power mode
- Under voltage lock out protection
- Over temperature shut down (TSD) protection

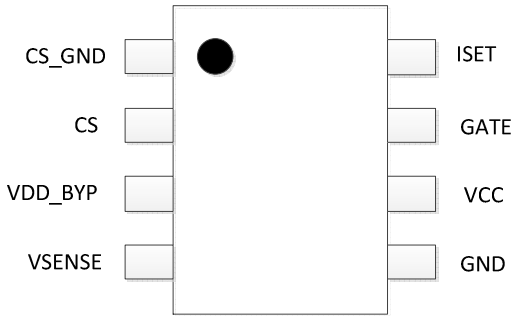
Typical Application Circuit



Pin Configuration



DFN-8
(Top View)

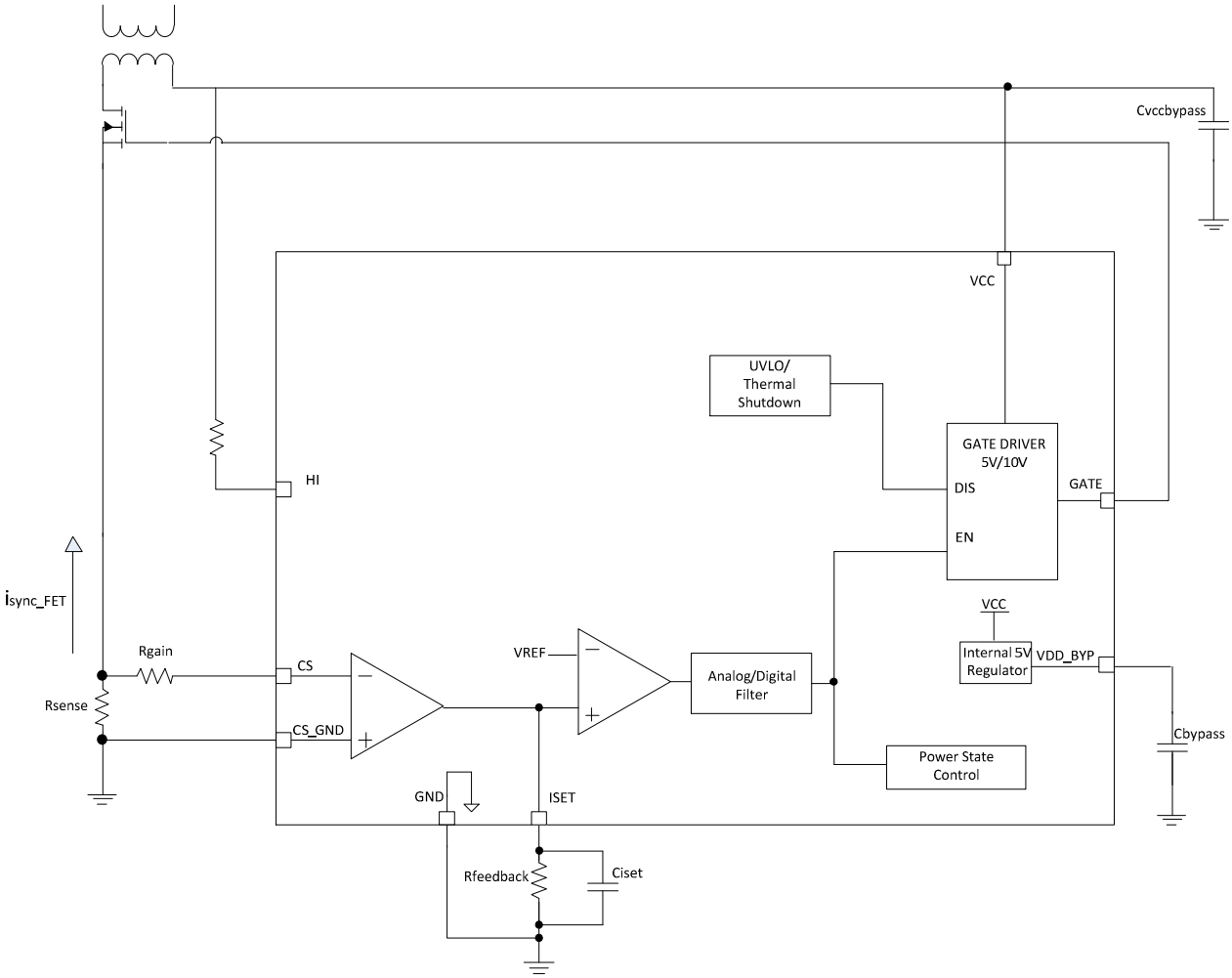


SOIC-8
(Top View)

Pin Configuration

DFN-8/SOIC-8 Pin #	Pin Name	Function	Description
1	CS_GND	Current Sense	Current sense resistor high-side terminal
2	CS	Current Sense	Current sense resistor low-side terminal
3	VDD_BYP	Power Bypass	External bypass capacitor for internal 5V VDD supply
4	HI	Vendor Test Mode	Tie to VCC through 1Meg resistor
5	GND	Ground	Circuit Common
6	VCC	Power Input	Supply voltage
7	GATE	FET Gate Drive	Gate drive, regulated voltage swing
8	ISET	Current Sense Output	Current sense in voltage form using Rfeedback

Functional Block Diagram



Functional Diagram Configured in QR Flyback application

Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted (1, 2)

Parameter	Value	Unit
VCC	-0.3 to 26	V
GATE	-0.3 to 12	V
ISET, CS, HI, VDD_BYP	-0.3 to 5.5	V
Electrostatic Discharge – Human Body Model	+/-2k	V
Electrostatic Discharge – Charge Device Model	+/-500	V
Reflow or solder Temperature (soldering, 10 seconds)	260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND.

Thermal Characteristics DFN-8

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Air (1)	70	°C/W
T_{STG}	Storage Temperature Range	-65 to 150	°C
$T_{J\,MAX}$	Maximum Junction Temperature	150	°C
T_A	Operating Ambient Temperature Range	-20 to 85	°C
T_J	Operating Junction Temperature Range	-20 to 125	°C

(1) Assumes 8LD DFN mounted on a 4-layer FR4 2S2P JEDEC board as per JESD51-7 with 13.5 inch^2 of 1 oz Cu.

Thermal Characteristics SOIC-8

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Air (1)	153	°C/W
T_{STG}	Storage Temperature Range	-65 to 150	°C
$T_{J\,MAX}$	Maximum Junction Temperature	150	°C
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Operating Junction Temperature Range	-40 to 125	°C

(1) Assumes 8LD SOIC mounted on a 1-layer FR4 2S2P JEDEC board as per JESD51-7 with 13.5 inch^2 of 1 oz Cu.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Input Operating Voltage	4.5		24	V
$CS_{dv/dt}$	CS Input Slew Rate			10	V/ms
CS_{Input}	CS Input voltage with respect to GND			100	mV
$C_{VCCBYP1}$	VCC Bypass Capacitor, appropriate voltage rating per VCC		10		µF
$C_{VCCBYP2}$	VCC Bypass Capacitor, appropriate voltage rating per VCC		10		pF
C_{byp}	Internal 5V VDD Bypass Capacitor		1		µF
F_{switch}	Maximum Gate Drive Switching Frequency			150	kHz

Electrical Characteristics

T_J = 25°C for typical, T_J = -40°C to 125°C, unless otherwise noted

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Current Sense Amplifier						
VREF	2.0V Comparator reference	T_J=0°C to +85°C	1.99	2	2.01	V
		T_J=-40°C to +125°C	1.95	2	2.05	V
Supply						
VCC	Supply voltage		4.5		24	V
I_{supply}	Quiescent supply current	CS amp = Off during lockout time period		180	300	µA
V_{LGC}	Internal LV supply for logic			5		V
T_{SD}	Thermal shutdown temperature(1)			135		°C
Under Voltage Lock Out						
V_{UVLO_ON}	UV Turn On Threshold (VCC)	10V Gate Drive	8	9	10	V
		5V Gate Drive	3.7	4.2	4.7	V
V_{UVLO_OFF}	UV Turn Off Threshold (VCC)	10V Gate Drive	7.5	8.5	9.5	V
		5V Gate Drive	3.4	3.9	4.4	V
V_{UVLO_hyst}	UVLO hysteresis	10V Gate Drive	0.35		1.0	V
		5V Gate Drive	0.25		0.65	V
Gate Drive						
V_{GATE}	Gate drive voltage	10V Gate Drive, VCC > 13V	7.75	10	13	V
		5V Gate Drive, VCC > 13V	4.3	5	6.5	V
R_{DRVHI}	Gate drive source resistance	VCC>13V, Gate=10V, T_J=25°C, IL=50mA		7.2	17	Ω
		VCC=4.5V, Gate=5V, T_J=25°C, IL=100mA		8.1	11	Ω
R_{DRVLO}	Gate drive sink resistance	VCC>13V, Gate=10V, T_J=25°C		2.1	3.1	Ω
		VCC=4.5V, Gate=5V, T_J=25°C		1.9	2.9	Ω
t_{prop_dly}	Propagation delay from CS to GATE	-20mV step, R_{sense}=5mΩ, R_{gain}=5Ω, $R_{feedback}$=10kΩ		53		ns
$Ton_{\_pulse}$	Minimum gate ON pulse width		0.8	1.3	1.8	µs
$Toff_{blanking}$	Minimum gate OFF blanking width		1.0	2.3	4.6	µs

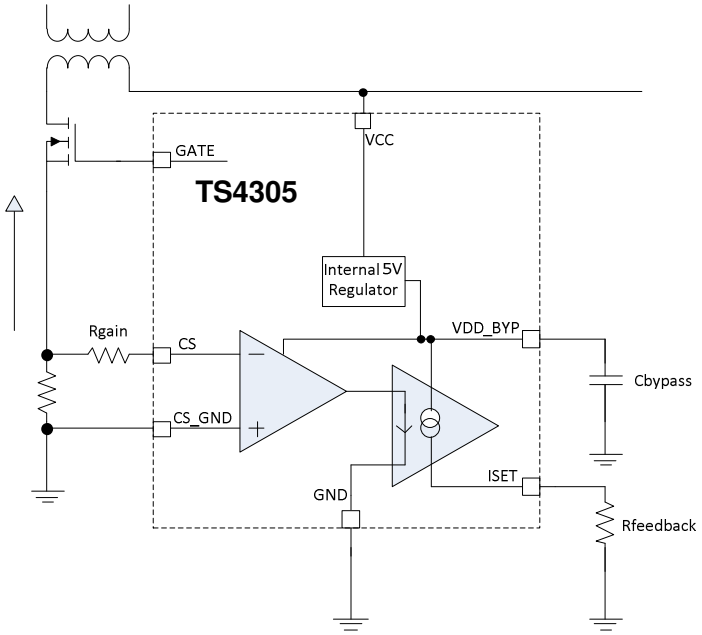
(1) Not tested in production

Detailed Description of Operation

TS4305 is intended for use on the secondary side of a power supply to drive a synchronous MOSFET. Unlike traditional synchronous MOSFET controllers, the TS4305 uses an architecture that synchronizes the rectification FET with the secondary-side current as opposed to the secondary side voltage. Because secondary side current and voltage are not necessarily in phase, the zero current detection method yields to a more efficient operation as opposed to operation with voltage detection only.

Synchronous Rectifier Control

The TS4305 uses a current mirror in conjunction with a high-sensitivity, low-offset voltage op-amp specifically designed for sensing voltages near the low-side supply rail. This op-amp operates over a small range of input voltage suited specifically for converting the voltage across a low-ohmic sense resistor to current. The equivalent circuit is shown below with typical values for external components:



In the above figure, the syncFET current flows through an external 5mΩ. There is also an external gain resistor Rgain = 5Ω and a feedback resistor Rfeedback = 10kΩ. The amplifier inside the TS4305 holds the voltage at the CS pin close to the GND pin over a small operating range in which i_{sync_FET} is positive. Over this operating range, the voltage at ISET will be equal to (i_{sync_FET}x5mΩ)x(10kΩ/5Ω).

TS4305 contains a comparator that compares the voltage at ISET to an internal reference which is set to 2.0V at T_J=25°C. In the example shown above, when VREF = 2V, the current trip level would be 200mA. This level can be adjusted by changing Rsense, Rgain, and Rfeedback.

A hysteresis resistor can also be connected between the gate drive output and ISET to provide hysteresis in the ON/OFF trip values. In this case, the gate turn on is expected when I_{sync_FET} is greater than:

$$\mathrm{Isync}_{\mathrm{FETon}} \gtrsim \frac{2 * Rgain}{(Rfeedback||Rhysteresis) * Rsense}$$

Using the example values Rgain = 5Ω, Rsense=5mΩ, Rfeedback = 10kΩ, Rhysteresis=100kΩ, $\mathrm{Isync}_{\mathrm{FETon}} \gtrsim 220mA$.

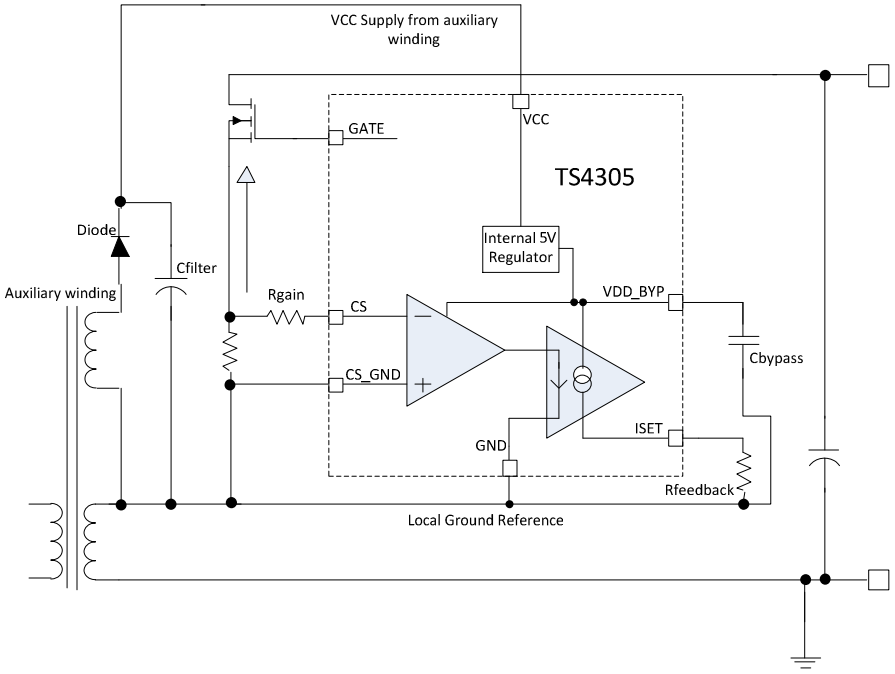
The gate will turn off when I_{sync_FET} falls below the level according to:

$$\mathrm{Isync_{FEToff}} \lesssim \frac{\left[\left(\frac{2.0}{Rfeedback} - \frac{Vgate - 2.0}{Rhysteresis}\right) * Rgain\right]}{Rsense}$$

Which yields $\mathrm{Isync_{FEToff}} \lesssim 120mA$ using the same example values with the Vgate=10V gate drive option.

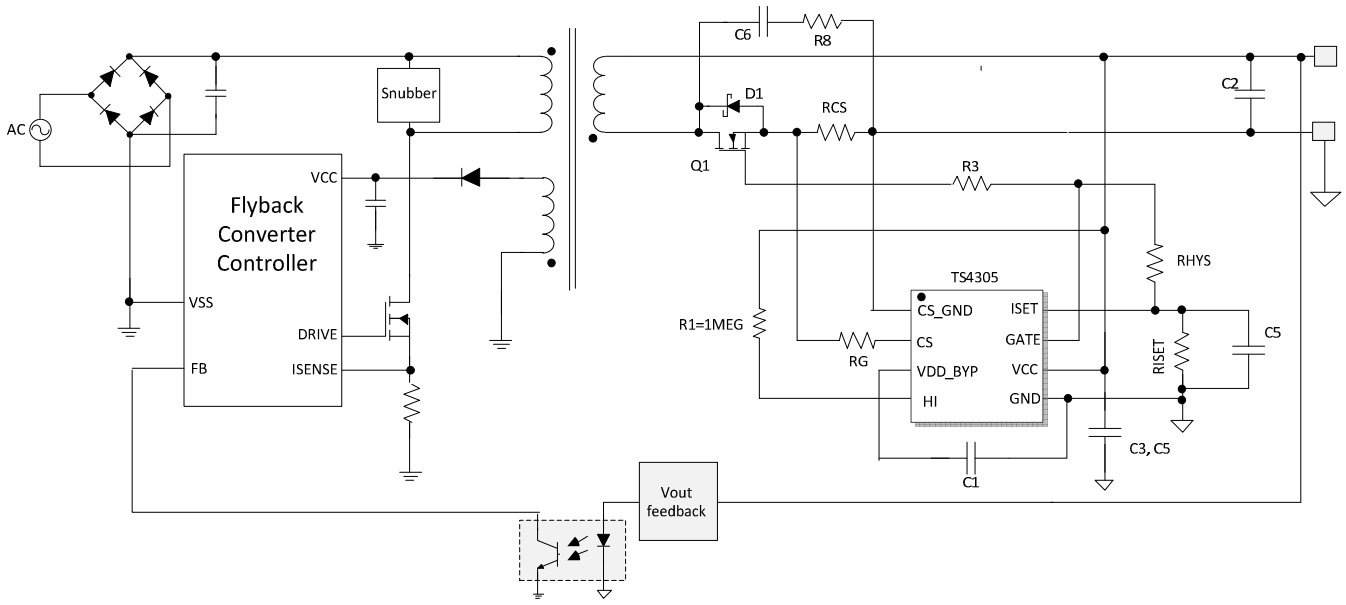
If the signal frequency on the ISET pin is above approximately 200kHz at 27°C (~150kHz at -40°C and ~300kHz at 125°C), the gate driver output will latch low to prevent the synchronous FET from operating. This condition is maintained until VCC is power cycled.

TS4305 can also be configured for sensing voltages on the high-side supply rail. One possible implementation can be accomplished by powering TS4305 through an auxiliary winding and diode-capacitor filter as shown below. Alternative charge pump schemes can also be contemplated.



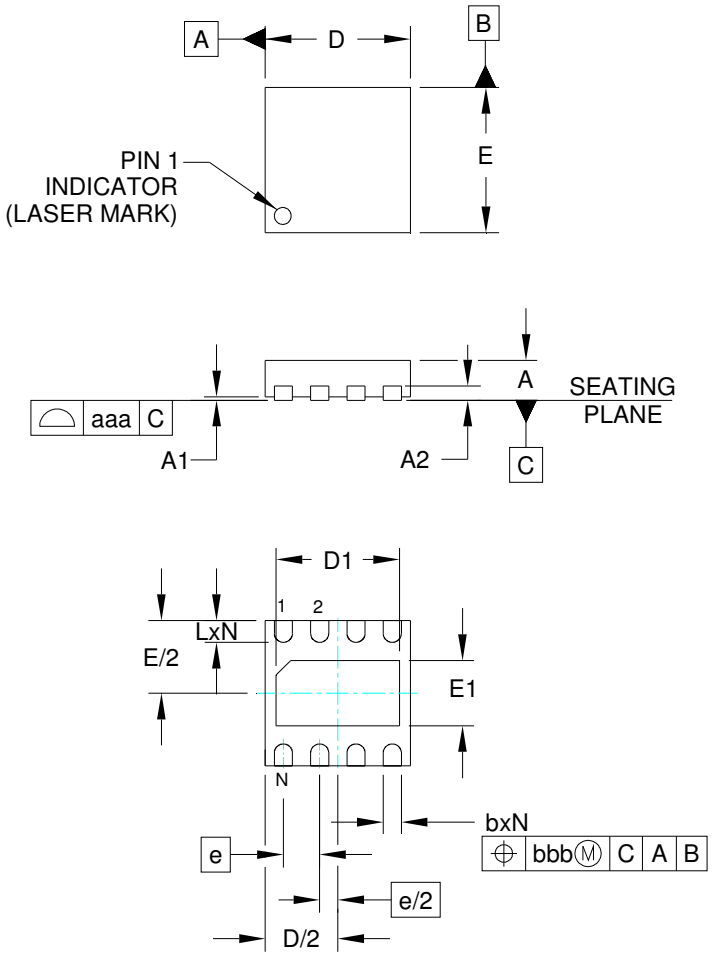
High-side Rectification with auxiliary winding and diode-capacitor filter to power TS4305

Application Schematic



Component	Schematic Value	Notes
R1	1MegΩ	HI pin tie off to VCC
R3	2Ω	Gate resistor
R8	10Ω	Snubber resistor, sized for proper power
RCS	5mΩ	Sense resistor
RG	5.1Ω	Rgain resistor
RISET	10kΩ	Iset resistor
RHYS	100kΩ	Hysteresis resistor
C1	1µF	Internal 5V filter capacitor
C2	10µF	25V VCC filter capacitor
C3	22pF	25V VCC filter capacitor
C5	10µF	25V VCC filter capacitor
C6	1nF	Snubber capacitor, rated for proper Vds
Q1		Power NMOS, with proper Vds rating
D1		100V schottky diode
U1		TS4305 DFN/SOIC, 5V or 10V Gate Drive

Package Drawing: 2.0 x 2.0 mm MLPD(DFN), 8 lead



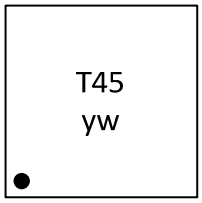
DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		(0.20)	
b	0.18	0.25	0.30
D	1.90	2.00	2.10
D1	1.55	1.70	1.80
E	1.90	2.00	2.10
E1	0.75	0.90	1.00
e		0.50 BSC	
L	0.20	0.30	0.40
N		8	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

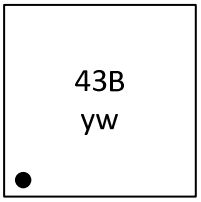
Package Marking: 2.0 x 2.0 mm MLPD(DFN), 8 lead

Top Mark



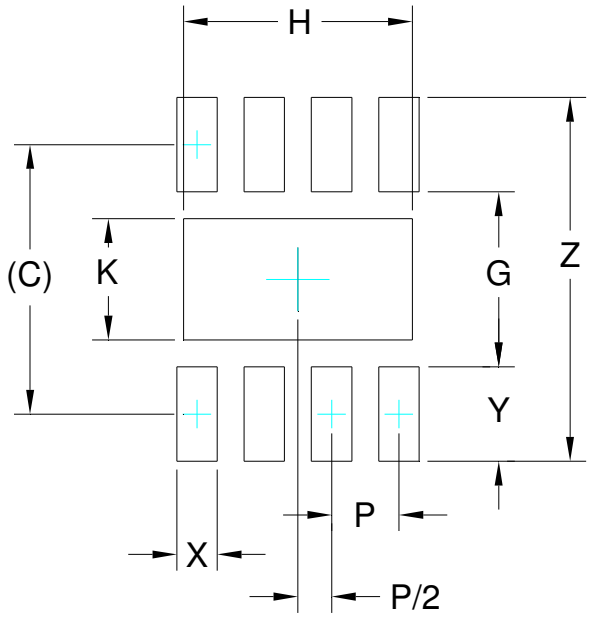
TS4305AMLTRT (2.0 x 2.0 mm MLPD 8 lead):
T45 = Part Number
yw = Date Code

Top Mark



TS4305BMLTRT (2.0 x 2.0 mm MLPD 8 lead):
43B = Part Number
yw = Date Code

Landing Pattern: 2.0 x 2.0 mm MLPD(DFN), 8 lead

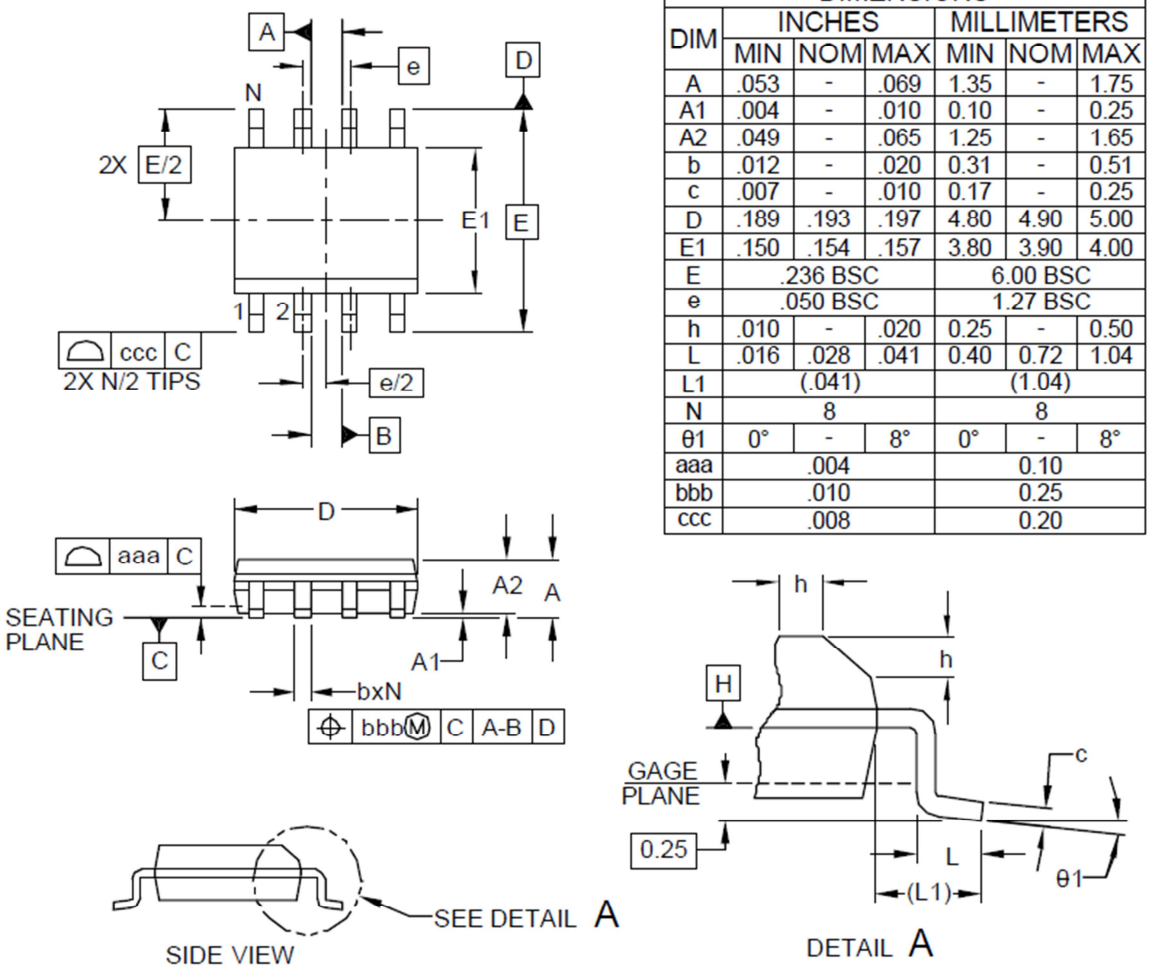


DIMENSIONS	
DIM	MILLIMETERS
C	(2.00)
G	1.30
H	1.70
K	0.90
P	0.50
X	0.30
Y	0.70
Z	2.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Package Drawing: SOIC-8



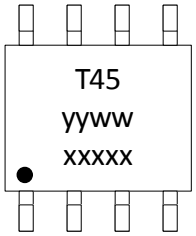
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

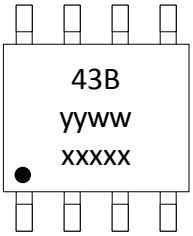
Package Marking: SOIC-8

Top Mark



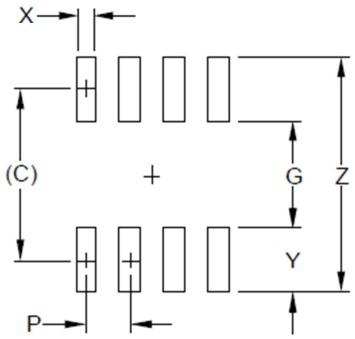
TS4305ASTRT (SOIC 8 lead):
T45 = Part Number
yyww = Date Code
xxxxx = Semtech Lot No.

Top Mark



TS4305BSTRT (SOIC 8 lead):
43B = Part Number
yyww = Date Code
xxxxx = Semtech Lot No.

Landing Pattern: SOIC-8



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

Ordering Information

Device Part Number	Description	Package
TS4305AMLTRT	5V Gate Drive, 8ms lockout period	MLPD(DFN)-8 2x2mm Tape & Reel (3,000 parts/reel)
TS4305BMLTRT	10V Gate Drive, 8ms lockout period	MLPD(DFN)-8 2x2mm Tape & Reel (3,000 parts/reel)
TS4305ASTRT	5V Gate Drive, 8ms lockout period	SOIC-8 Tape & Reel (2,500 parts/reel)
TS4305BSTRT	10V Gate Drive, 8ms lockout period	SOIC-8 Tape & Reel (2,500 parts/reel)

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