

74F109

Dual JK Positive Edge-Triggered Flip-Flop

General Description

The F109 consists of two high-speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D-type flip-flop (refer to F74 data sheet) by connecting the J and K inputs.

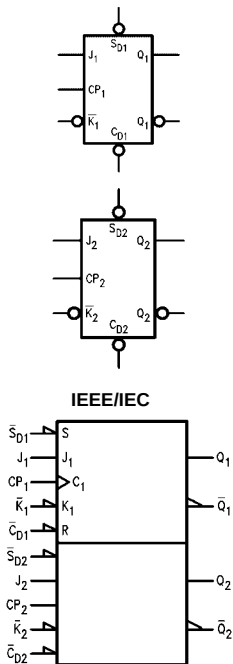
- Asynchronous Inputs:
- LOW input to $\overline{S}_D$ sets Q to HIGH level
 - LOW input to $\overline{C}_D$ sets Q to LOW level
 - Clear and Set are independent of clock
 - Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Ordering Code:

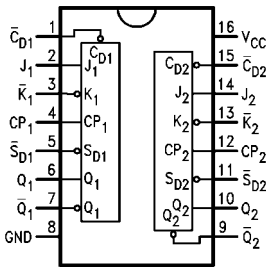
Order Number	Package Number	Package Description
74F109SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F109SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F109PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



74F109 Dual JK Positive Edge-Triggered Flip-Flop

Truth Table

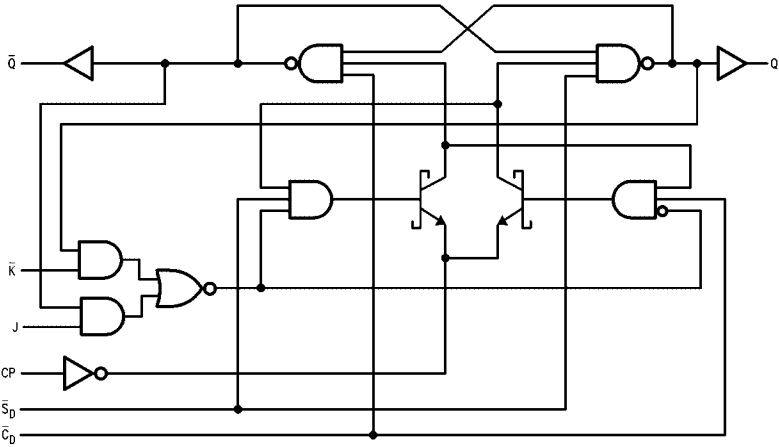
Inputs					Outputs	
$\overline{S_D}$	$\overline{C_D}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↗	l	l	L	H
H	H	↗	h	l	Toggle	
H	H	↗	l	h		
H	H	↗	h	h	H	L
H	H	L	X	X	Q	$\overline{Q}$

H (h) = HIGH Voltage Level
L (l) = LOW Voltage Level
↗ = LOW-to-HIGH Transition
X = Immaterial
Q₀ ($\overline{Q}_0$) = Before LOW-to-HIGH Transition of Clock
Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.

Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
J ₁ , J ₂ , $\overline{K}_1$, $\overline{K}_2$	Data Inputs	1.0/1.0	20 μ A/-0.6 mA
CP ₁ , CP ₂	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20 μ A/-0.6 mA
$\overline{C_{D1}}$, $\overline{C_{D2}}$	Direct Clear Inputs (Active LOW)	1.0/3.0	20 μ A/-1.8 mA
$\overline{S_{D1}}$, $\overline{S_{D2}}$	Direct Set Inputs (Active LOW)	1.0/3.0	20 μ A/-1.8 mA
Q ₁ , Q ₂ , $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33.3	-1 mA/20 mA

Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

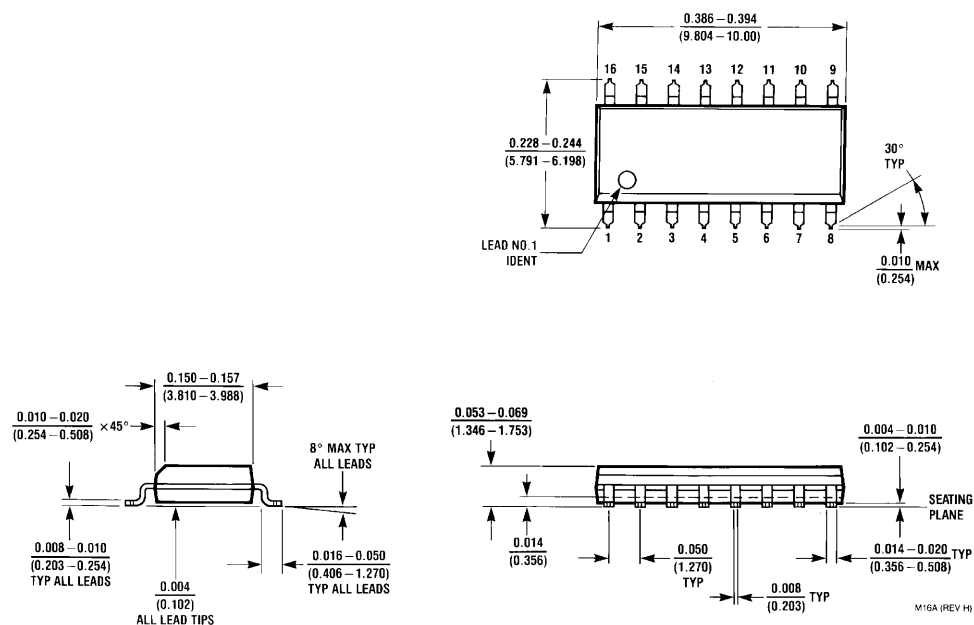
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC}	2.5		V	Min	I _{OH} = −1 mA
		5% V _{CC}	2.7				I _{OH} = −1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6	mA	Max	V _{IN} = 0.5V (J _n , $\overline{K}_n$)
				−1.8	mA	Max	V _{IN} = 0.5V ($\overline{C}_{Dn}$, $\overline{S}_{Dn}$)
I _{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		11.7	17.0	mA	Max	CP = 0V

AC Electrical Characteristics

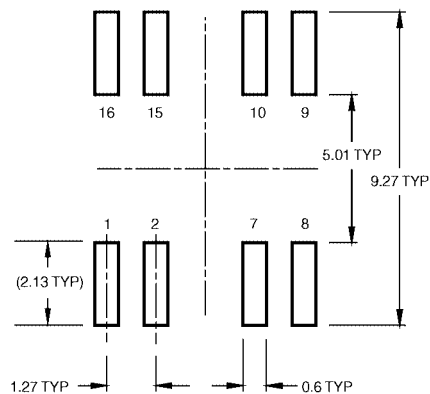
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100	125		90		MHz
t _{PLH}	Propagation Delay	3.8	5.3	7.0	3.8	8.0	ns
t _{PHL}	CP _n to Q _n or $\overline{Q}_n$	4.4	6.2	8.0	4.4	9.2	
t _{PLH}	Propagation Delay	3.2	5.2	7.0	3.2	8.0	ns
t _{PHL}	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q _n or $\overline{Q}_n$	3.5	7.0	9.0	3.5	10.5	ns

AC Operating Requirements

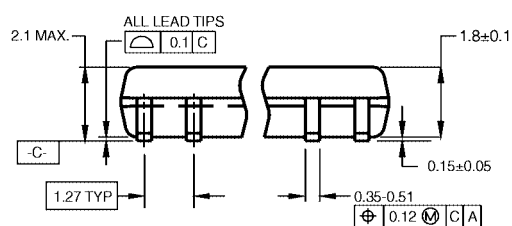
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	3.0		3.0		ns
t _S (L)	J _n or $\overline{K}_n$ to CP _n	3.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0		1.0		ns
t _H (L)	J _n or $\overline{K}_n$ to CP _n	1.0		1.0		
t _W (H)	CP _n Pulse Width	4.0		4.0		ns
t _W (L)	HIGH or LOW	5.0		5.0		
t _W (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0		4.0		ns
t _{REC}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0		2.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted


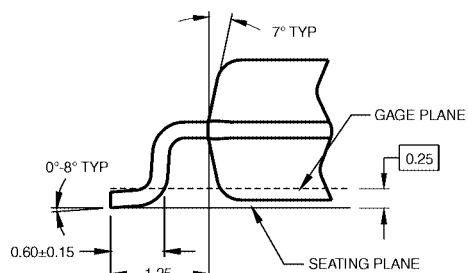
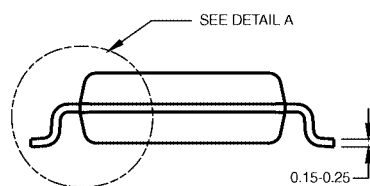
**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A**



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

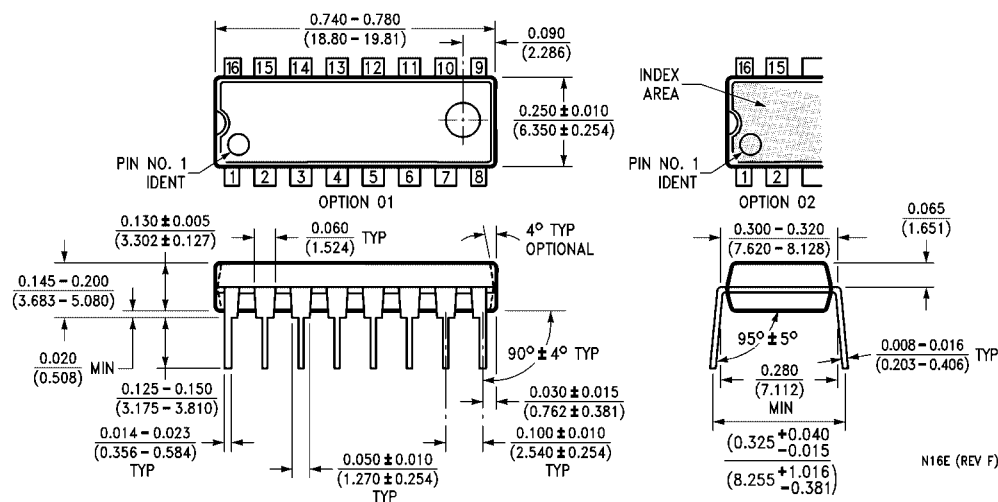
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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