

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

Bare Die

OptiMOS™3 Power MOS Transistor Chip
IPC26N12N

Data Sheet

Rev. 2.5
Final

Industrial & Multimarket

1 Description

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPP048N12N3 G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlSi system
- Passivation: nitride (only on edge structure)

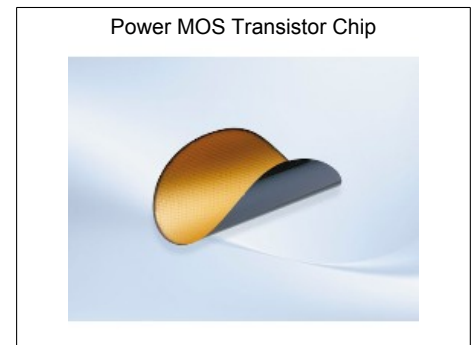
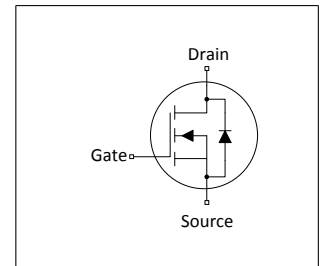


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{(BR)DSS}$	120	V
$R_{DS(on)}$	4.8 ¹⁾	mΩ
Die size	6.6 x 3.96	mm ²
Thickness	250	μm



Type / Ordering Code	Package	Marking	Related Links
IPC26N12N	Chip	not defined	-

2 Electrical Characteristics on Wafer Level

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	120	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	-	4	V	$V_{DS}=V_{GS}$, $I_D=244\text{ μA}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on- resistance	$R_{DS(on)}$	-	3.0 ²⁾	100 ³⁾	mΩ	$V_{GS}=10\text{ V}$, $I_D=2.0\text{ A}$
Reverse diode forward on-voltage	V_{SD}	-	1.0	1.2	V	$V_{GS}=0\text{ V}$, $I_F=1\text{ A}$

¹⁾ packaged in a P-TO220-3 (see ref. product)

²⁾ typical bare die $R_{DS(on)}$; $V_{GS}=10\text{ V}$ when used with 3x500μm Al-wedge bonding

³⁾ limited by wafer test-equipment

3 Package Outlines

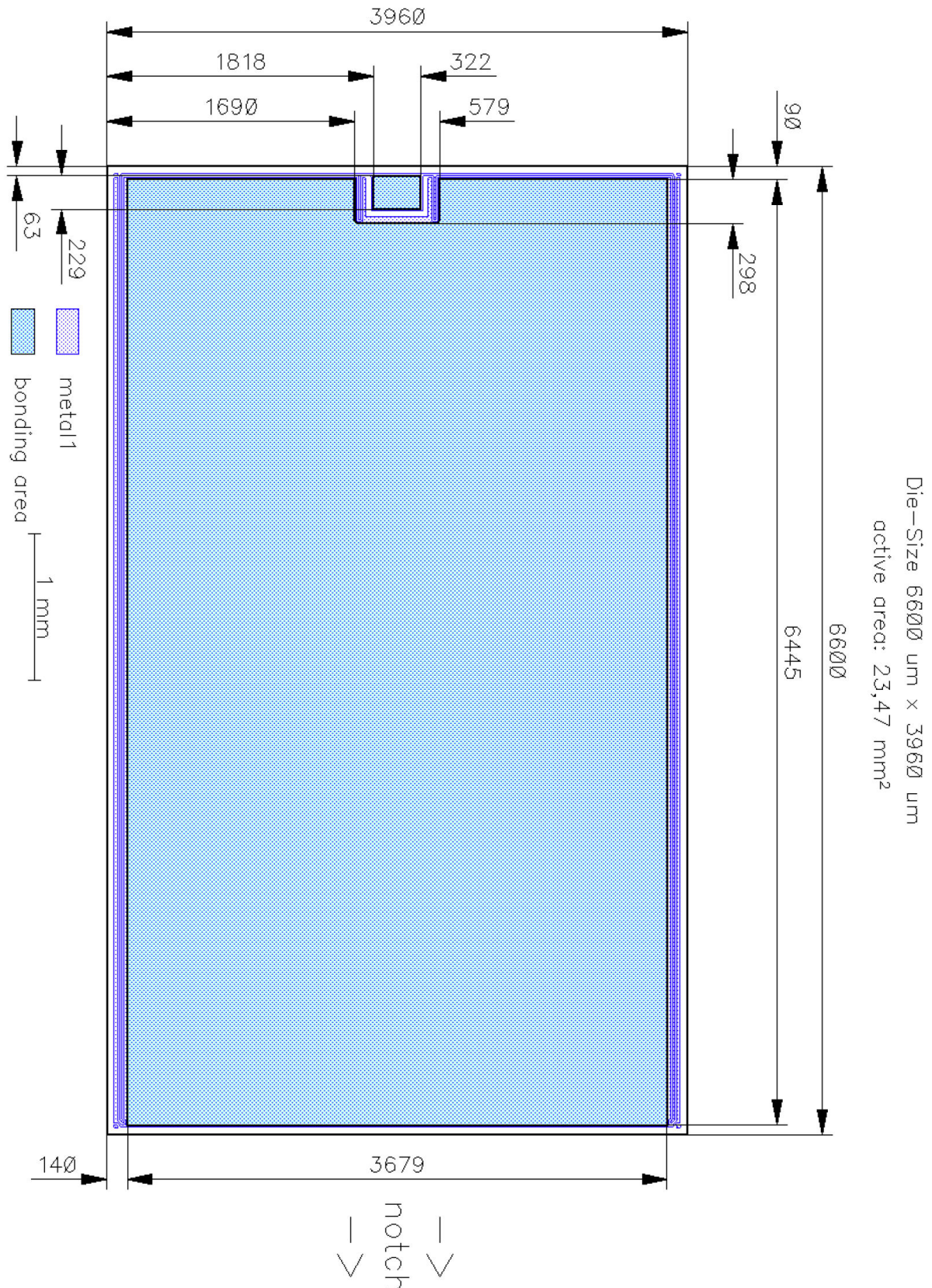


Figure 1 Outline Chip, dimensions in μm

Revision History

IPC26N12N

Revision: 2014-07-23, Rev. 2.5

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.5	2014-07-23	Release Final Version

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