PRELIMINARY

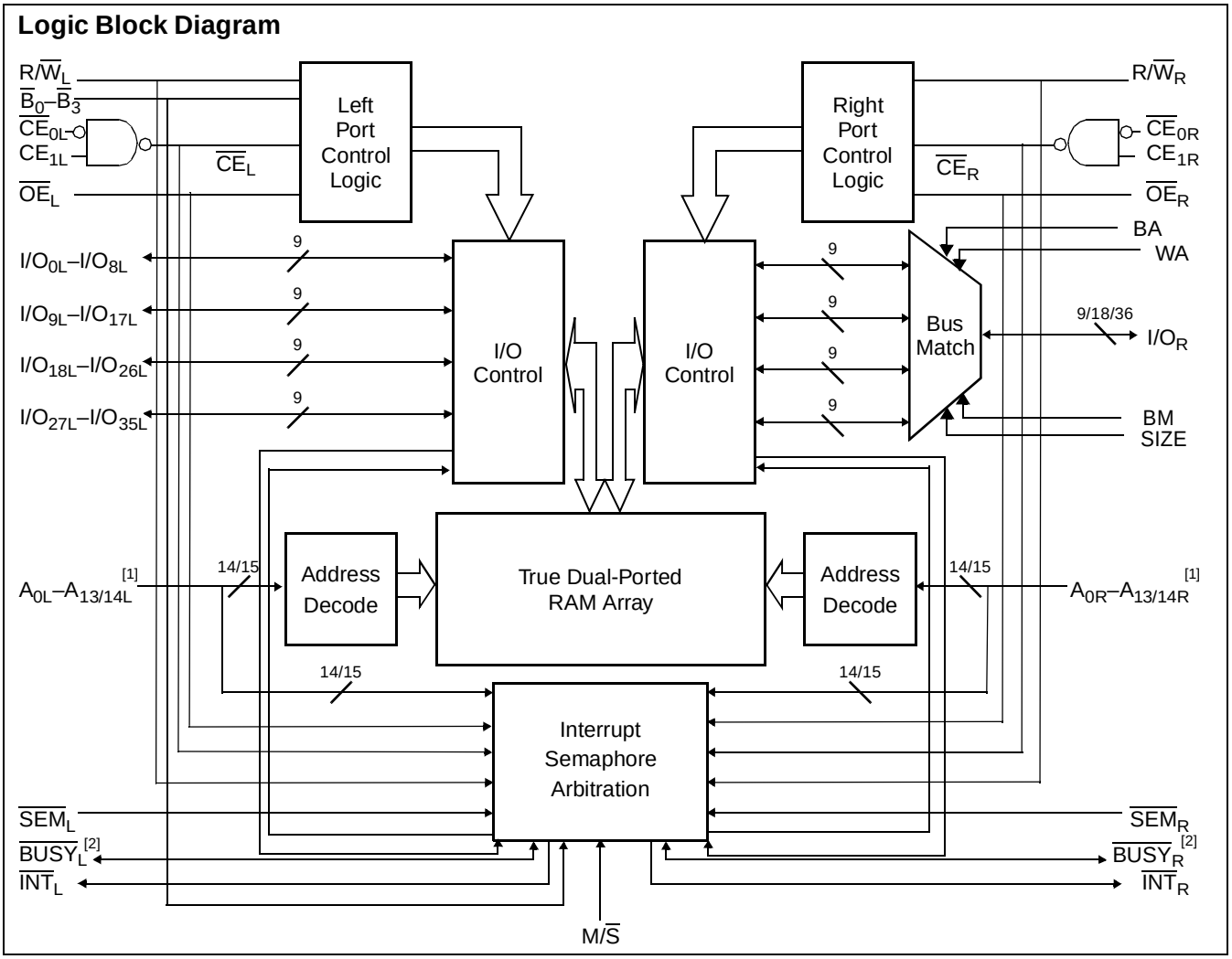
CY7C056V
CY7C057V

3.3V 16K/32K x 36
FLEx36™ Asynchronous Dual-Port Static RAM

Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- 16K x 36 organization (CY7C056V)
- 32K x 36 organization (CY7C057V)
- 0.25-micron CMOS for optimum speed/power
- High-speed access: 10/12/15/20 ns
- Low operating power
  - Active: I_{CC} = 260 mA (typical)
  - Standby: I_{SB3} = 10 µA (typical)
- Fully asynchronous operation
- Automatic power-down
- Expandable data bus to 72 bits or more using Master/Slave Chip Select when using more than one device
- On-Chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flag for port-to-port communication
- Byte Select on Left Port
- Bus Matching on Right Port
- Depth Expansion via dual chip enables
- Pin select for Master or Slave
- Commercial and Industrial Temperature Ranges
- Compact package
  - 144-Pin TQFP (20 x 20 x 1.4 mm)
  - 172-Ball BGA (1.0 mm pitch) (15 x 15 x .51 mm)

Logic Block Diagram



Notes:

1. A_0–A_{13} for 16K; A_0–A_{14} for 32K devices.
2. BUSY is an output in Master mode and an input in Slave mode.

Functional Description

The CY7C056V and CY7C057V are low-power CMOS 16K and 32K x 36 dual-port static RAMs. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as standalone 36-bit dual-port static RAMs or multiple devices can be combined in order to function as a 72-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 72-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable ($\overline{CE}$)[3], Read or Write Enable (R/$\overline{W}$), and Output Enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt Flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic Power-Down feature is controlled independently on each port by Chip Select ($\overline{CE}_0$ and CE_1) pins.

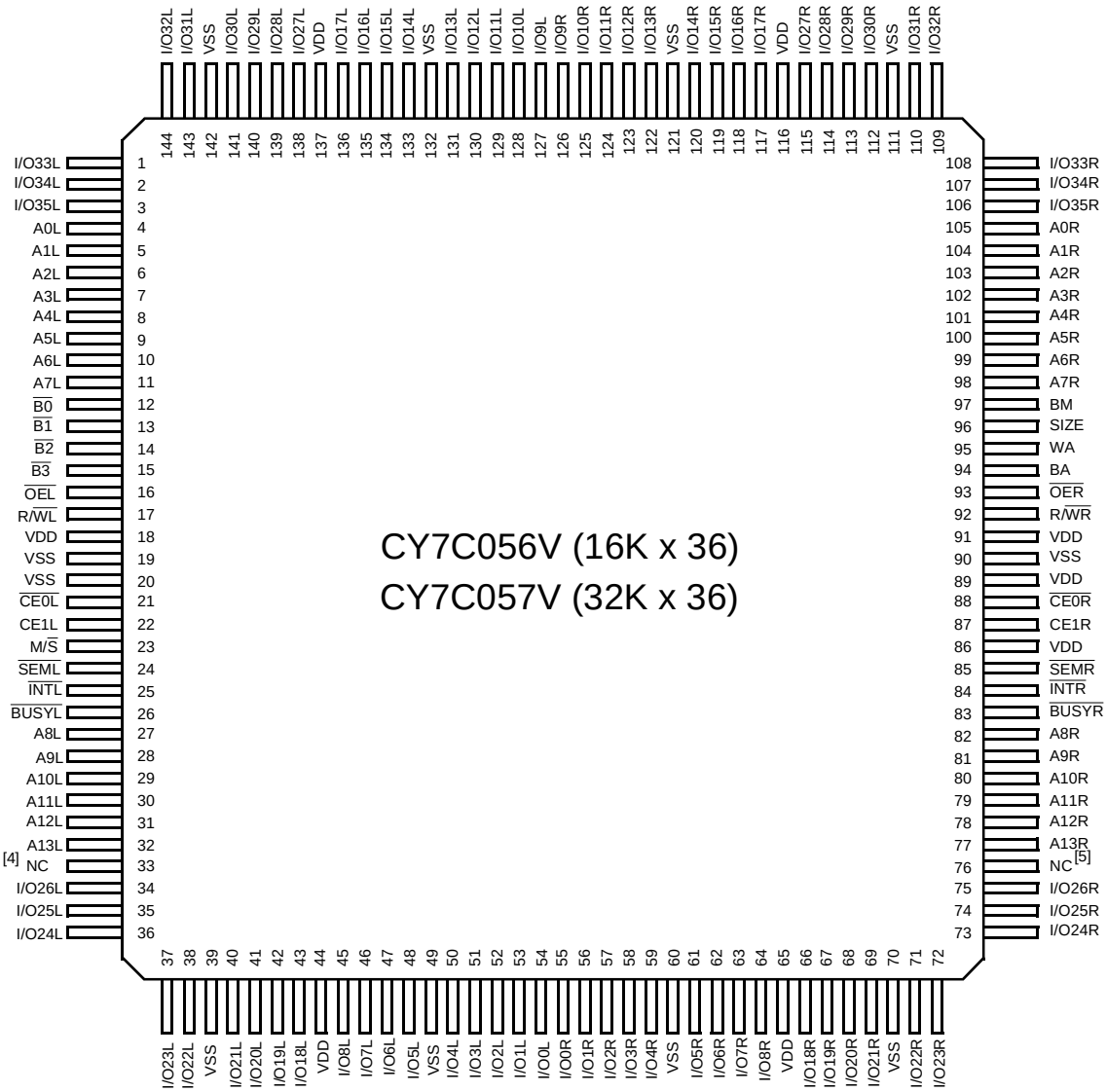
The CY7C056V and CY7C057V are available in 144-Pin Thin Quad Plastic Flatpack (TQFP) and 172-Ball Ball Grid Array (BGA) packages.

Note:
3. $\overline{CE}$ is LOW when $\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$.

Pin Configurations

144-Pin Thin Quad Flatpack (TQFP)

Top View



Notes:

4. This pin is A14L for CY7C057V.
5. This pin is A14R for CY7C057V.

Pin Configurations (continued)

172-Ball Ball Grid Array (BGA)

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	I/O32L	I/O30L	NC	VSS	I/O13L	VDD	I/O11L	I/O11R	VDD	I/O13R	VSS	NC	I/O30R	I/O32R
B	A0L	I/O33L	I/O29	I/O17L	I/O14L	I/O12L	I/O9L	I/O9R	I/O12R	I/O14R	I/O17R	I/O29R	I/O33R	A0R
C	NC	A1L	I/O31L	I/O27L	NC	I/O15L	I/O10L	I/O10R	I/O15R	NC	I/O27R	I/O31R	A1R	NC
D	A2L	A3L	I/O35L	I/O34L	I/O28L	I/O16L	VSS	VSS	I/O16R	I/O28R	I/O34R	I/O35R	A3R	A2R
E	A4L	A5L	NC	$\overline{B0L}$	NC	NC			NC	NC	BM	NC	A5R	A4R
F	VDD	A6L	A7L	$\overline{B1L}$	NC					NC	SIZE	A7R	A6R	VDD
G	$\overline{OEL}$	$\overline{B2L}$	$\overline{B3L}$	$\overline{CE0L}$							$\overline{CE0R}$	BA	WA	$\overline{OER}$
H	VSS	R/$\overline{WL}$	A8L	CE1L							CE1R	A8R	R/$\overline{WR}$	VSS
J	A9L	A10L	VSS	M/$\overline{S}$	NC					NC	VDD	VDD	A10R	A9R
K	A11L	A12L	NC	$\overline{SEML}$	NC	NC			NC	NC	$\overline{SEMR}$	NC	A12R	A11R
L	$\overline{BUSYL}$	A13L	$\overline{INTL}$	I/O26L	I/O25L	I/O19L	VSS	VSS	I/O19R	I/O25R	I/O26R	$\overline{INTR}$	A13R	$\overline{BUSYR}$
M	NC	NC[4]	I/O22L	I/O18L	NC	I/O7L	I/O2L	I/O2R	I/O7R	NC	I/O18R	I/O22R	NC[5]	NC
N	I/O24L	I/O20L	I/O8L	I/O6L	I/O5L	I/O3L	I/O0L	I/O0R	I/3R	I/O5R	I/O6R	I/O8R	I/O20R	I/O24R
P	I/O23L	I/O21L	NC	VSS	I/O4L	VDD	I/O1L	I/O1R	VDD	I/O4R	VSS	NC	I/O21R	I/O23R

Selection Guide

	CY7C056V CY7C057V -10	CY7C056V CY7C057V -12	CY7C056V CY7C057V -15	CY7C056V CY7C057V -20
Maximum Access Time (ns)	10	12	15	20
Typical Operating Current (mA)	260	250	240	230
Typical Standby Current for I_{SB1} (mA) (Both Ports TTL Level)	60	55	50	45
Typical Standby Current for I_{SB3} (µA) (Both Ports CMOS Level)	10 µA	10 µA	10 µA	10 µA

Pin Definitions

Left Port	Right Port	Description
A_{0L}–$A_{13/14L}$	A_{0R}–$A_{13/14R}$	Address (A_0–A_{13} for 16K; A_0–A_{14} for 32K devices)
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enable ($\overline{CE}$ is LOW when $\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
I/O_{0L}–I/O_{35L}	I/O_{0R}–I/O_{35R}	Data Bus Input/Output
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{B}_0$–$\overline{B}_3$		Byte Select Inputs. Asserting these signals enables read and write operations to the corresponding bytes of the memory array.
	BM, SIZE	See Bus Matching for details.
	WA, BA	See Bus Matching for details.
$M/\overline{S}$		Master or Slave Select
V_{SS}		Ground
V_{DD}		Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State .....–0.5V to V_{DD}+0.5V

DC Input Voltage.....–0.5V to V_{DD}+0.5V[6]

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V

Latch-Up Current..... >200 mA

Note:
6. Pulse width < 20 ns.

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	3.3V ± 165 mV
Industrial	–40°C to +85°C	3.3V ± 165 mV

Shaded areas contain advance information.

Electrical Characteristics Over the Operating Range [7, 8]

Parameter	Description		CY7C056V CY7C057V -10 Min.	-10 Typ.	-10 Max.	-12 Min.	-12 Typ.	-12 Max.	-15 Min.	-15 Typ.	-15 Max.	-20 Min.	-20 Typ.	-20 Max.	Unit
V_{OH}	Output HIGH Voltage (V_{DD} = Min., I_{OH} = –4.0 mA)		2.4			2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{DD} = Min., I_{OL} = +4.0 mA)				0.4			0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.0			2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage				0.8			0.8			0.8			0.8	V
I_{OZ}	Output Leakage Current		-10		10	–10		10	–10		10	–10		10	µA
I_{CC}	Operating Current (V_{DD} = Max., I_{OUT} = 0 mA) Outputs Disabled	Com'l.		260	410		250	385		240	360		230	340	mA
		Indust.								265	385				mA
I_{SB1}	Standby Current (Both Ports TTL Level and Deselected) f = f_{MAX}	Com'l.		60	80		55	75		50	70		45	65	mA
		Indust.								65	95				mA
I_{SB2}	Standby Current (One Port TTL Level and Deselected) f = f_{MAX}	Com'l.		185	250		180	240		175	230		165	210	mA
		Indust.								190	255				mA
I_{SB3}	Standby Current (Both Ports CMOS Level and Deselected) f =0	Com'l.		0.01	1		0.01	1		0.01	1		0.01	1	mA
		Indust.								0.01	1				mA
I_{SB4}	Standby Current (One Port CMOS Level and Deselected) f = f_{MAX} [9]	Com'l.		170	220		160	210		155	200		145	180	mA
		Indust.								170	215				mA

Shaded areas contain advance information.

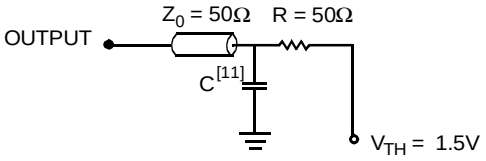
Capacitance [10]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V	10	pF
C_{OUT}	Output Capacitance		10	pF

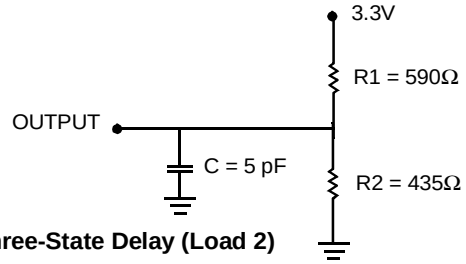
Notes:

7. Cross Levels are V_{DD} – 0.2V≤ V≤0.2V.
8. Deselection for a port occurs if $\overline{CE}_0$ is HIGH or if CE_1 is LOW.
9. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except Output Enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
10. Tested initially and after any design or process changes that may affect these parameters.

AC Test Load and Waveforms

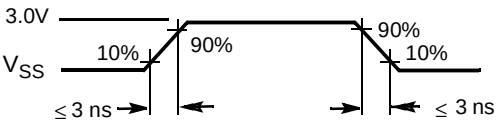


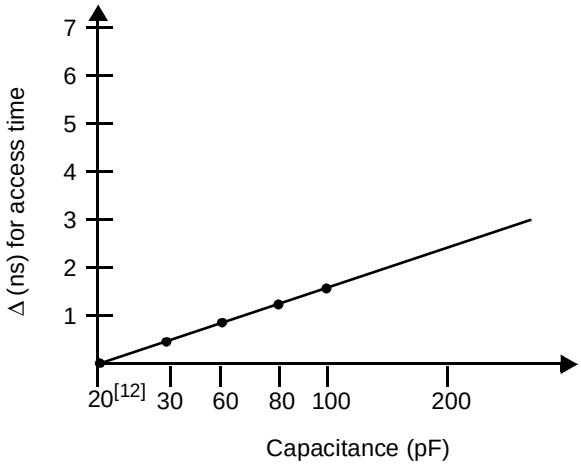
(a) Normal Load (Load 1)



(b) Three-State Delay (Load 2)

ALL INPUT PULSES





(b) Load Derating Curve

Notes:
11. External AC Test Load Capacitance = 10 pF.
12. (Internal I/O pad Capacitance = 10 pF) + AC Test Load.

Switching Characteristics Over the Operating Range[13]

Parameter	Description	CY7C056V CY7C057V								Unit
		-10		-12		-15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		ns
t_{ACE}[3, 14]	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		8		10		12	ns
t_{LZOE}[3, 15, 16, 17]	$\overline{OE}$ Low to Low Z	0		0		0		0		ns
t_{HZOE}[3, 15, 16, 17]	$\overline{OE}$ HIGH to High Z		8		10		10		12	ns
t_{LZCE}[3, 13, 16, 17]	$\overline{CE}$ LOW to Low Z	3		3		3		3		ns
t_{HZCE}[3, 15, 16, 17]	$\overline{CE}$ HIGH to High Z		8		10		10		12	ns
t_{LZBE}	Byte Enable to Low Z	3		3		3		3		ns
t_{HZBE}	Byte Enable to High Z		8		10		10		12	ns
t_{PU}[3, 17]	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}[3, 17]	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
t_{ABE}[14]	Byte Enable Access Time		10		12		15		20	ns
Write Cycle										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}[3, 14]	$\overline{CE}$ LOW to Write End	7.5		10		12		15		ns
t_{AW}	Address Valid to Write End	7.5		10		12		15		ns
t_{HA}	Address Hold From Write End	0		0		0		0		ns
t_{SA}[14]	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	Write Pulse Width	7.5		10		12		15		ns
t_{SD}	Data Set-Up to Write End	7.5		10		10		15		ns
t_{HD}	Data Hold From Write End	0		0		0		0		ns
t_{HZWE}[16, 17]	R/$\overline{W}$ LOW to High Z		8		10		10		12	ns
t_{LZWE}[16, 17]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		ns
t_{WDD}[18]	Write Pulse to Data Delay		20		25		30		45	ns
t_{DDD}[18]	Write Data Valid to Read Data Valid		16		20		25		30	ns
Busy Timing[19]										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		10		12		15		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		10		12		15		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		10		12		15		20	ns

Notes:

13. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 10-pF load capacitance.
14. To access RAM, $\overline{CE}$ = L and $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{SCE} time.
15. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
16. Test conditions used are Load 2.
17. This parameter is guaranteed by design, but it is not production tested. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
18. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
19. Test conditions used are Load 1.

Switching Characteristics Over the Operating Range[13] (continued)

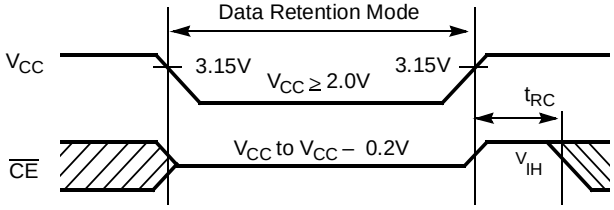
Parameter	Description	CY7C056V CY7C057V								Unit
		-10		-12		-15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Busy Timing[19]										
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		10		12		15		20	ns
t_{PS}	Port Set-Up for Priority	5		5		5		5		ns
t_{WB}	R/$\overline{W}$ LOW after $\overline{BUSY}$ (Slave)	0		0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	8		11		13		15		ns
t_{BDD}[19]	$\overline{BUSY}$ HIGH to Data Valid		10		12		15		20	ns
Interrupt Timing[19]										
t_{INS}	$\overline{INT}$ Set Time		10		12		15		20	ns
t_{INR}	$\overline{INT}$ Reset Time		10		12		15		20	ns
Semaphore Timing										
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		10		10		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		ns
t_{SAA}	SEM Address Access Time		10		12		15		20	ns

Data Retention Mode

The CY7C056V and CY7C057V are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable ($\overline{CE}$)[3] must be held HIGH during data retention, within V_{DD} to V_{DD} – 0.2V.
2. $\overline{CE}$ must be kept between V_{DD} – 0.2V and 70% of V_{DD} during the power-up and power-down transitions.
3. The RAM can begin operation >t_{RC} after V_{DD} reaches the minimum operating voltage (3.15 volts).

Timing



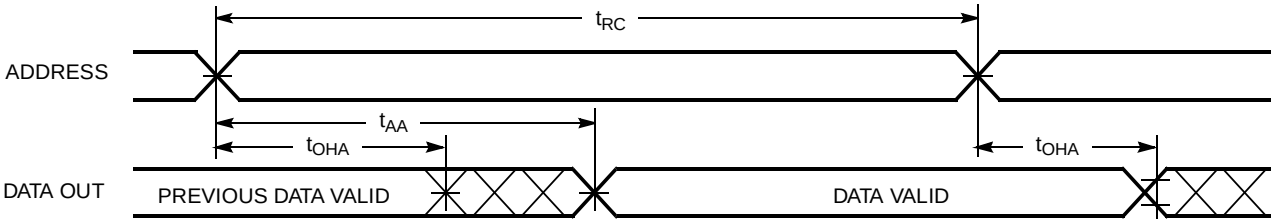
Parameter	Test Conditions[21]	Max.	Unit
ICC_{DR1}	@ VDD_{DR} = 2V	50	µA

Notes:

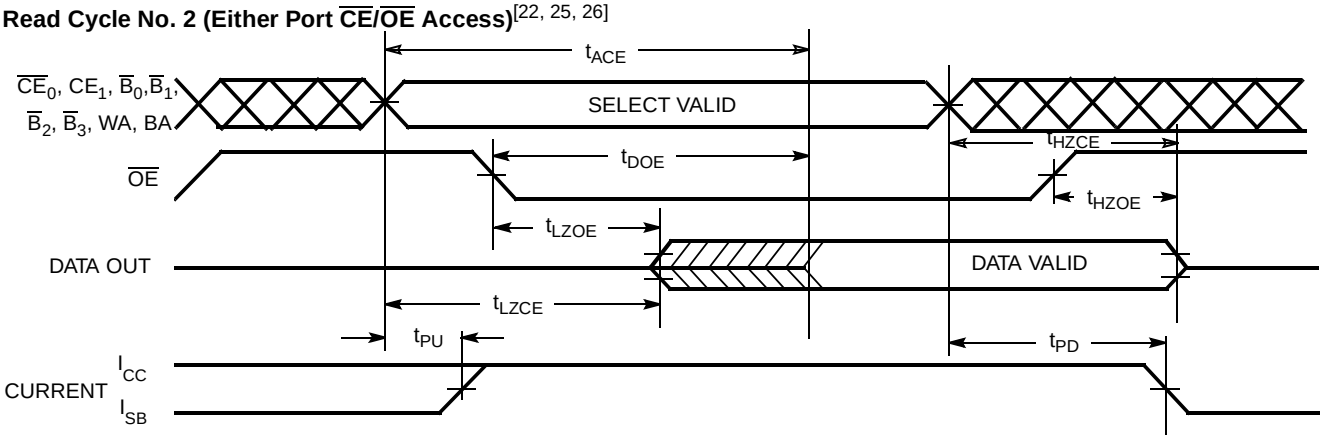
20. t_{BDD} is a calculated parameter and is the greater of t_{WDD}–t_{PWE} (actual) or t_{DDD}–t_{SD} (actual).
21. $\overline{CE}$ = V_{DD}, V_{in} = V_{SS} to V_{DD}, T_A = 25°C. This parameter is guaranteed but not tested.

Switching Waveforms

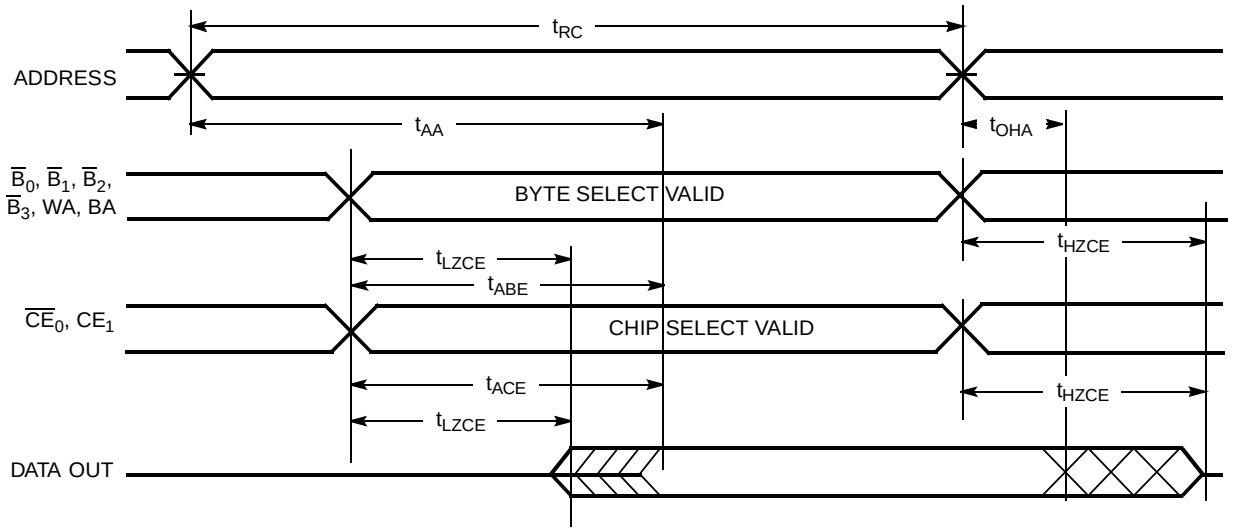
Read Cycle No. 1 (Either Port Address Access)[22, 23, 24]



Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[22, 25, 26]



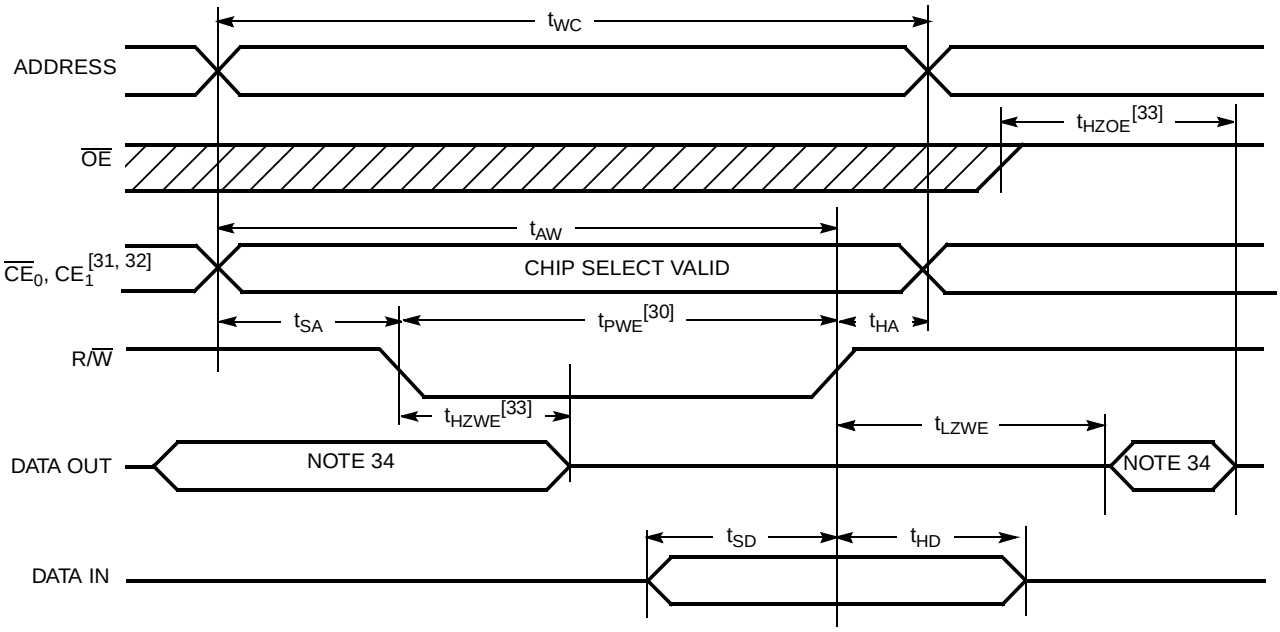
Read Cycle No. 3 (Either Port)[22, 24, 25, 26]



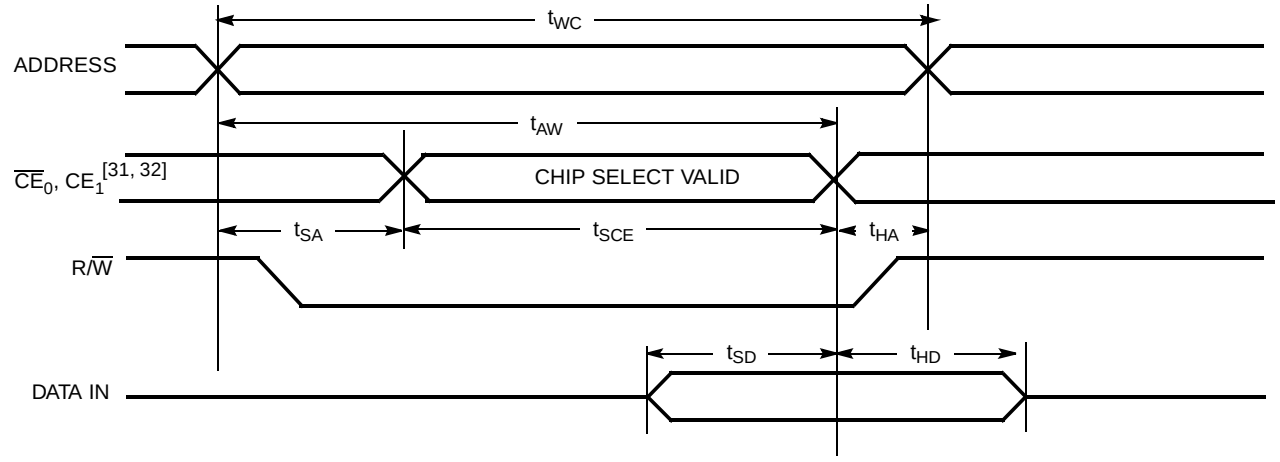
Notes:
22. R/$\overline{W}$ is HIGH for read cycles.
23. Device is continuously selected. $\overline{CE}_0 = V_{IL}$, $CE_1 = V_{IH}$, and $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$, WA, BA are valid. This waveform cannot be used for semaphore reads.
24. $\overline{OE} = V_{IL}$.
25. Address valid prior to or coinciding with $\overline{CE}_0$ transition LOW and CE_1 transition HIGH.
26. To access RAM, $\overline{CE}_0 = V_{IL}$, $CE_1 = V_{IH}$, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$, WA, BA are valid, and $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE}_0 = V_{IH}$, $CE_1 = V_{IL}$ and $\overline{SEM} = V_{IL}$ or $\overline{CE}_0$ and $\overline{SEM} = V_{IL}$, and $CE_1 = \overline{B}_0 = \overline{B}_1 = \overline{B}_2 = \overline{B}_3 = V_{IH}$.

Switching Waveforms (continued)

Write Cycle No. 1: R/$\overline{W}$ Controlled Timing[27, 28, 29, 30]



Write Cycle No. 2: $\overline{CE}$ Controlled Timing[27, 28, 29, 35]

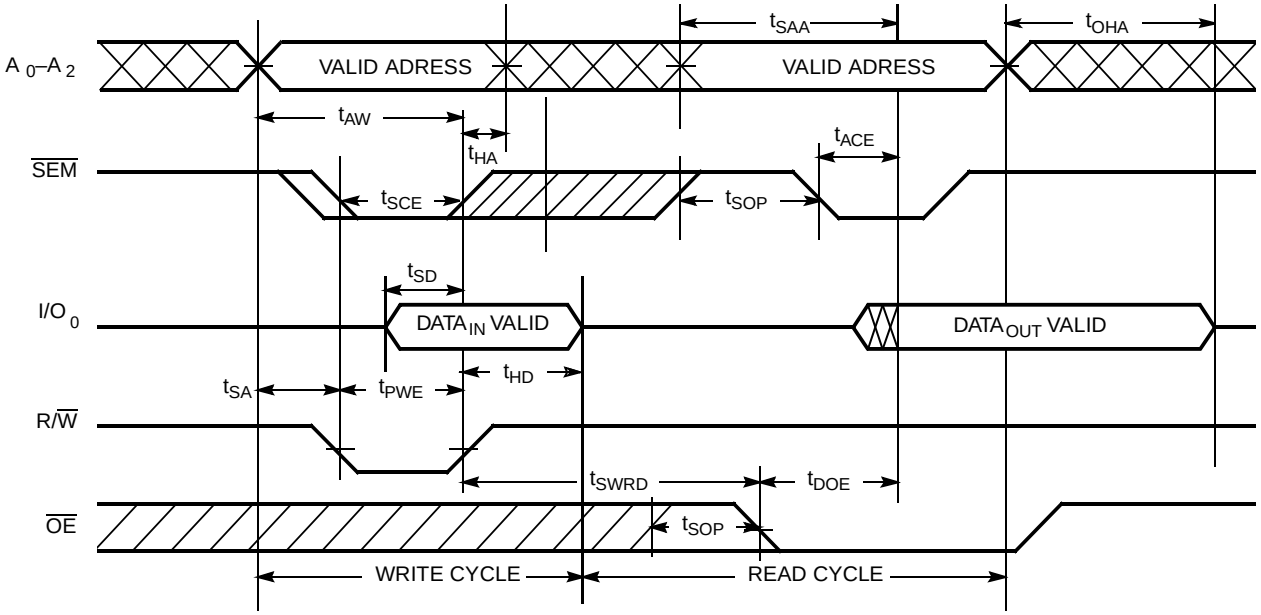


Notes:

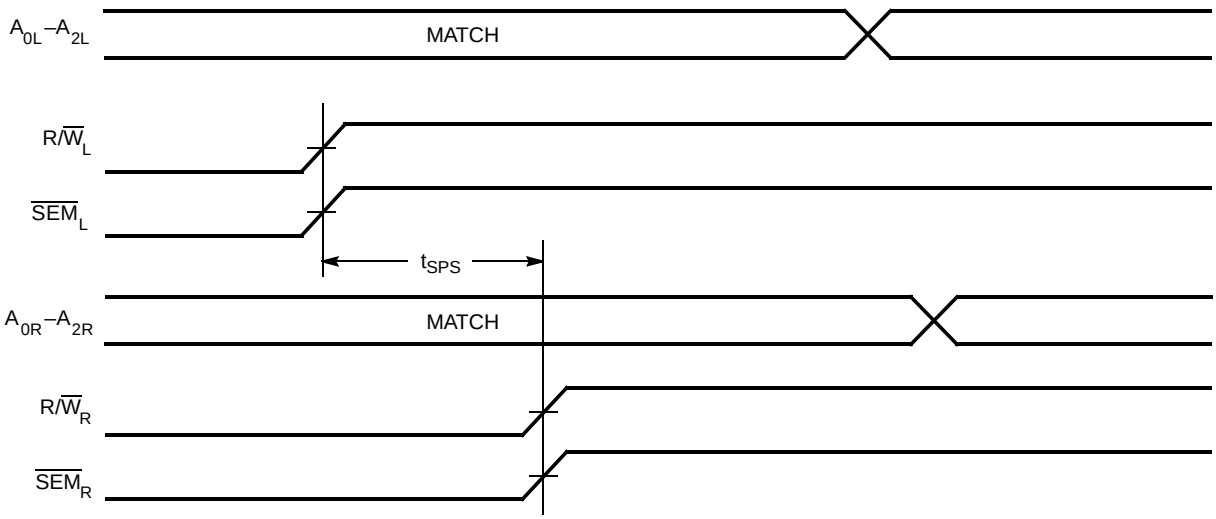
27. R/$\overline{W}$ must be HIGH during all address transitions.
28. A write occurs during the overlap (t_{SCE} or t_{PWE}) of $\overline{CE}_0$=V_{IL} and CE_1=V_{IH} or $\overline{SEM}$=V_{IL} and $\overline{B}_{0-3}$ LOW.
29. t_{HA} is measured from the earlier of $\overline{CE}_0$/CE_1 or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of Write Cycle.
30. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
31. To access RAM, $\overline{CE}_0$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
32. To access byte $\overline{B}_0$, $\overline{CE}_0$ = V_{IL}, $\overline{B}_0$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
    To access byte $\overline{B}_1$, $\overline{CE}_0$ = V_{IL}, $\overline{B}_1$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
    To access byte $\overline{B}_2$, $\overline{CE}_0$ = V_{IL}, $\overline{B}_2$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
    To access byte $\overline{B}_3$, $\overline{CE}_0$ = V_{IL}, $\overline{B}_3$ = V_{IL}, CE_1=$\overline{SEM}$ = V_{IH}.
33. Transition is measured ±150 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
34. During this period, the I/O pins are in the output state, and input signals must not be applied.
35. If the $\overline{CE}_0$ LOW and CE_1 HIGH or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[36]



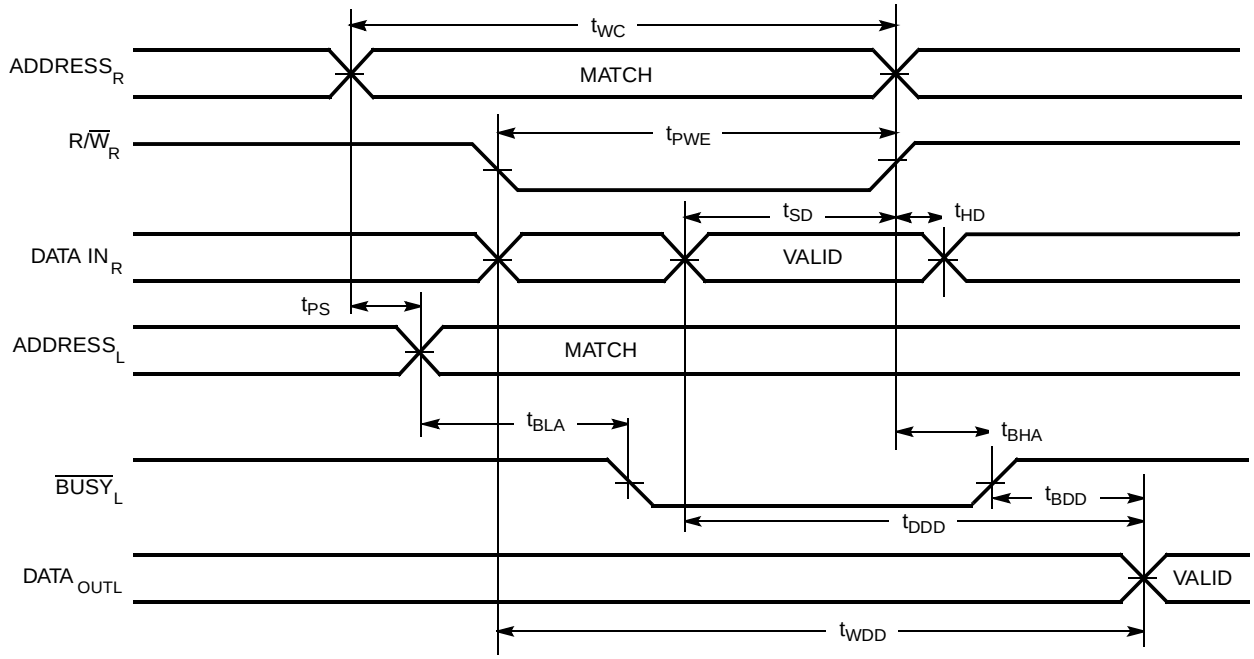
Timing Diagram of Semaphore Contention[37, 38, 39]



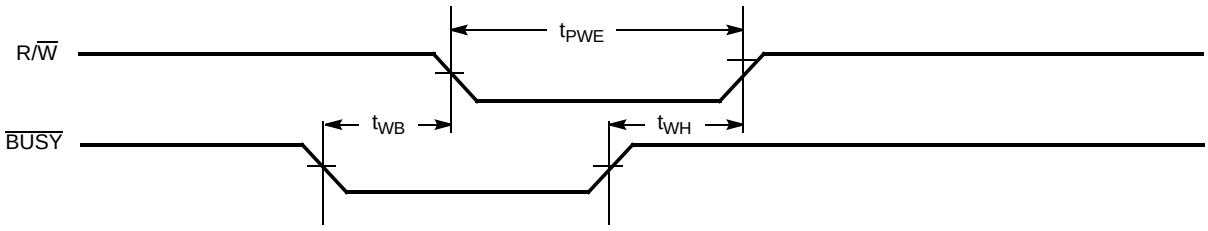
Notes:
36. $\overline{CE}_0$ = HIGH and CE_1 = LOW for the duration of the above timing (both write and read cycle).
37. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_{0R} = \overline{CE}_{0L}$ = HIGH and $CE_{1R} = CE_{1L}$=LOW.
38. Semaphores are reset (available to both ports) at cycle start.
39. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms (continued)

Timing Diagram of Write with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[40]



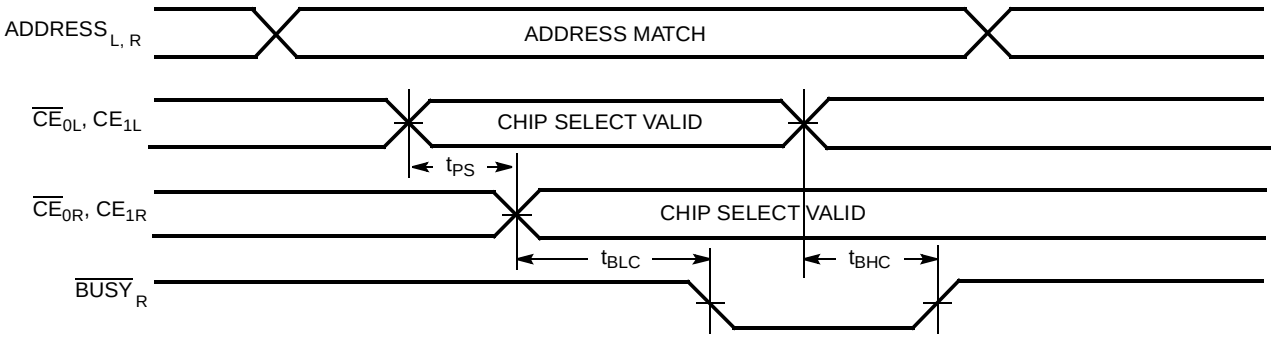
Write Timing with Busy Input (M/$\overline{S}$=LOW)



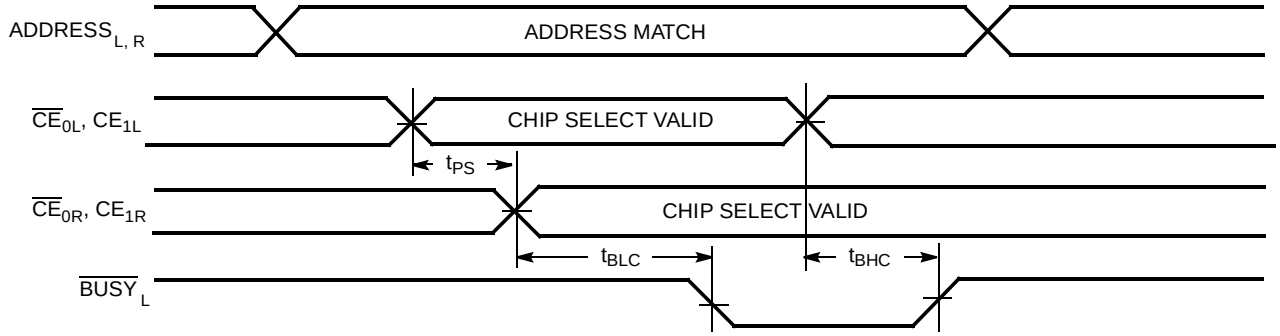
Note:
40. $\overline{CE}_{0L}$ = $\overline{CE}_{0R}$ = LOW; CE_{1L} = CE_{1R} = HIGH.

Switching Waveforms (continued)

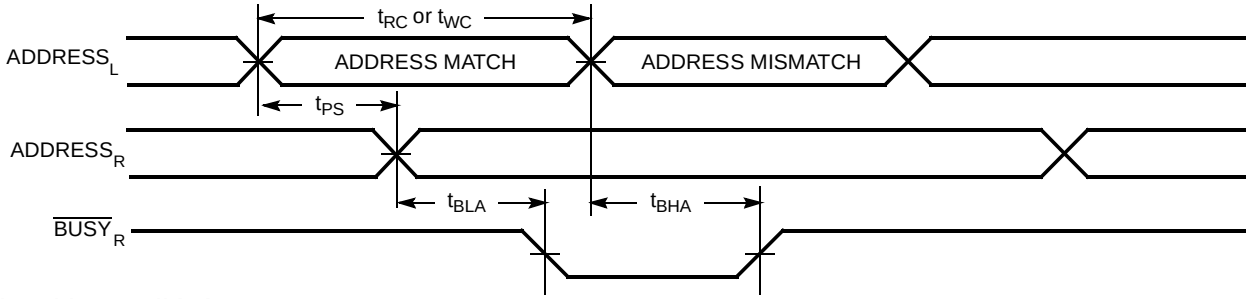
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[41]
$\overline{CE}_L$ Valid First:



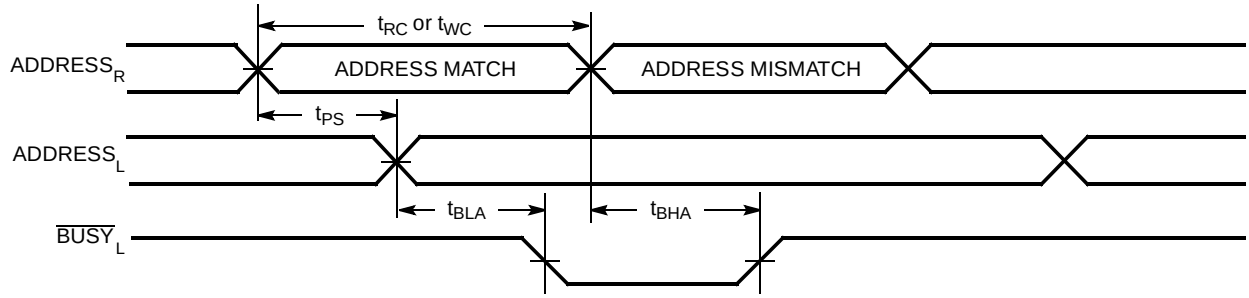
CE_R Valid First:



Busy Timing Diagram No. 2 (Address Arbitration)[41]
Left Address Valid First:



Right Address Valid First:

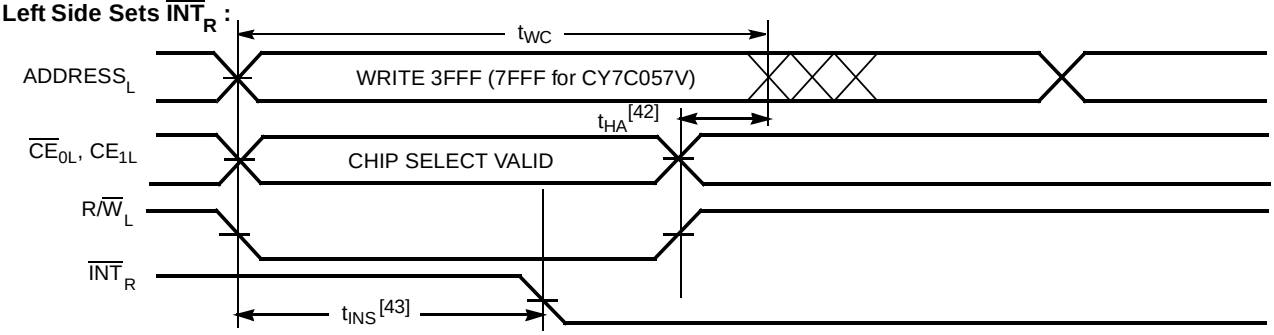


Note:
41. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

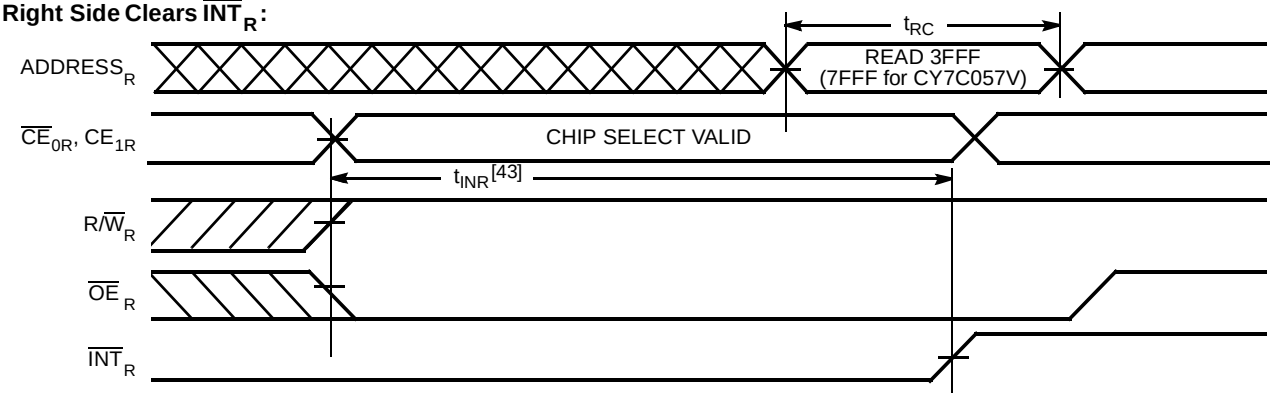
Switching Waveforms (continued)

Interrupt Timing Diagrams

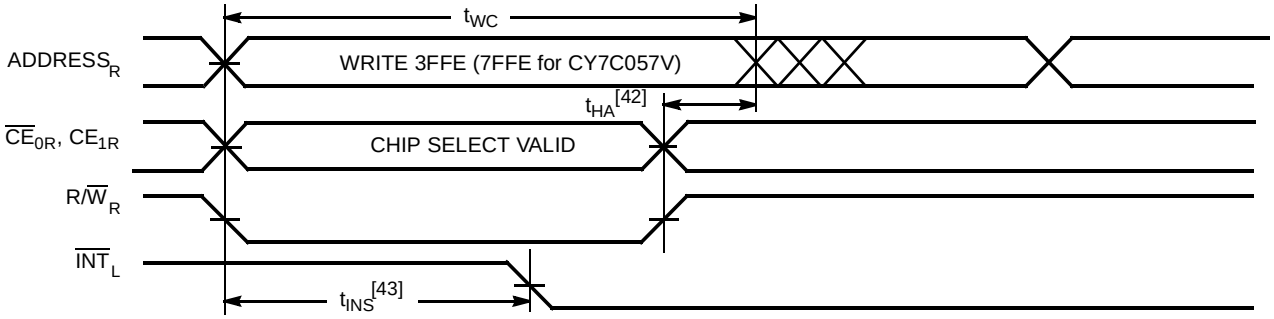
Left Side Sets $\overline{INT}_R$:



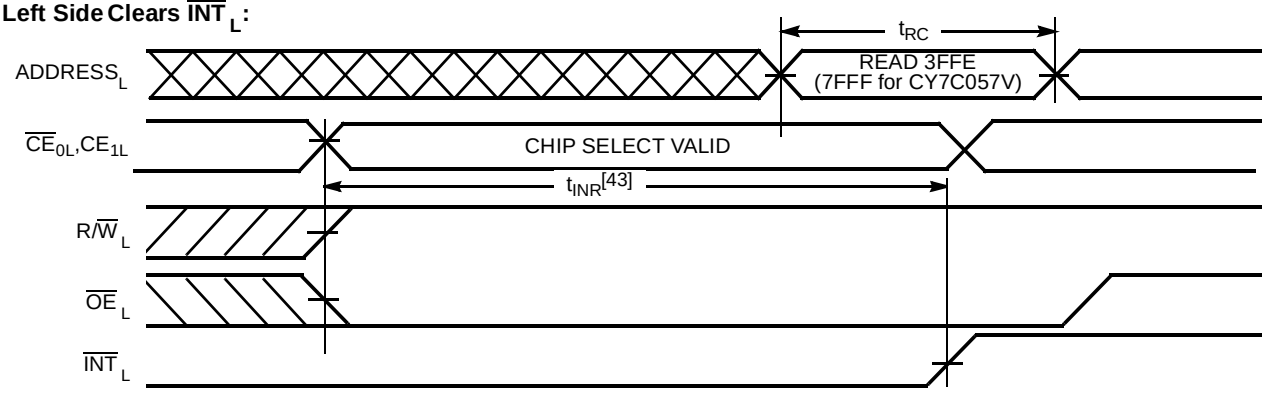
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Notes:

42. t_{HA} depends on which enable pin ($\overline{CE}_{0L}$/CE_{1L} or R/$\overline{W}_L$) is deasserted first.
43. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_{0L}$/CE_{1L} or R/$\overline{W}_L$) is asserted last.

Architecture

The CY7C056V and CY7C057V consist of an array of 16K and 32K words of 36 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}_0$/CE_1, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two Interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two Semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the devices can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The devices also have an automatic power-down feature controlled by $\overline{CE}_0$/CE_1. Each port is provided with its own Output Enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the R/$\overline{W}$ pin (see Write Cycle No. 1 waveform) or the $\overline{CE}_0$ and CE_1 pins (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$[3] pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$[3] pin, and $\overline{OE}$ must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (3FFF for the CY7C056V, 7FFF for the CY7C057V) is the mailbox for the right port and the second-highest memory location (3FFE for the CY7C056V, 7FFE for the CY7C057V) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in *Table 2.*

Busy

The CY7C056V and CY7C057V provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' Chip Enables[3] are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the $\overline{BUSY}$ input has settled (t_{BLC} or t_{BLA}), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C056V and CY7C057V provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control of the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip select for the semaphore latches. For normal semaphore access, $\overline{CE}$[3] must remain HIGH during $\overline{SEM}$ LOW. A $\overline{CE}$ active semaphore access is also available. The semaphore may be accessed through the right port with $\overline{CE}_{0R}$/CE_{1R} active by asserting the Bus Match Select (BM) pin LOW and asserting the Bus Size Select (SIZE) pin HIGH. The semaphore may be accessed through the left port with $\overline{CE}_{0L}$/CE_{1L} active by asserting all $\overline{B}_{0-3}$ Byte Select pins HIGH. A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a 1 will appear at the same semaphore address on the right port. That semaphore can now only be modified by the port showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both ports. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, data lines 0 through 8 output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Table 1. Non-Contending Read/Write[3]

Inputs					Outputs	Operation
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$	$\overline{SEM}$	I/O_0–I/O_{35}	
H	X	X	X	H	High Z	Deselected: Power-Down
X	X	X	All H	H	High Z	Deselected: Power-Down
L	L	X	H/L	H	Data In and High Z	Write to Selected Bytes Only
L	L	X	All L	H	Data In	Write to All Bytes
L	H	L	H/L	H	Data Out and High Z	Read Selected Bytes Only
L	H	L	All L	H	Data Out	Read All Bytes
X	X	H	X	X	High Z	Outputs Disabled
H	H	L	X	L	Data Out	Read Data in Semaphore Flag
X	H	L	All H	L	Data Out	Read Data in Semaphore Flag
H	⌐	X	X	L	Data In	Write D_{IN0} into Semaphore Flag
X	⌐	X	All H	L	Data In	Write D_{IN0} into Semaphore Flag
L	X	X	Any L	L		Not Allowed

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = HIGH)[3, 44]

	Left Port					Right Port				
Function	R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L-13L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R-13R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	X	3FFF	X	X	X	X	X	L[46]
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	X	X	L	L	3FFF	H[45]
Set Left $\overline{INT}_L$ Flag	X	X	X	X	L[45]	L	L	X	3FFE	X
Reset Left $\overline{INT}_L$ Flag	X	L	L	3FFE	H[46]	X	X	X	X	X

Table 3. Semaphore Operation Example

Function	I/O_0–I/O_8 Left	I/O_0–I/O_8 Right	Status
No Action	1	1	Semaphore Free
Left Port Writes 0 to Semaphore	0	1	Left Port Has Semaphore Token
Right Port Writes 0 to Semaphore	0	1	No Change. Right Side Has No Write Access to Semaphore
Left Port Writes 1 to Semaphore	1	0	Right Port Obtains Semaphore Token
Left Port Writes 0 to Semaphore	1	0	No Change. Left Port Has No Write Access to Semaphore
Right Port Writes 1 to Semaphore	0	1	Left Port Obtains Semaphore Token
Left Port Writes 1 to Semaphore	1	1	Semaphore Free
Right Port Writes 0 to Semaphore	1	0	Right Port Has Semaphore Token
Right Port Writes 1 to Semaphore	1	1	Semaphore Free
Left Port Writes 0 to Semaphore	0	1	Left Port Has Semaphore Token
Left Port Writes 1 to Semaphore	1	1	Semaphore Free

Notes:
44. A_{0L-14L} and A_{0R-14R}, 7FFF/7FFE for the CY7C057V.
45. If $\overline{BUSY}_R$=L, then no change.
46. If $\overline{BUSY}_L$=L, then no change.

Right Port Configuration [47, 48, 49]

BM	SIZE	Configuration	I/O Pins Used
0	0	x36 (Standard)	$I/O_{0–35}$
0	1	x36 ($\overline{CE}$ Active $\overline{SEM}$ Mode)	$I/O_{0–35}$
1	0	x18	$I/O_{0–17}$
1	1	x9	$I/O_{0–8}$

Right Port Operation

Configuration	WA	BA	Data Accessed[50]	I/O Pins Used
x36	X	X	$DQ_{0–35}$	$I/O_{0–35}$
x18	0	X	$DQ_{0–17}$	$I/O_{0–17}$
x18	1	X	$DQ_{18–35}$	$I/O_{0–17}$
x9	0	0	$DQ_{0–8}$	$I/O_{0–8}$
x9	0	1	$DQ_{9–17}$	$I/O_{0–8}$
x9	1	0	$DQ_{18–26}$	$I/O_{0–8}$
x9	1	1	$DQ_{27–35}$	$I/O_{0–8}$

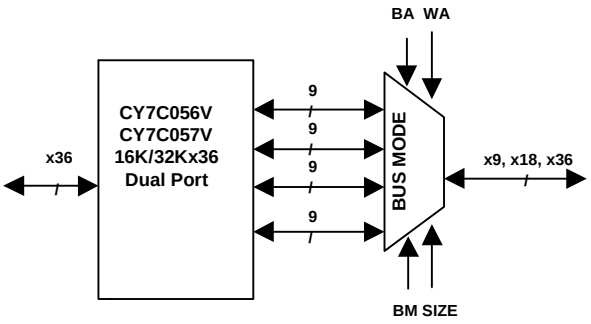
Left Port Operation

Control Pin	Effect
$\overline{B0}$	$I/O_{0–8}$ Byte Control
$\overline{B1}$	$I/O_{9–17}$ Byte Control
$\overline{B2}$	$I/O_{18–26}$ Byte Control
$\overline{B3}$	$I/O_{27–35}$ Byte Control

Notes:
47. BM and SIZE must be configured one clock cycle before operation is guaranteed.
48. In x36 mode WA and BA pins are “Don’t Care.”
49. In x18 mode BA pin is a “Don’t Care.”
50. DQ represents data output of the chip.

Bus Match Operation

The right port of the CY7C057V 32Kx36 dual-port SRAM can be configured in a 36-bit long-word, 18-bit word, or 9-bit byte format for data I/O. The data lines are divided into four lanes, each consisting of 9 bits (byte-size data lines).



The Bus Match Select (BM) pin works with Bus Size Select (SIZE) to select bus width (long-word, word, or byte) for the right port of the dual-port device. The data sequencing arrangement is selected using the Word Address (WA) and Byte Address (BA) input pins. A logic “0” applied to both the Bus Match Select (BM) pin and to the Bus Size Select (SIZE) pin will select long-word (36-bit) operation. A logic “1” level applied to the Bus Match Select (BM) pin will enable either byte or word bus width operation on the right port I/Os depending on the logic level applied to the SIZE pin. The level of Bus Match Select (BM) must be static throughout device operation.

Normally, the Bus Size Select (SIZE) pin would have no standard-cycle application when BM = LOW and the device is in long-word (36-bit) operation. A “special” mode has been added however to disable ALL right port I/Os while the chip is active. This I/O disable mode is implemented when SIZE is forced to a logic “1” while BM is at a logic “0”. It allows the bus-matched port to support a chip enable “Don’t Care” semaphore read/write access similar to that provided on the left port of the device when all Byte Select ($\overline{B}_{0-3}$) control inputs are deselected.

The Bus Size Select (SIZE) pin selects either a byte or word data arrangement on the right port when the Bus Match Select (BM) pin is HIGH. A logic “1” on the SIZE pin when the BM pin is HIGH selects a byte bus (9-bit) data arrangement). A logic “0” on the SIZE pin when the BM pin is HIGH selects a word bus (18-bit) data arrangement. The level of the Bus Size Select (SIZE) must also be static throughout normal device operation.

Long-Word (36-bit) Operation

Bus Match Select (BM) and Bus Size Select (SIZE) set to a logic “0” will enable standard cycle long-word (36-bit) operation. In this mode, the right port’s I/O operates essentially in an identical fashion as does the left port of the dual-port SRAM. However no Byte Select control is available. All 36 bits of the long-word are shifted into and out of the right port’s I/O buffer stages. All read and write timing parameters may be identical with respect to the two data ports. When the right port is configured for a long-word size, Word Address (WA), and Byte Address (BA) pins have no application and their inputs are “Don’t Care”[51] for the external user.

Word (18-bit) Operation

Word (18-bit) bus sizing operation is enabled when Bus Match Select (BM) is set to a logic “1” and the Bus SIze Select (SIZE) pin is set to a logic “0”. In this mode, 18 bits of data are ported through I/O_{0R-17R}. The level applied to the Word Address (WA) pin during word bus size operation determines whether the most-significant or least-significant data bits are ported through the I/O_{0R-17R} pins in an Upper Word/Lower Word select fashion (note that when the right port is configured for word size operation, the Byte Address pin has no application and its input is “Don’t Care”[51]).

Device operation is accomplished by treating the WA pin as an additional address input and using standard cycle address and data setup/hold times. When transferring data in word (18-bit) bus match format, the unused $I/O_{18R-35R}$ pins are three-stated.

Byte (9-bit) Operation

Byte (9-bit) bus sizing operation is enabled when Bus Match Select (BM) is set to a logic “1” and the Bus Size Select (SIZE) pin is set to a logic “1”. In this mode, data is ported through I/O_{0R-8R} in four groups of 9-bit bytes. A particular 9-bit byte group is selected according to the levels applied to the Word Address (WA) and Byte Address (BA) input pins.

I/Os	Rank	WA	BA
$I/O_{27R-35R}$	Upper-MSB	1	1
$I/O_{18R-26R}$	Lower-MSB	1	0
I/O_{9R-17R}	Upper-MSB	0	1
I/O_{0R-8R}	Lower-MSB	0	0

Device operation is accomplished by treating the Word Address (WA) pin and the Byte Address (BA) pins as additional address inputs having standard cycle address and data setup/hold times. When transferring data in byte (9-bit) bus match format, the unused I/O_{9R-35R} pins are three-stated.

Note:

51. Even though a logic level applied to a “Don’t Care” input will not change the logical operation of the dual-port, inputs that are temporarily a “Don’t Care” (along with unused inputs) must not be allowed to float. They must be forced either HIGH or LOW.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C056V–10AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C056V–10BAC	BB172	172-Ball Ball Grid Array (BGA)	Commercial
12	CY7C056V–12AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C056V–12BAC	BB172	172-Ball Ball Grid Array (BGA)	Commercial
15	CY7C056V–15AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C056V–15AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C056V–15BAC	BB172	172-Ball Ball Grid Array (BGA)	Commercial
	CY7C056V–15BAI	BB172	172-Ball Ball Grid Array (BGA)	Industrial
20	CY7C056V–20AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C056V–20BAC	BB172	172-Ball Ball Grid Array (BGA)	Commercial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C057V–10AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C057V–10BAC	BB172	172-Ball Ball Grid Array (BGA)	Commercial
12	CY7C057V–12AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C057V–12BAC	BB172	172-Ball Ball Grid Array (BGA)	Commercial
15	CY7C057V–15AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C057V–15AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C057V–15BAC	BB172	172-Ball Ball Grid Array (BGA)	Commercial
	CY7C057V–15BAI	BB172	172-Ball Ball Grid Array (BGA)	Industrial
20	CY7C057V–20AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C057V–20BAC	BB172	172-Ball Ball Grid Array (BGA)	Commercial

Shaded areas contain advance information.

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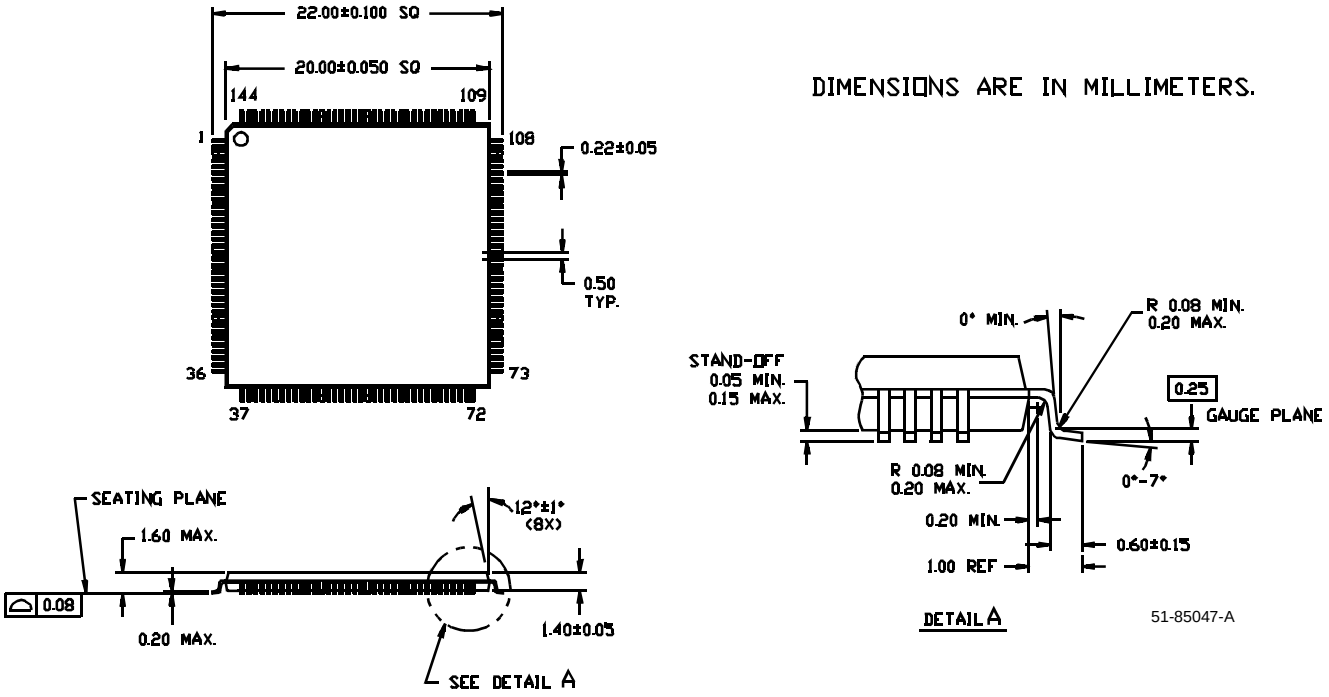
Package Diagrams

144-Pin Plastic Thin Quad Flat Pack (TQFP) A144



Package Diagrams (continued)

172-Ball BGA BB172