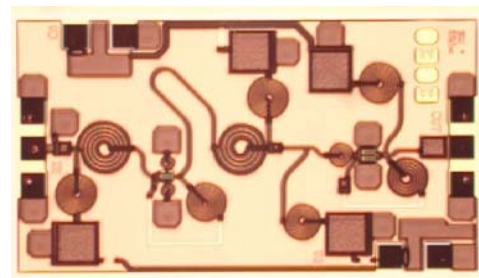


M/A-COM 1.5-6.5 GHz Low Noise Amplifier**MAALGM0006-DIE**

MAALGM0006-DIE

Features

- ◆ 3.5 dB Typical Noise Figure
- ◆ Variable Drain Voltage (3-6V) Operation
- ◆ GaAs MSAG™ Process
- ◆ Proven Manufacturability and Reliability
 - No Airbridges
 - Polyimide Scratch Protection
 - No Hydrogen Poisoning Susceptibility

**Description**

The MAALGM0006-Die is a 2-stage low noise amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MESFET Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- ◆ SatCom
- ◆ Radar

Electrical Characteristics: $T_B = 40^\circ\text{C}^1$, $Z_0 = 50\Omega$, $V_{DD} = 5\text{V}$, $I_{DQ} \approx 40 \text{ mA}^2$, $P_{in} = 5 \text{ dBm}$, $R_G \approx 5 \text{ k}\Omega$

Parameter	Symbol	Typical	Units
Bandwidth	f	1.5-6.5	GHz
Output Power	POUT	17.5	dBm
1-dB Compression Point	P _{1dB}	16	dB
Small Signal Gain	G	17	dB
Noise Figure	NF	3.5	dB
Input VSWR	VSWR	1.5:1	
Output VSWR	VSWR	1.5:1	
Gate Supply Current	I _{GG}	<1	mA
Drain Supply Current	I _{DD}	70	mA

1. T_B = MMIC Base Temperature
2. Adjust V_{GG} between -1.0 to -0.3V to achieve I_{DQ} indicated.

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Maximum Operating Conditions ³

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	10.0	dBm
Drain Supply Voltage	V_{DD}	+7.0	V
Gate Supply Voltage	V_{GG}	-2.0	V
Quiescent Drain Current (No RF, 40% I_{DSS})	I_{DQ}	70	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	0.5	W
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Die Attach Temperature		310	°C

3. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}	3.0	5.0	6.0	V
Gate Supply Voltage	V_{GG}	-1.0	-0.6	-0.3	V
Input Power	P_{IN}		5.0	8.0	dBm
Junction Temperature	T_J			150	°C
Thermal Resistance	Θ_{JC}		157		°C/W
MMIC Base Temperature	T_B			Note 4	°C

4. Maximum MMIC Base Temperature = $150^{\circ}\text{C} - \Theta_{JC} * V_{DD} * I_{DQ}$

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply $V_{GG} = -0.8\text{ V}$, $V_{DD} = 0\text{ V}$.
2. Ramp V_{DD} to desired voltage, typically 5 V.
3. Adjust V_{GG} to set I_{DQ} .
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.



Specifications subject to change without notice.

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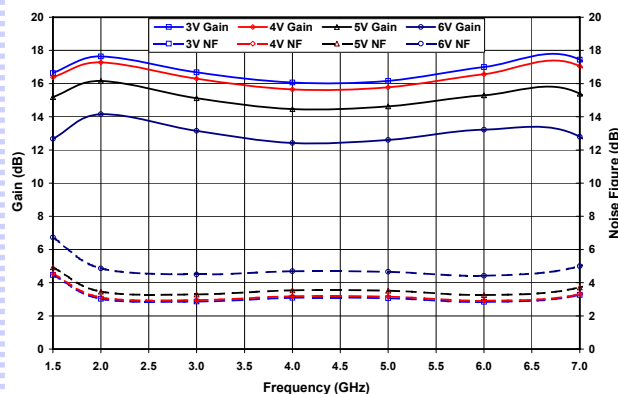


Figure 1. Gain and Noise Figure vs. Frequency and Drain Voltage at 25% IDSS

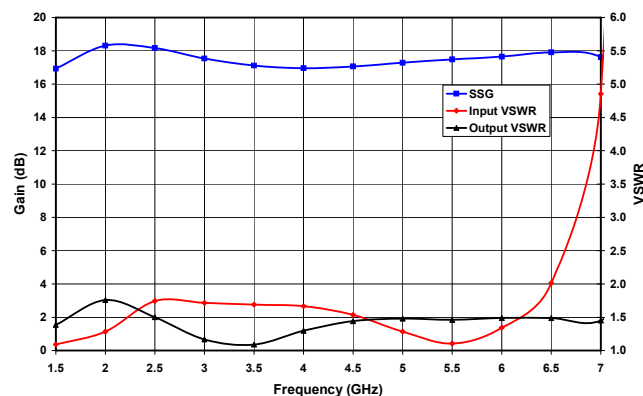
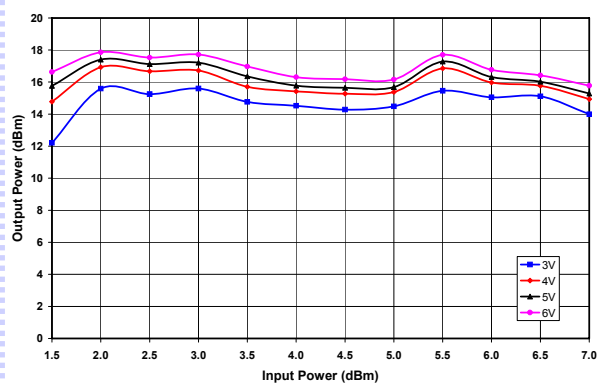
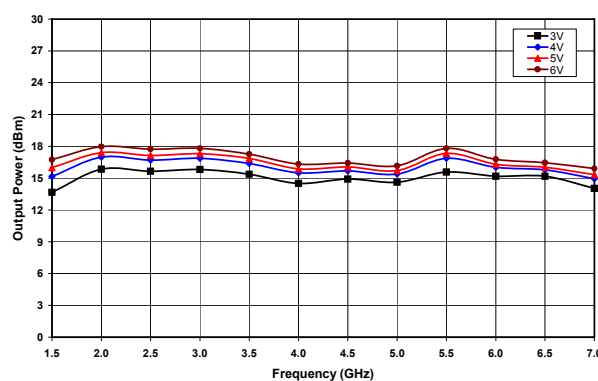
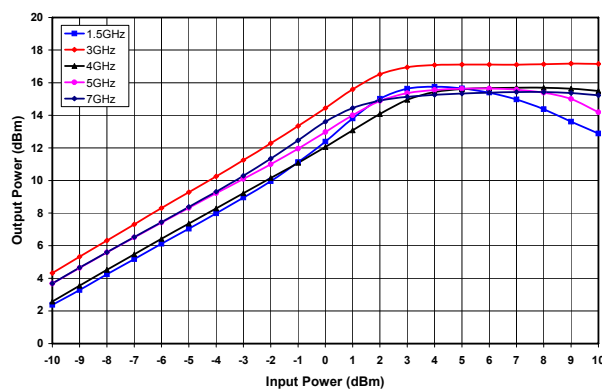
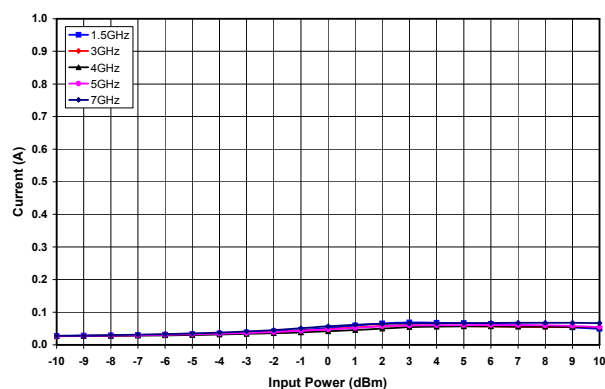
Figure 2. Small Signal Gain and Input and Output VSWR vs. Frequency at $V_D=5V$.Figure 3. Output Power vs. Frequency and Drain Voltage at $P_{1dB}=5dBm$ And 40% IDSS.

Figure 4. Saturated Output Power vs. Frequency and Drain Voltage at 40% IDSS.

Figure 5. Output Power vs. Input Power and Frequency at $V_D=5V$ And 40% IDSS.Figure 6. RF Drain Current vs. Input Power and Frequency at $V_D=5V$ And 40% IDSS.

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Mechanical Information

Chip Size: 2.939 x 1.637 x 0.075 mm (116 x 64 x 3 mils)

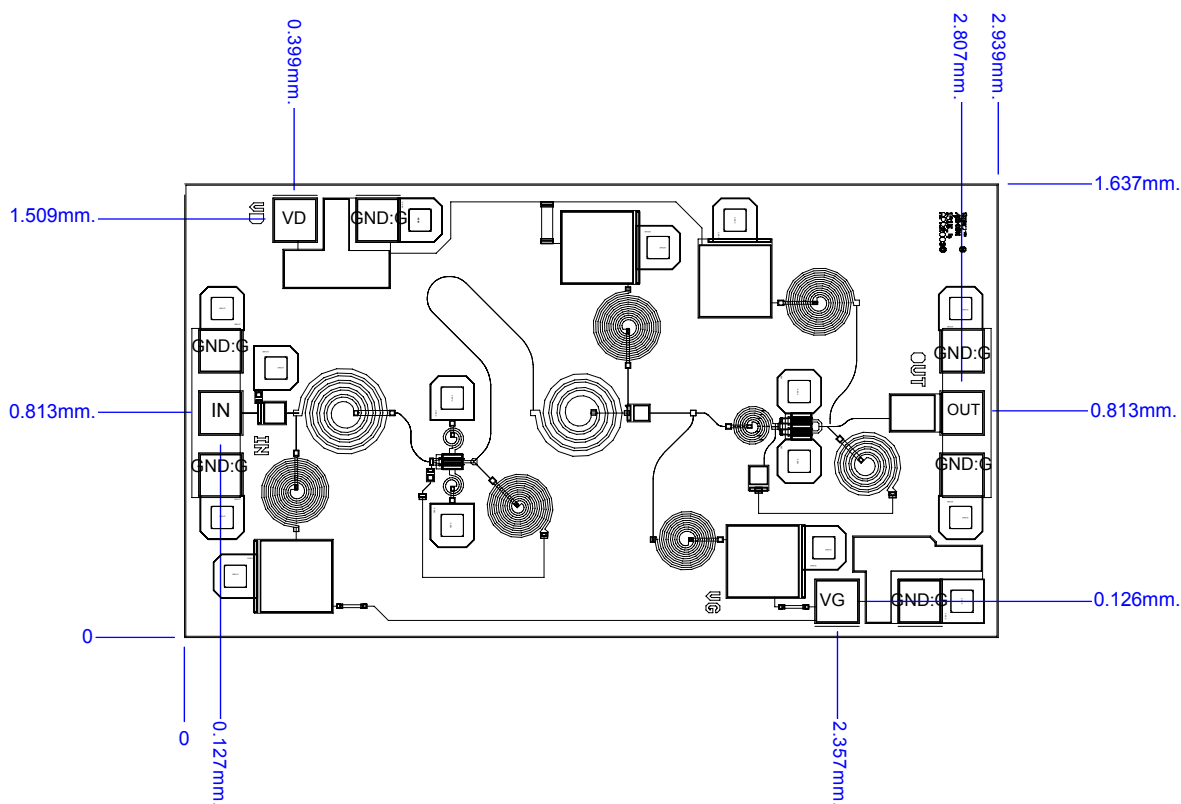


Figure 7. Die Layout

Chip edge to bond pad dimensions are shown to the center of the bond pad.

Bond Pad Dimensions

Pad	Size (μm)	Size (mils)
RF In and Out	150 x 150	6 x 6
DC Drain Supply Voltage VD	150 x 150	6 x 6
DC Gate Supply Voltage VG	150 x 150	6 x 6

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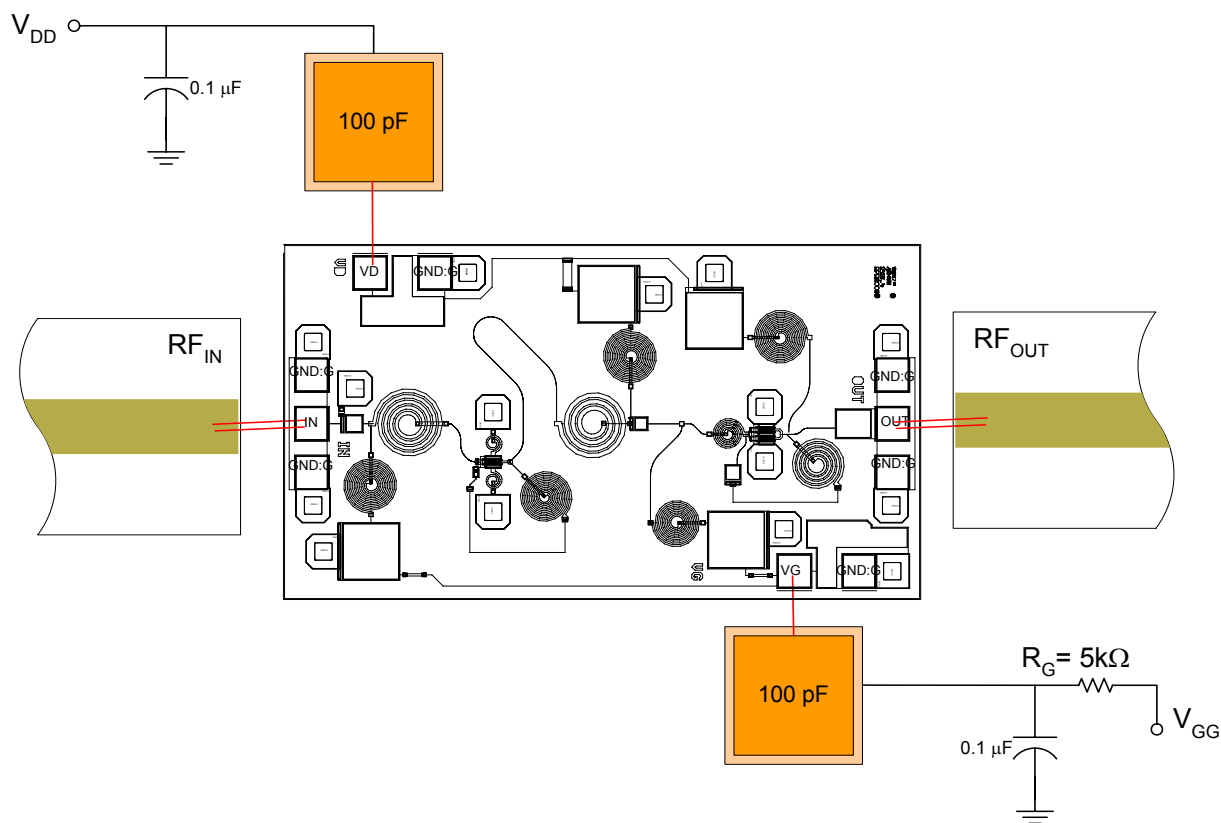


Figure 8. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization fixture for CW testing.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1-2 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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