



PSMN040-100MSE

N-channel 100 V 36.6 mΩ standard level MOSFET in LPAK33 designed specifically for high power PoE applications

26 March 2013

Product data sheet

1. General description

New standards and proprietary approaches are enabling Power-over-Ethernet (PoE) systems capable of delivering up to 90W to each powered device (PD). Such solutions place increased demands on the power sourcing equipment (PSE) in terms of “soft-start”, thermal management and power density requirements.

2. Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Low $R_{DS(on)}$ for low conduction losses
- Ultra reliable LPAK33 package for superior thermal and ruggedness performance
- Very low I_{DSS}

3. Applications

- High power PoE applications (60W and higher)
- IEEE802.3at and proprietary solutions

4. Quick reference data

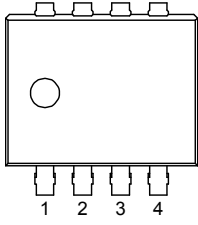
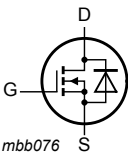
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_J \geq 25\text{ °C}$; $T_J \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$T_J = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	-	30	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	-	91	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_J = 25\text{ °C}$; Fig. 13	-	29.4	36.6	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $V_{DS} = 50\text{ V}$;	-	10.7	-	nC
$Q_{G(tot)}$	total gate charge	$T_J = 25\text{ °C}$; Fig. 14 ; Fig. 15	-	30	-	nC
Avalanche Ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 30\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ Ω}$; unclamped; Fig. 3	-	-	54	mJ

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN040-100MSE	LPAK33	Plastic single ended surface mounted package (LPAK33); 4 leads	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN040-100MSE	M40E10

8. Limiting values

Table 5. Limiting values

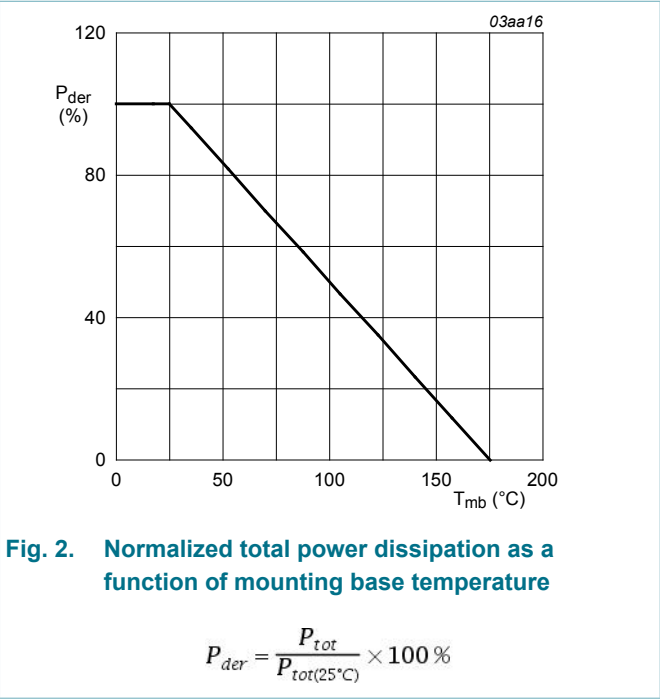
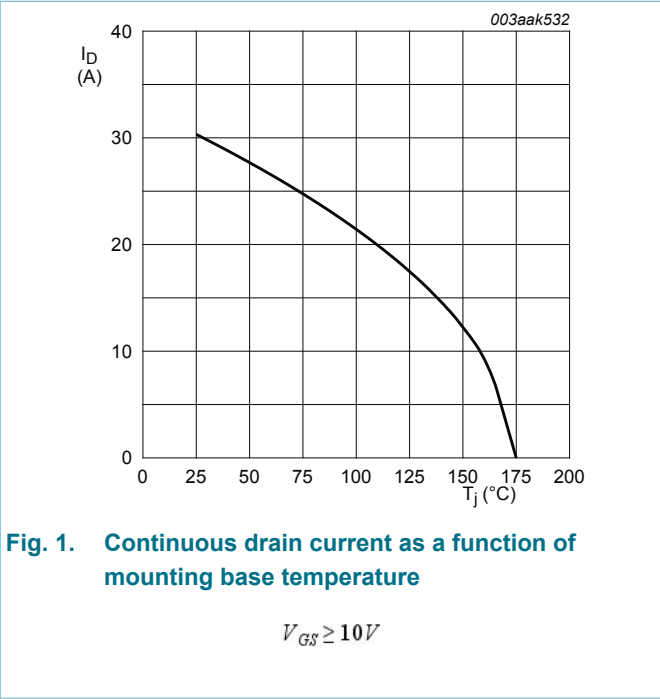
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 1	-	30	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^{\circ}\text{C}$; Fig. 1	-	21	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 4	-	121	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; Fig. 2	-	91	W
T_{stg}	storage temperature		-55	175	$^{\circ}\text{C}$

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Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	70	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	121	A
Avalanche Ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 30 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; unclamped; Fig. 3		-	54	mJ

[1] Continuous current is limited by package.



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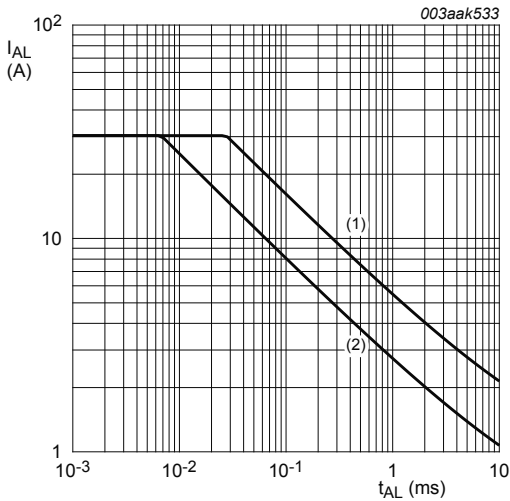


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_j = 25^\circ C$; (2) $T_j = 100^\circ C$

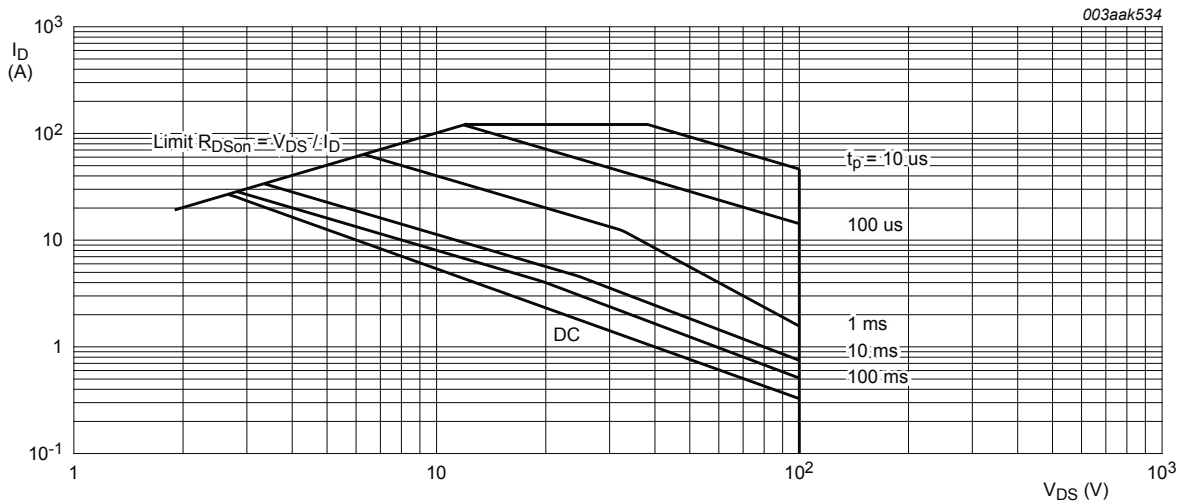


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

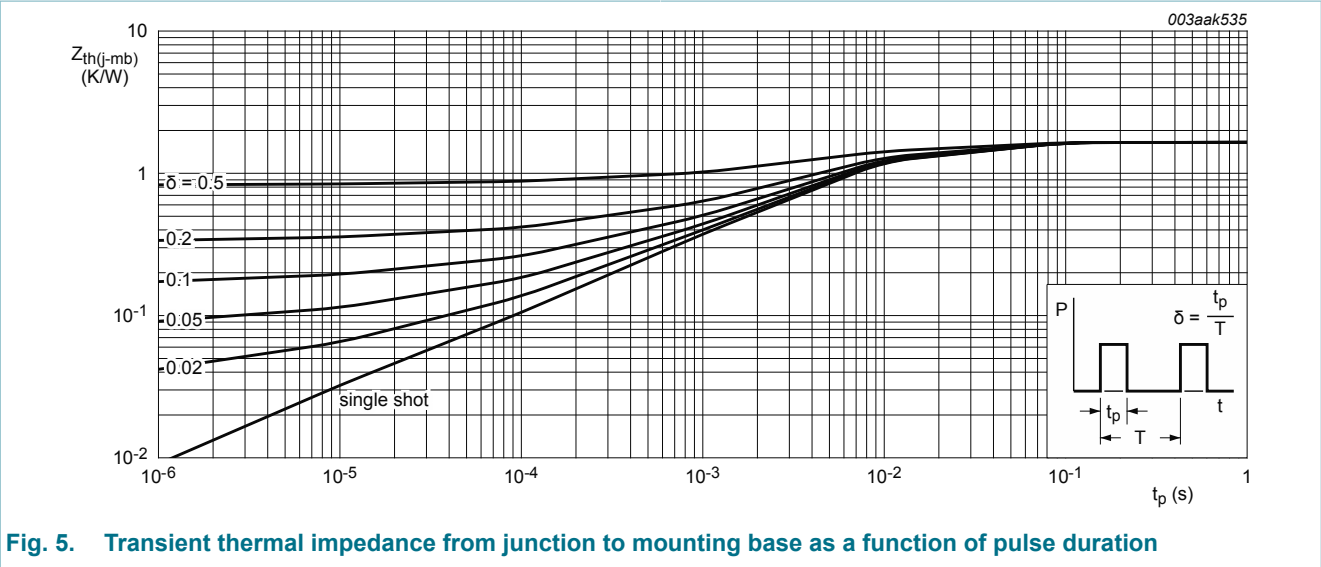
$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	1.44	1.65	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	100	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; Fig. 10; Fig. 11	2.3	3.3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; Fig. 10	-	-	4.6	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; Fig. 10	1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _J = 25 °C	-	0.05	1	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _J = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C	-	10	100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _J = 100 °C; Fig. 12; Fig. 13	-	-	66	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _J = 175 °C; Fig. 12; Fig. 13	-	-	99	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _J = 25 °C; Fig. 13	-	29.4	36.6	mΩ
R _G	gate resistance	f = 10 MHz	-	1.65	-	Ω

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		-	30	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C		-	24	-	nC
Q _{GS}	gate-source charge	I _D = 10 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		-	7.6	-	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	4.5	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	3.1	-	nC
Q _{GD}	gate-drain charge			-	10.7	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 10 A; V _{DS} = 50 V; T _j = 25 °C; Fig. 14 ; Fig. 15		-	5.6	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16		-	1470	-	pF
C _{oss}	output capacitance			-	110	-	pF
C _{rss}	reverse transfer capacitance			-	80	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 5 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	8.3	-	ns
t _r	rise time			-	14.1	-	ns
t _{d(off)}	turn-off delay time			-	18.7	-	ns
t _f	fall time			-	13	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 20 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17		-	0.82	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _j = 25 °C		-	41	-	ns
Q _r	recovered charge			-	75	-	nC

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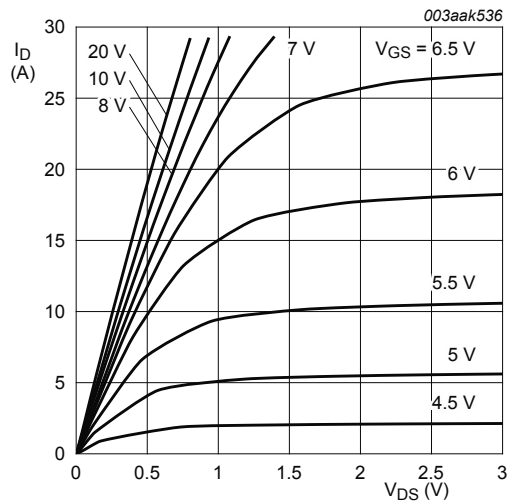


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

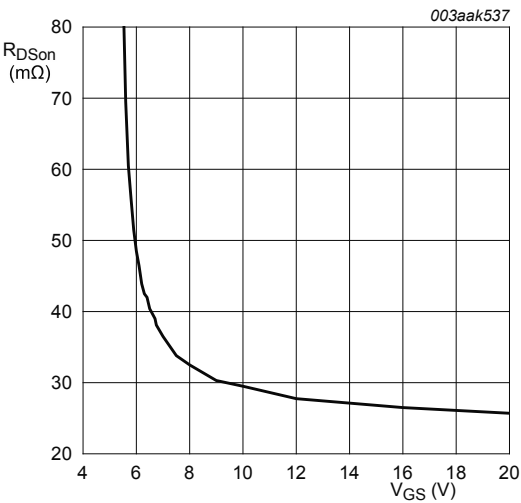


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$

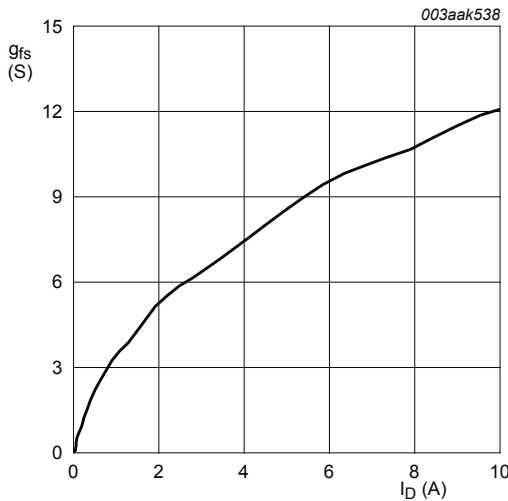


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; V_{DS} = 10\text{ V}$

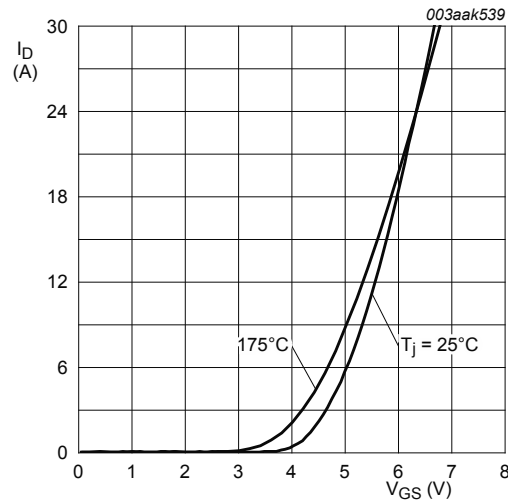


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

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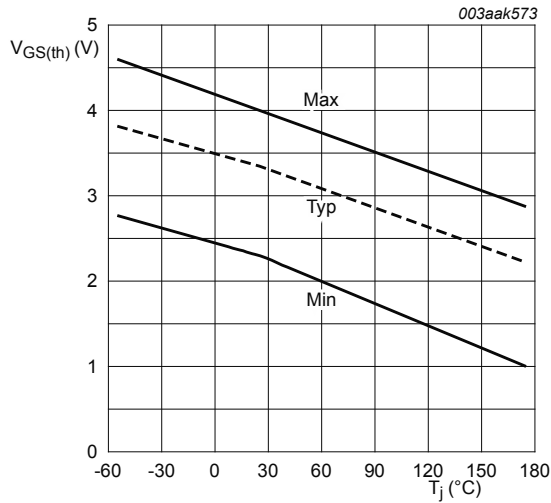


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

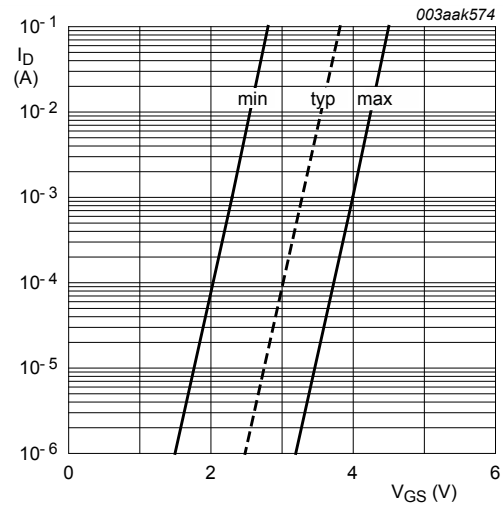


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_J = 25^\circ\text{C}; V_{DS} = 5 \text{ V}$$

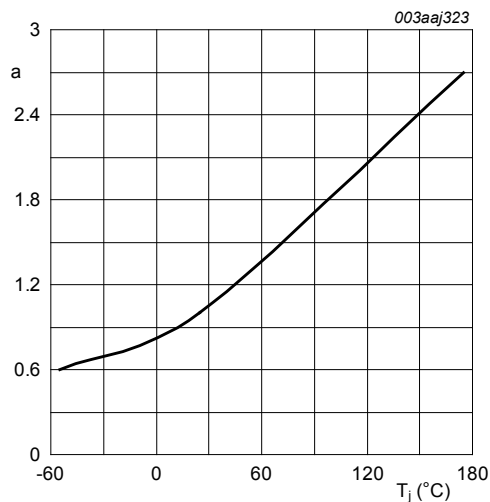


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\alpha = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

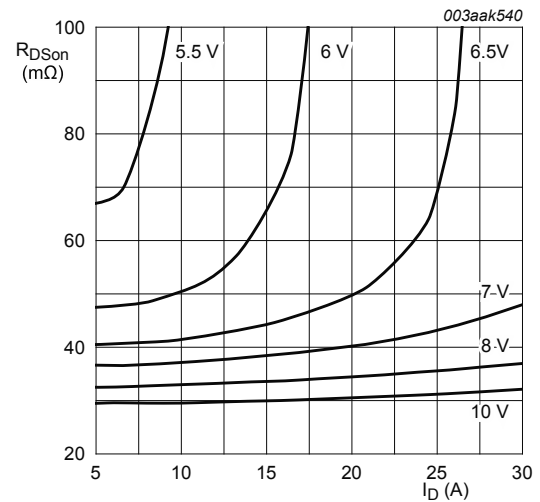


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$$T_J = 25^\circ\text{C}$$

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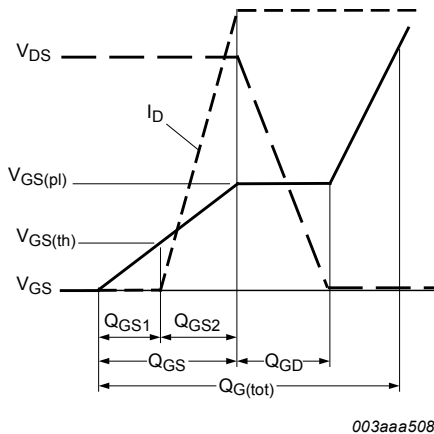


Fig. 14. Gate charge waveform definitions

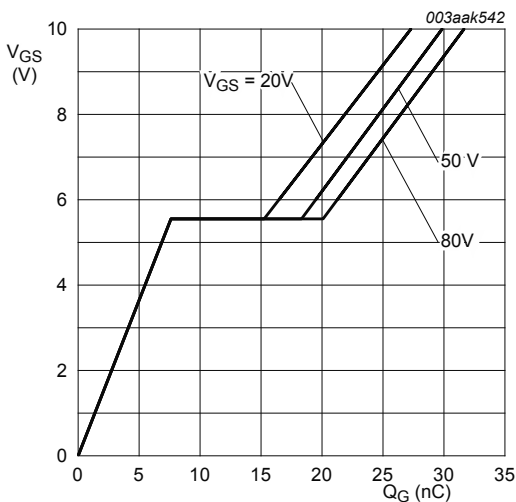


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^{\circ}C; I_D = 10A$

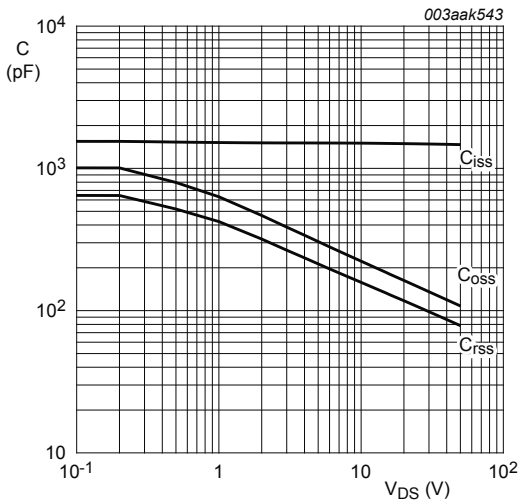


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

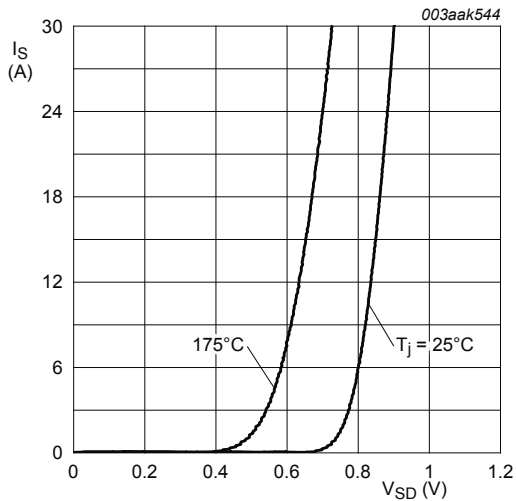


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

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11. Package outline

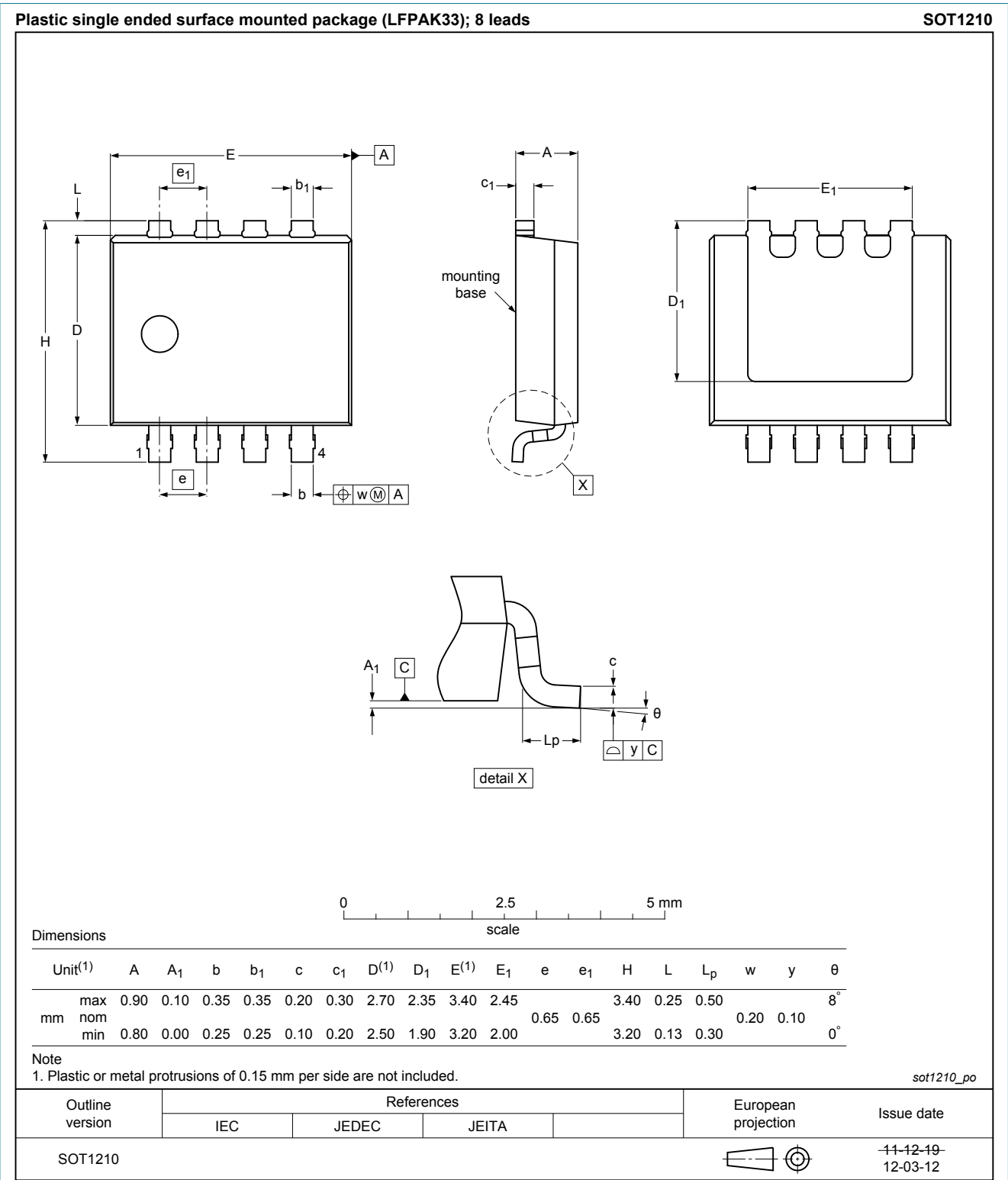


Fig. 18. Package outline LPAK33 (SOT1210)

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12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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