

NDF0610 / NDS0610

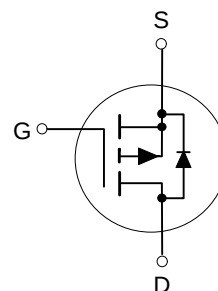
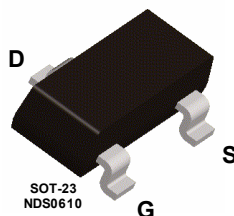
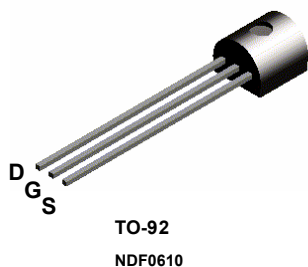
P-Channel Enhancement Mode Field Effect Transistor

General Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 180mA DC and can deliver pulsed currents up to 1A. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

- -0.18 and -0.12A, -60V. $R_{DS(ON)} = 10\Omega$
- Voltage controlled p-channel small signal switch
- High density cell design for low $R_{DS(ON)}$
- TO-92 and SOT-23 packages for both through hole and surface mount applications
- High saturation current



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDF0610	NDS0610	Units
V_{DS}	Drain-Source Voltage	-60	-60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1\text{ M}\Omega$)	-60	-60	V
V_{GSS}	Gate-Source Voltage - Continuous	± 20	± 20	V
	- Nonrepetitive ($t_p < 50\text{ }\mu\text{s}$)	± 30	± 30	V
I_D	Drain Current - Continuous	-0.18	-0.12	A
	- Pulsed	-1	-1	A
P_D	Maximum Power Dissipation $T_A = 25^\circ\text{C}$	0.8	0.36	W
	Derate above 25°C	5	2.9	mW/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/16" from case for 10 seconds	300		$^\circ\text{C}$

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	350	$^\circ\text{C/W}$
-----------------	---	-----	-----	--------------------

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _b = -10 μA	-60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -48 V, V _{GS} = 0 V			-1	μA
		T _j = 125°C			-200	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V			10	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V			-10	nA
ON CHARACTERISTICS (Note 1)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _b = -1 mA	-1	-2.4	-3.5	V
		T _j = 125°C	-0.6	-2.1	-3.2	
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _b = -0.5 A		3.6	10	Ω
		T _j = 125°C		5.9	16	
		V _{GS} = -4.5 V, I _b = -0.25 A		5.2	20	
		T _j = 125°C		7.9	30	
I _{D(on)}	On-State Drain Current	V _{GS} = -10 V, V _{DS} = -10 V	-0.6	-1.6		A
		V _{GS} = -4.5 V, V _{DS} = -10 V		-0.35		
g _{FS}	Forward Transconductance	V _{DS} = -10 V, I _b = -0.1 A	70	170		mS
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{DS} = -25 V, V _{GS} = 0 V, f = 1.0 MHz		40	60	pF
C _{oss}	Output Capacitance			11	25	pF
C _{rss}	Reverse Transfer Capacitance			3.2	5	pF
SWITCHING CHARACTERISTICS (Note 1)						
t _{D(on)}	Turn - On Delay Time	V _{DD} = -25 V, I _b = -0.18 A, V _{GS} = -10 V, R _{GEN} = 25 Ω		7	10	nS
t _r	Turn - On Rise Time			5	15	nS
t _{D(off)}	Turn - Off Delay Time			13	15	nS
t _f	Turn - Off Fall Time			10	20	nS
Q _g	Total Gate Charge	V _{DS} = -48 V, I _b = -0.5 A, V _{GS} = -10 V		1.43		nC
Q _{gs}	Gate-Source Charge			0.6		nC
Q _{gd}	Gate-Drain Charge			0.25		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I _S	Maximum Continuous Source Current				-0.18	A
I _{SM}	Maximum Pulse Source Current (Note 1)				-1	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _s = -0.5 A (Note 1)		-1.2	-1.5	V
		T _j = 125°C		-0.98	-1.3	
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _s = -0.5 A, dI _F /dt = 100 A/μs		40		ns
I _{rr}	Reverse Recovery Current			2.8		A

Note:

1. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

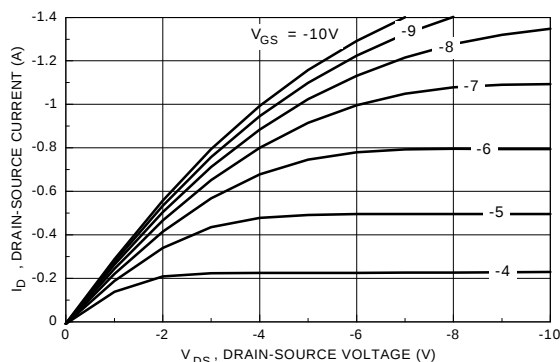


Figure 1. On-Region Characteristics

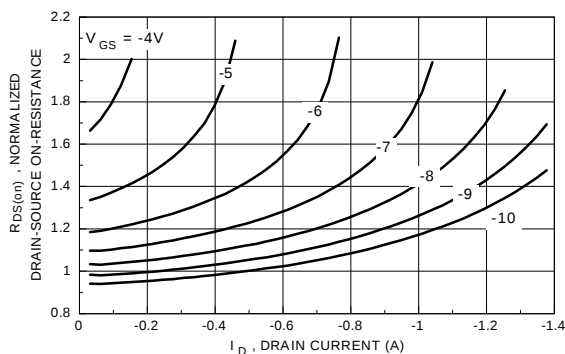


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

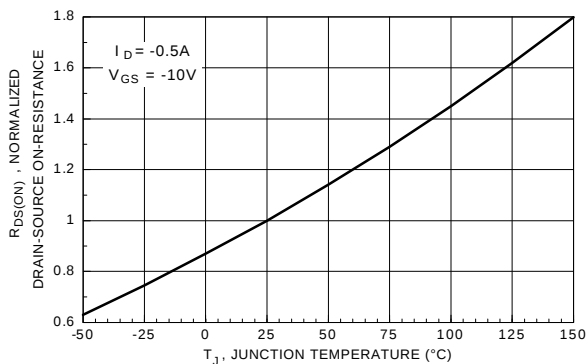


Figure 3. On-Resistance Variation with Temperature

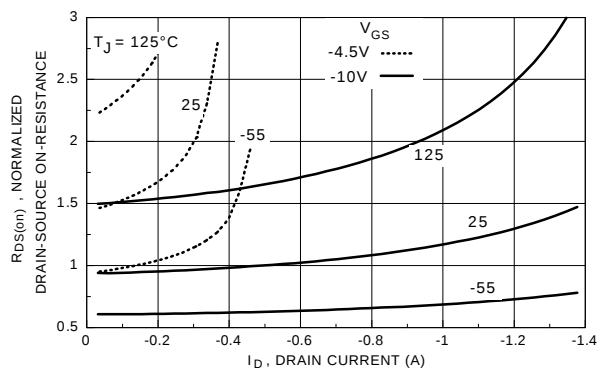


Figure 4. On-Resistance Variation with Drain Current and Temperature

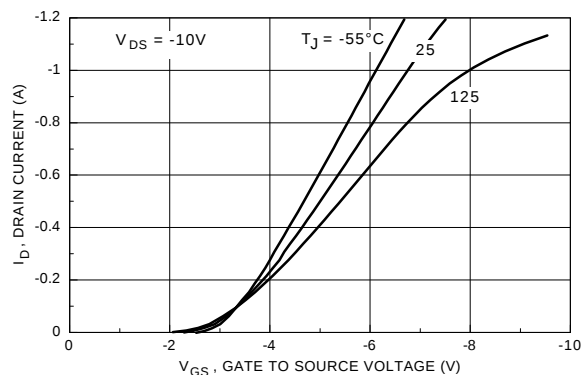


Figure 5. Transfer Characteristics

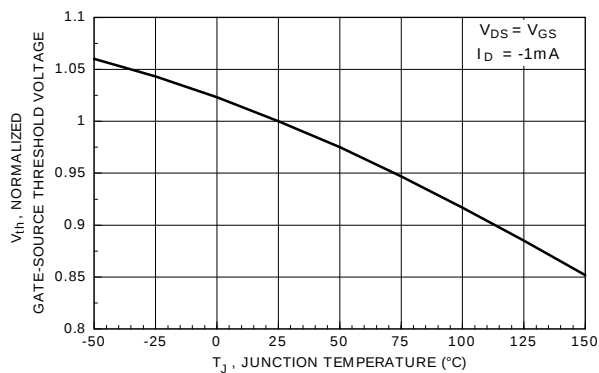


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

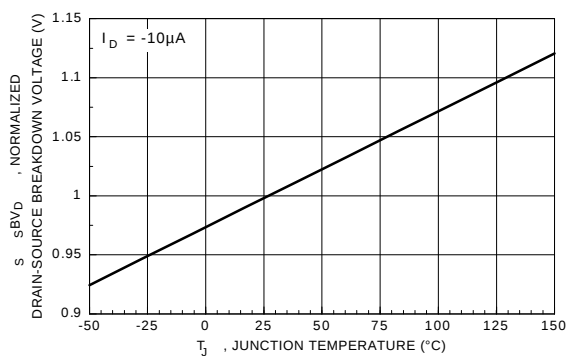


Figure 7. Breakdown Voltage Variation with Temperature

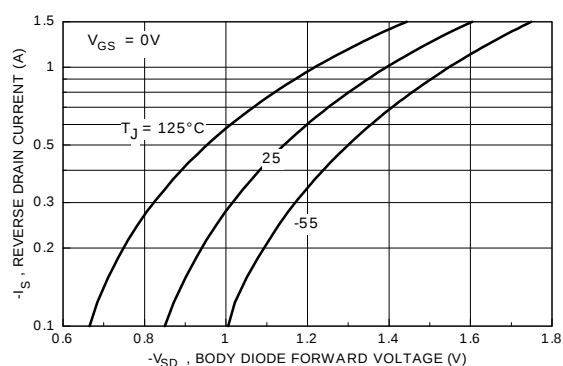


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

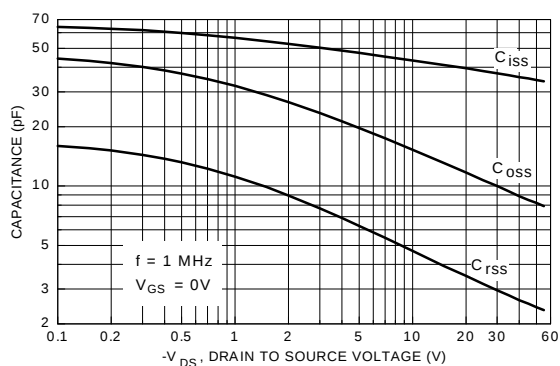


Figure 9. Capacitance Characteristics

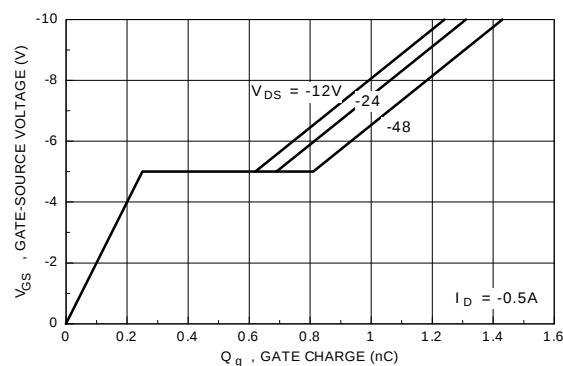


Figure 10. Gate Charge Characteristics

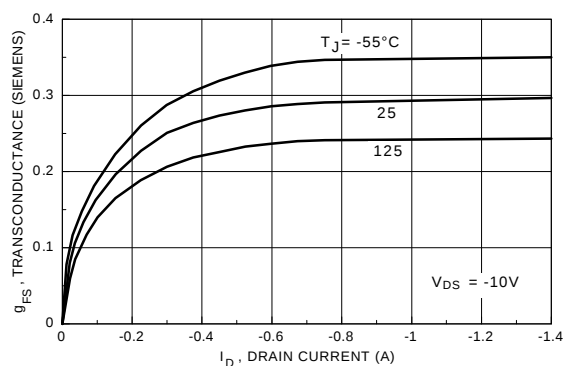
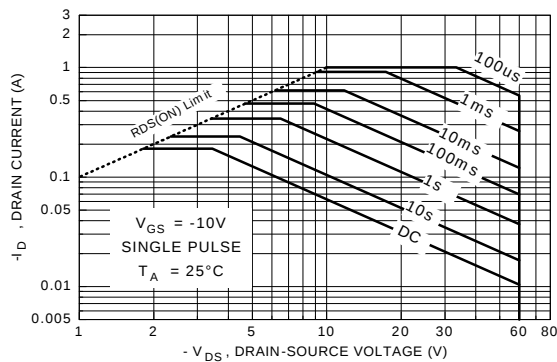


Figure 11. Transconductance Variation with Drain Current and Temperature

Typical Electrical Characteristics (continued)



**Figure 12. NDF0610 (TO-92)
Maximum Safe Operating Area**

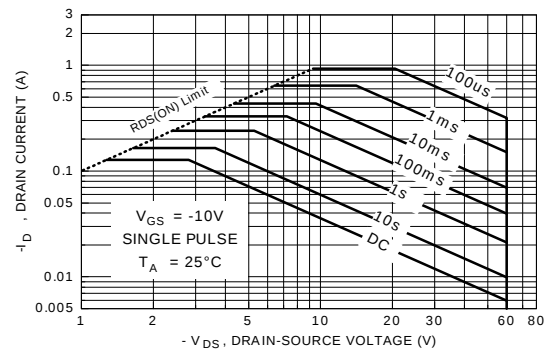


Figure 13. NDS0610 (SOT-23) Maximum Safe Operating Area

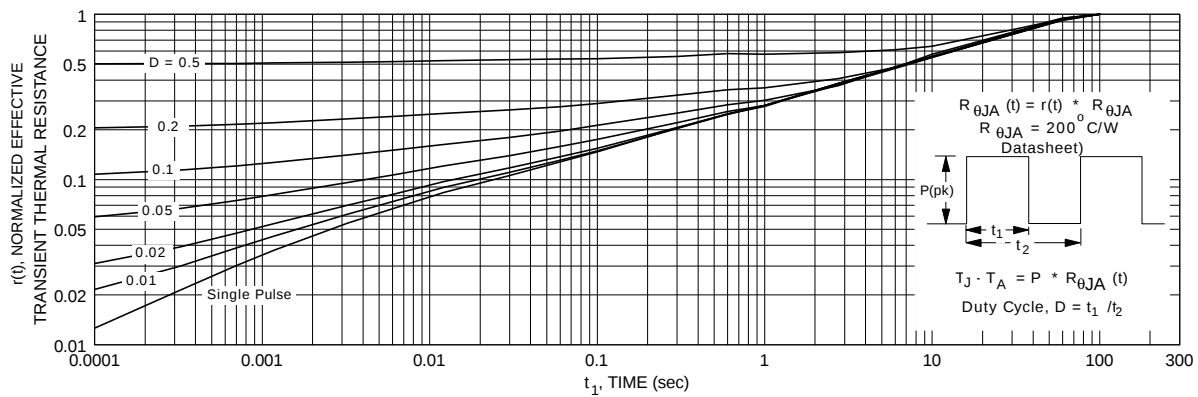


Figure 14. NDF0610 (TO-92) Transient Thermal Response Curve.

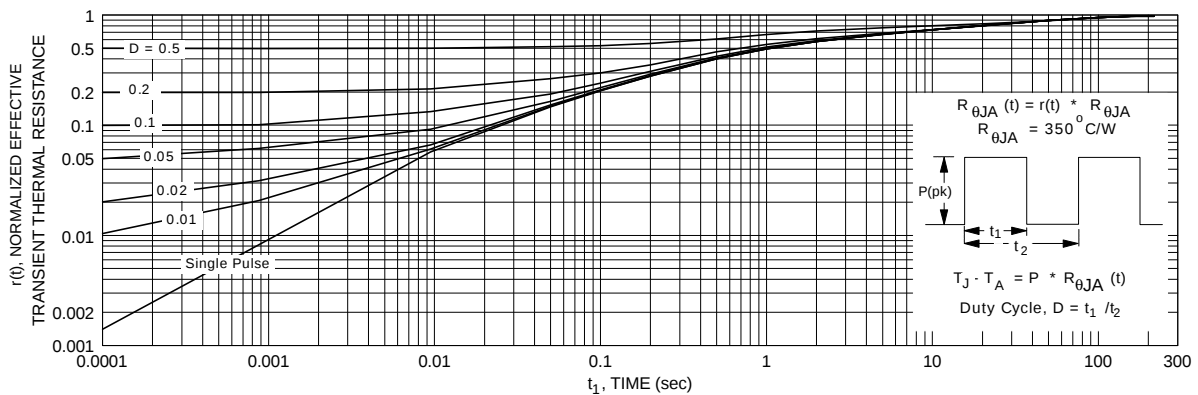


Figure 15. NDS0610 (SOT-23) Transient Thermal Response Curve.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE [™]	FAST [™]	PowerTrench [®]	SyncFET [™]
Bottomless [™]	GlobalOptoisolator [™]	QFET [™]	TinyLogic [™]
CoolFET [™]	GTO [™]	QS [™]	UHC [™]
CROSSVOLT [™]	HiSeC [™]	QT Optoelectronics [™]	VCX [™]
DOVE [™]	ISOPLANAR [™]	Quiet Series [™]	
E ² CMOS [™]	MICROWIRE [™]	SILENT SWITCHER [®]	
EnSigna [™]	OPTOLOGIC [™]	SMART START [™]	
FACT [™]	OPTOPLANAR [™]	SuperSOT [™] -3	
FACT Quiet Series [™]	PACMAN [™]	SuperSOT [™] -6	
FAST [®]	POP [™]	SuperSOT [™] -8	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.