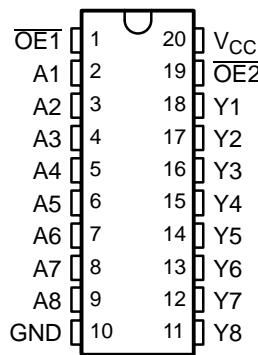


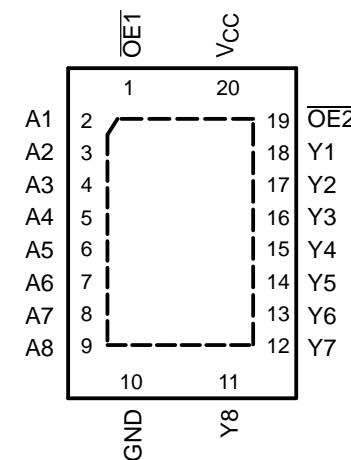
## FEATURES

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.1 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )

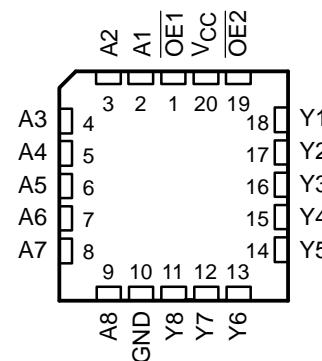
**SN54LVC541A . . . J OR W PACKAGE  
SN74LVC541A . . . DB, DGV, DW, NS,  
OR PW PACKAGE**  
(TOP VIEW)



**SN74LVC541A . . . RGY PACKAGE  
(TOP VIEW)**



**SN54LVC541A . . . FK PACKAGE  
(TOP VIEW)**



## DESCRIPTION/ORDERING INFORMATION

The SN54LVC541A octal buffer/driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC541A octal buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-40^\circ\text{C}$ to $85^\circ\text{C}$	QFN – RGY	Reel of 1000	SN74LVC541ARGYR	LC541A
	SOIC – DW	Tube of 25	SN74LVC541ADW	LVC541A
		Reel of 2000	SN74LVC541ADWR	
	SOP – NS	Reel of 2000	SN74LVC541ANSR	LVC541A
	SSOP – DB	Reel of 2000	SN74LVC541ADBR	LC541A
	TSSOP – PW	Tube of 70	SN74LVC541APW	LC541A
		Reel of 2000	SN74LVC541APWR	
		Reel of 250	SN74LVC541APWT	
$-55^\circ\text{C}$ to $125^\circ\text{C}$	TVSOP – DGV	Reel of 2000	SN74LVC541ADGVR	LC541A
	CDIP – J	Tube of 20	SNJ54LVC541AJ	SNJ54LVC541AJ
	CFP – W	Tube of 85	SNJ54LVC541AW	SNJ54LVC541AW
	LCCC – FK	Tube of 55	SNJ54LVC541AFK	SNJ54LVC541AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**SN54LVC541A, SN74LVC541A  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

SCAS298M—JANUARY 1993—REVISED MAY 2005

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## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The 'LVC541A devices are ideal for driving bus lines or buffering memory address registers.

These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

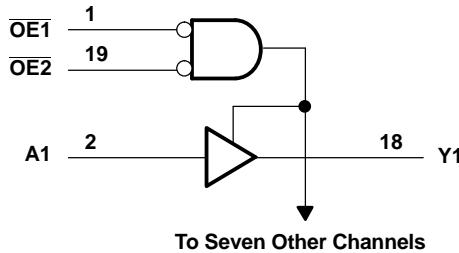
These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**FUNCTION TABLE**

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance	DB package <sup>(4)</sup>	70	°C/W
		DGV package <sup>(4)</sup>	92	
		DW package <sup>(4)</sup>	58	
		NS package <sup>(4)</sup>	60	
		PW package <sup>(4)</sup>	83	
		RGY package <sup>(5)</sup>	37	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

**SN54LVC541A, SN74LVC541A  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

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**Recommended Operating Conditions<sup>(1)</sup>**

		SN54LVC541A		SN74LVC541A		UNIT		
		MIN	MAX	MIN	MAX			
V <sub>CC</sub>	Supply voltage	Operating		2	3.6	1.65	3.6	V
		Data retention only		1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.65 × V <sub>CC</sub>		V	
		V <sub>CC</sub> = 2.3 V to 2.7 V			1.7			
		V <sub>CC</sub> = 2.7 V to 3.6 V		2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.35 × V <sub>CC</sub>		V	
		V <sub>CC</sub> = 2.3 V to 2.7 V			0.7			
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8		0.8		
V <sub>I</sub>	Input voltage			0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		3-state		0	5.5	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V				-4	mA	
		V <sub>CC</sub> = 2.3 V				-8		
		V <sub>CC</sub> = 2.7 V		-12		-12		
		V <sub>CC</sub> = 3 V		-24		-24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V				4	mA	
		V <sub>CC</sub> = 2.3 V				8		
		V <sub>CC</sub> = 2.7 V		12		12		
		V <sub>CC</sub> = 3 V		24		24		
T <sub>A</sub>	Operating free-air temperature			-55	125	-40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC541A			SN74LVC541A			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	1.65 V to 3.6 V				V <sub>CC</sub> - 0.2			V
		2.7 V to 3.6 V	V <sub>CC</sub> - 0.2						
	I <sub>OH</sub> = -4 mA	1.65 V				1.2			
	I <sub>OH</sub> = -8 mA	2.3 V				1.7			
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V		0.2					
	I <sub>OL</sub> = 4 mA	1.65 V				0.45			
	I <sub>OL</sub> = 8 mA	2.3 V				0.7			
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			0.4			
	I <sub>OL</sub> = 24 mA	3 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V		±5			±5	µA	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0					±10	µA	
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V		±15			±10	µA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	3.6 V		10		10	µA	
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>				10		10		
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V		500			500	µA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4			4	pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		5.5			5.5	pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This applies in the disabled state only.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC541A				UNIT	
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			
			MIN	MAX	MIN	MAX		
t <sub>pd</sub>	A	Y	5.6		1	5.1	ns	
t <sub>en</sub>	OE	Y	7.5		1	7	ns	
t <sub>dis</sub>	OE	Y	7.7		1	7	ns	

**SN54LVC541A, SN74LVC541A  
OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS**

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**Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

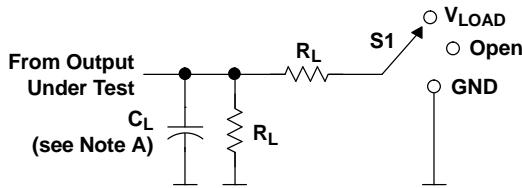
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC541A						UNIT		
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V				
			MIN	MAX	MIN	MAX	MIN	MAX			
t <sub>pd</sub>	A	Y	1	15.7	1	7.8	1	5.6	1.5	5.1	
t <sub>en</sub>	OE	Y	1	17.5	1	10.5	1	7.5	1.5	7	
t <sub>dis</sub>	OE	Y	1	16.5	1	9	1	7.7	1.5	7	
t <sub>sk(o)</sub>									1	ns	

**Operating Characteristics**

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
		TYP	TYP	TYP	
	f = 10 MHz				
C <sub>pd</sub> Power dissipation capacitance per buffer/driver	Outputs enabled	65	58	33	pF
	Outputs disabled	2	2	2	

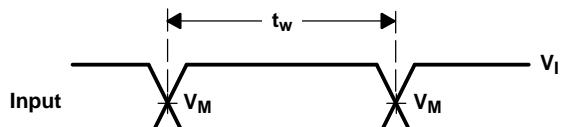
PARAMETER MEASUREMENT INFORMATION



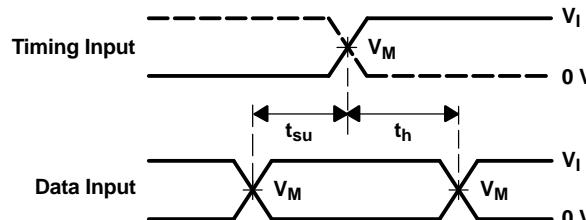
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

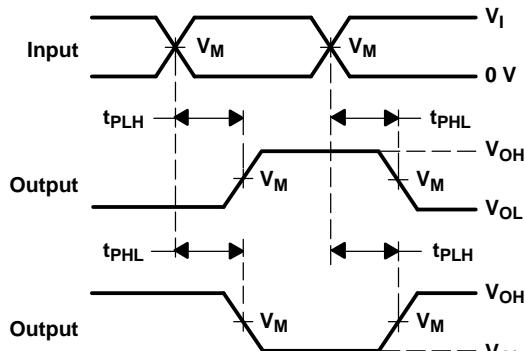
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



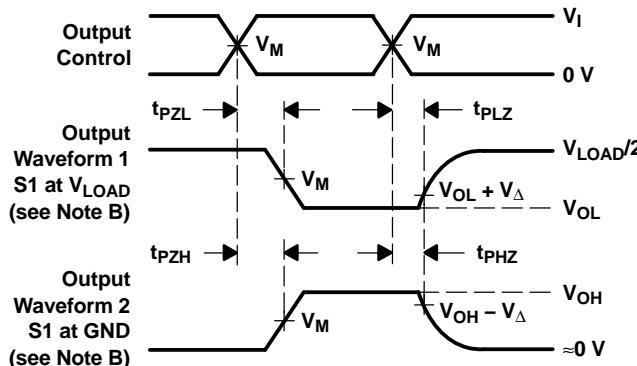
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9759501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9759501Q2A SNJ54LVC541AFK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9759501QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9759501QR A SNJ54LVC541AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
5962-9759501QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9759501QS A SNJ54LVC541AW	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADBLE	OBsolete	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVC541ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC541ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541APWLE	OBsolete	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVC541APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74LVC541ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC541A	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LVC541AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9759501Q2A SNJ54LVC541AFK	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LVC541AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9759501QR A SNJ54LVC541AJ	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SNJ54LVC541AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9759501QS A SNJ54LVC541AW	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54LVC541A, SN74LVC541A :**

• Catalog: [SN74LVC541A](#)

• Automotive: [SN74LVC541A-Q1](#), [SN74LVC541A-Q1](#)

• Enhanced Product: [SN74LVC541A-EP](#), [SN74LVC541A-EP](#)

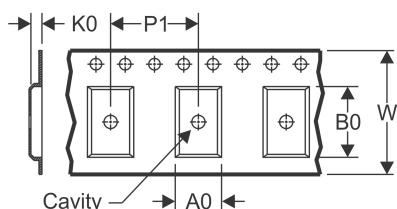
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- Military: [SN54LVC541A](#)

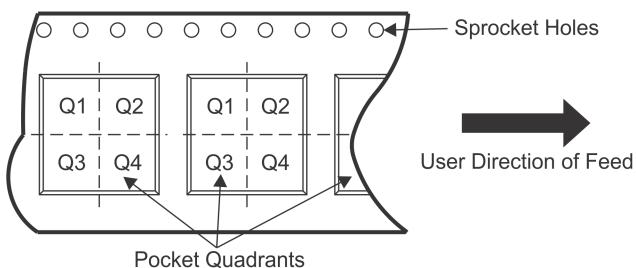
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

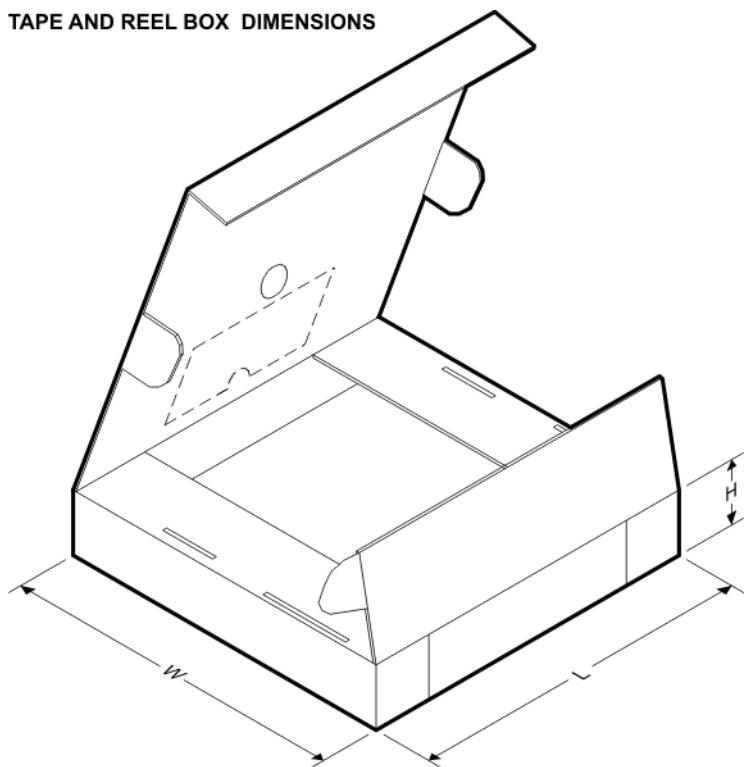
**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC541ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC541ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC541ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVC541ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVC541APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC541APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC541ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


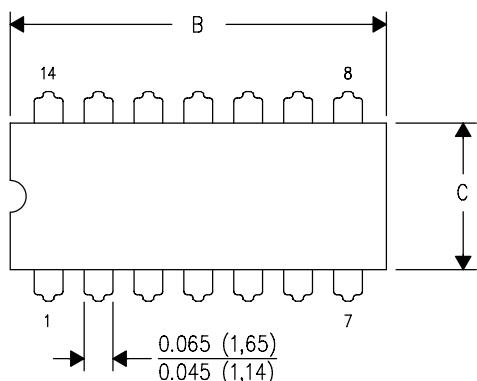
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC541ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVC541ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74LVC541ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVC541ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVC541APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC541APWT	TSSOP	PW	20	250	367.0	367.0	38.0
SN74LVC541ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

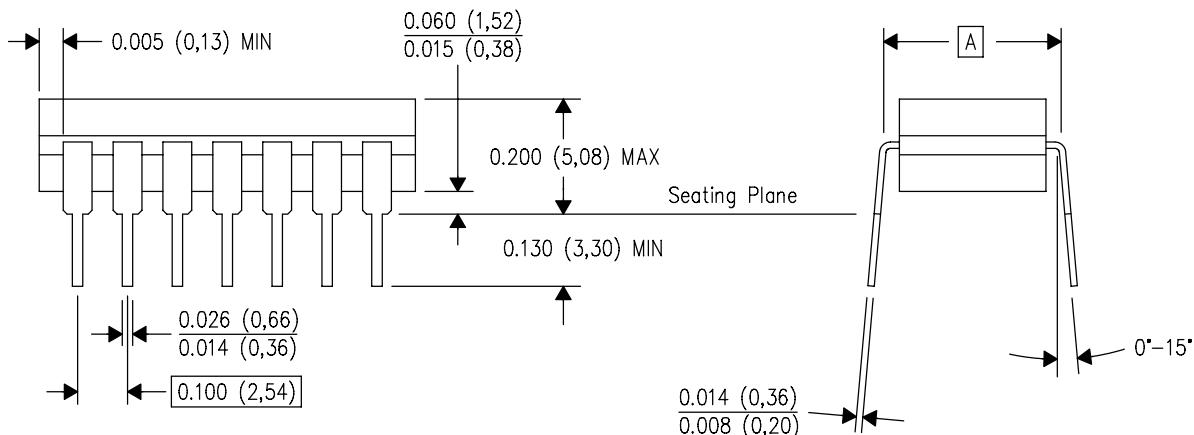
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

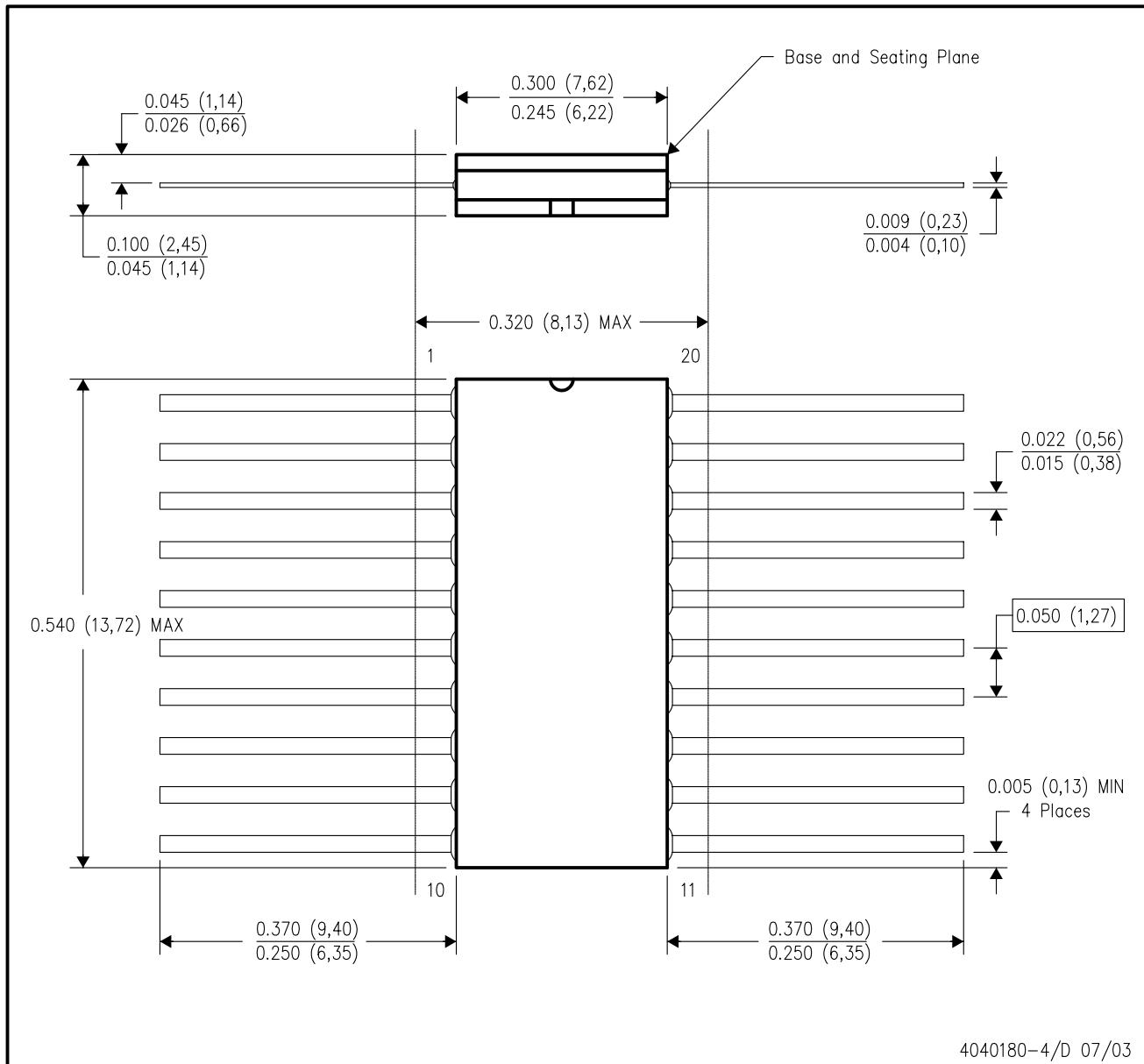


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



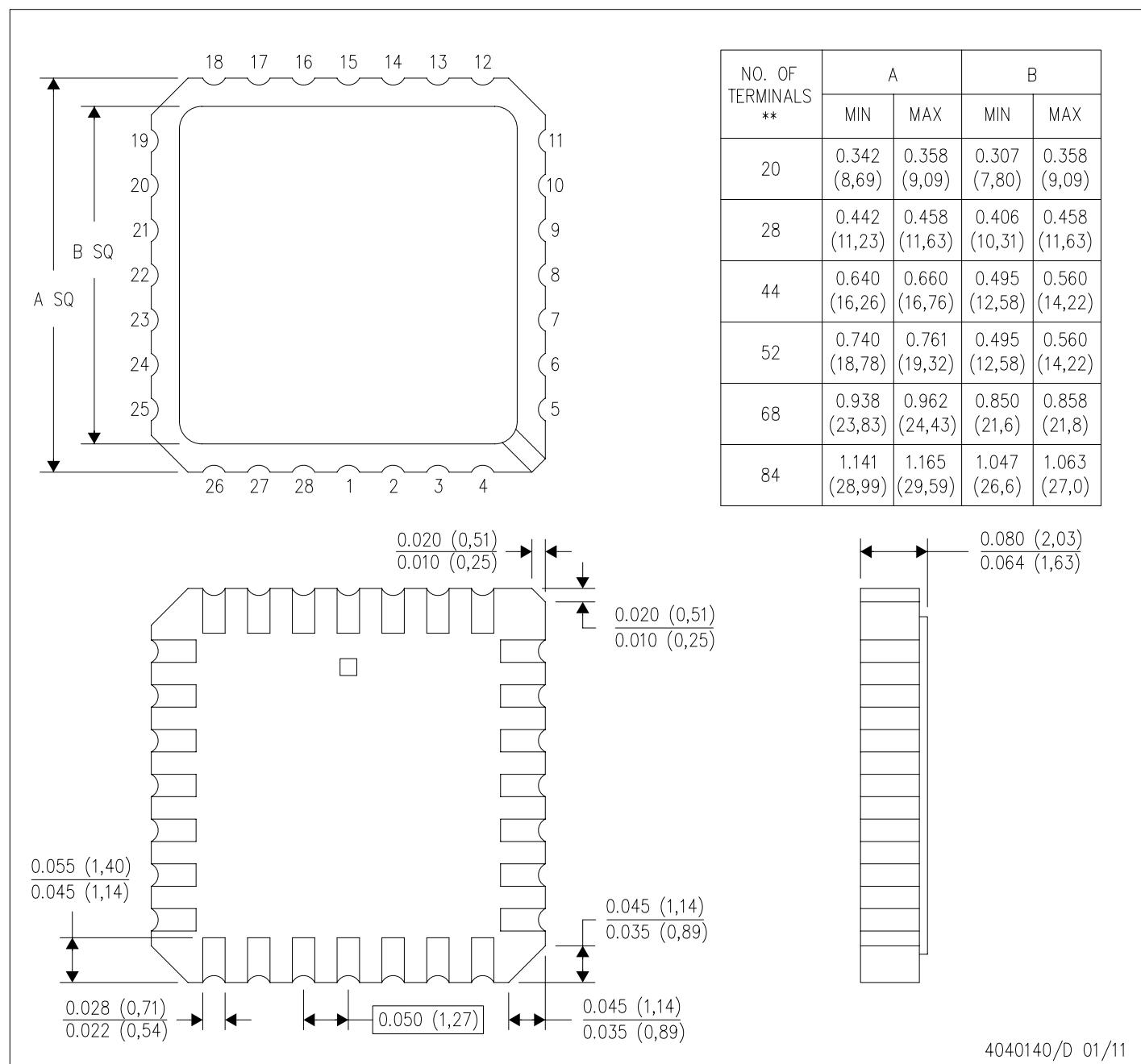
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

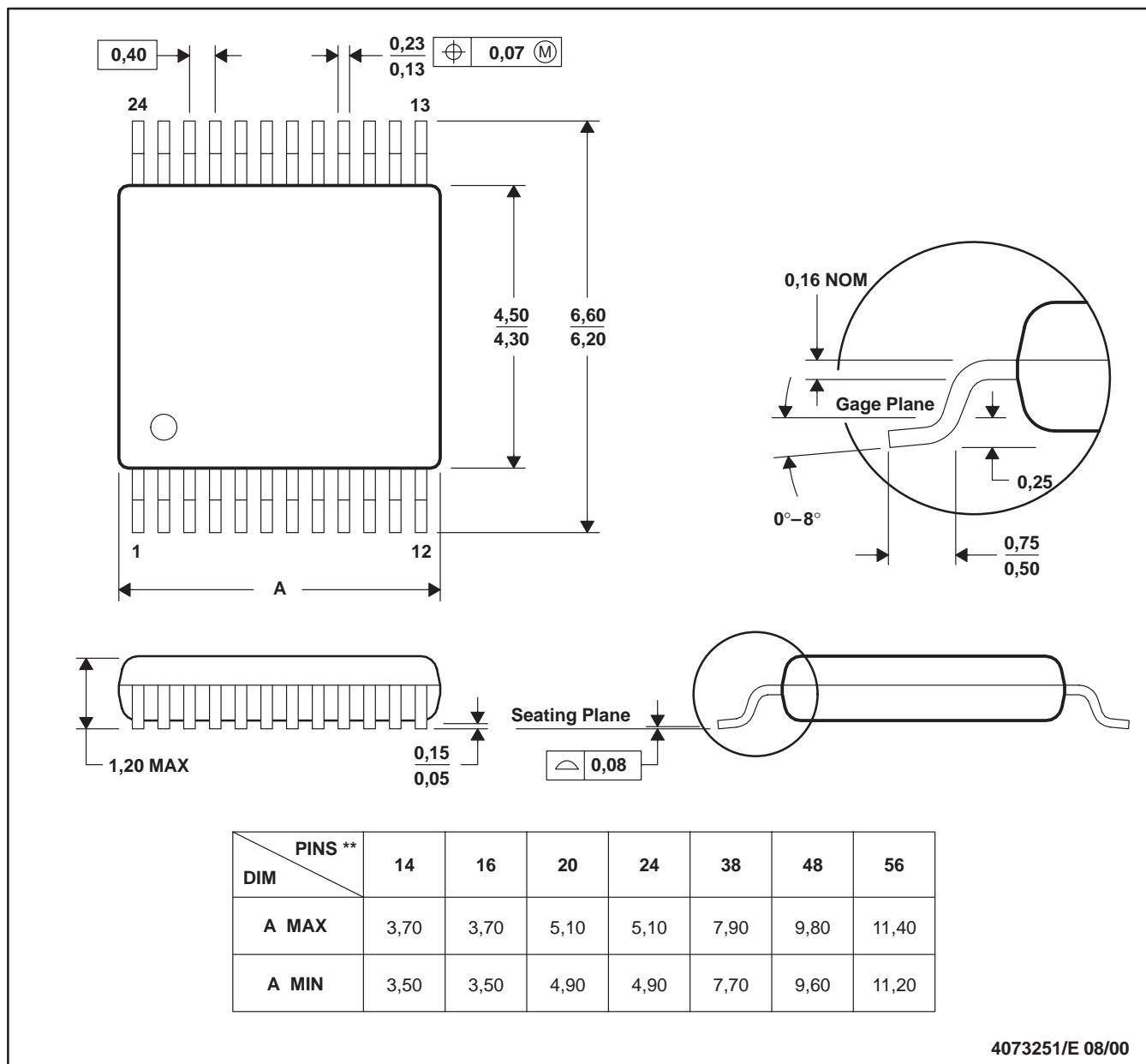
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

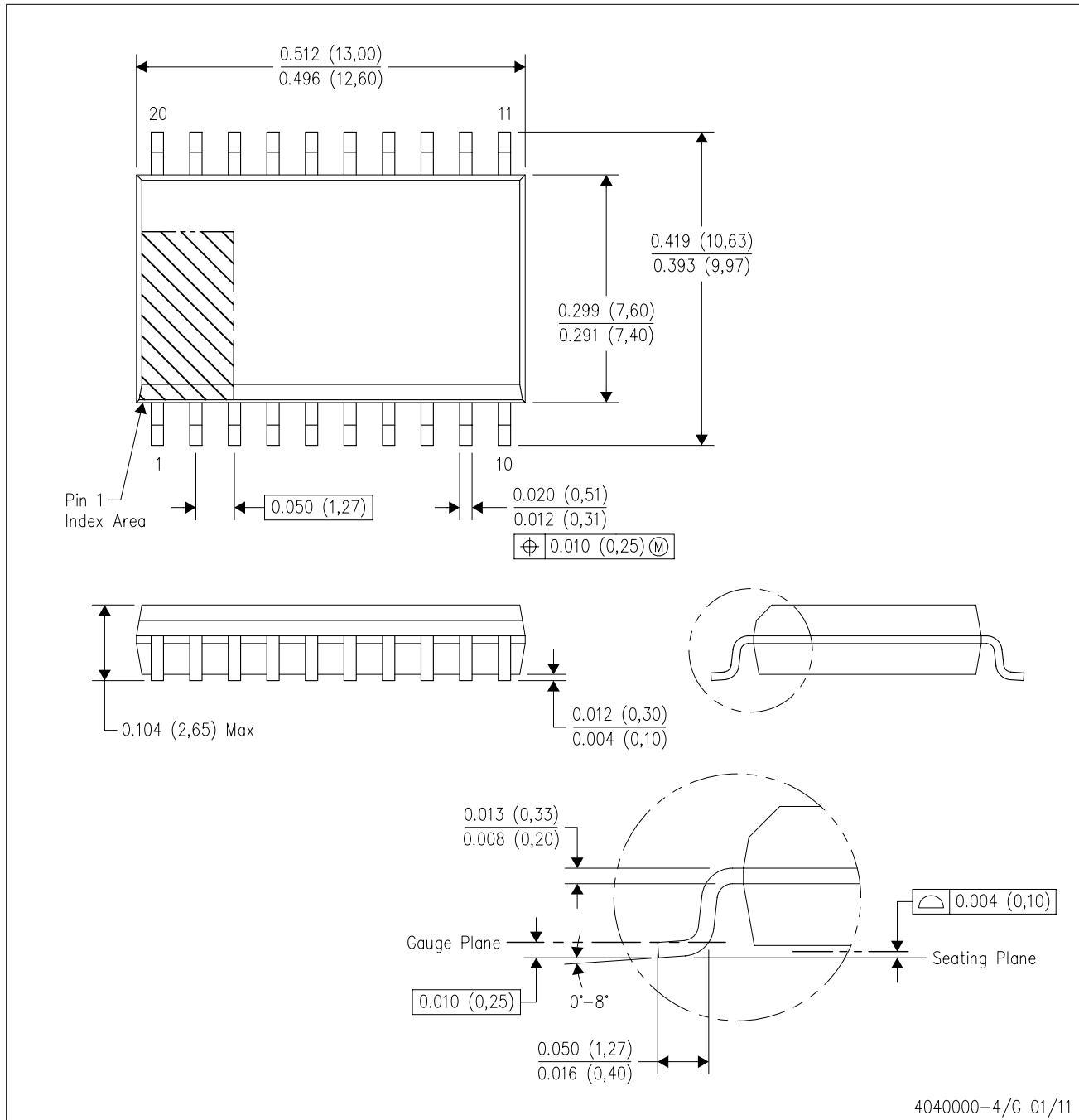
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

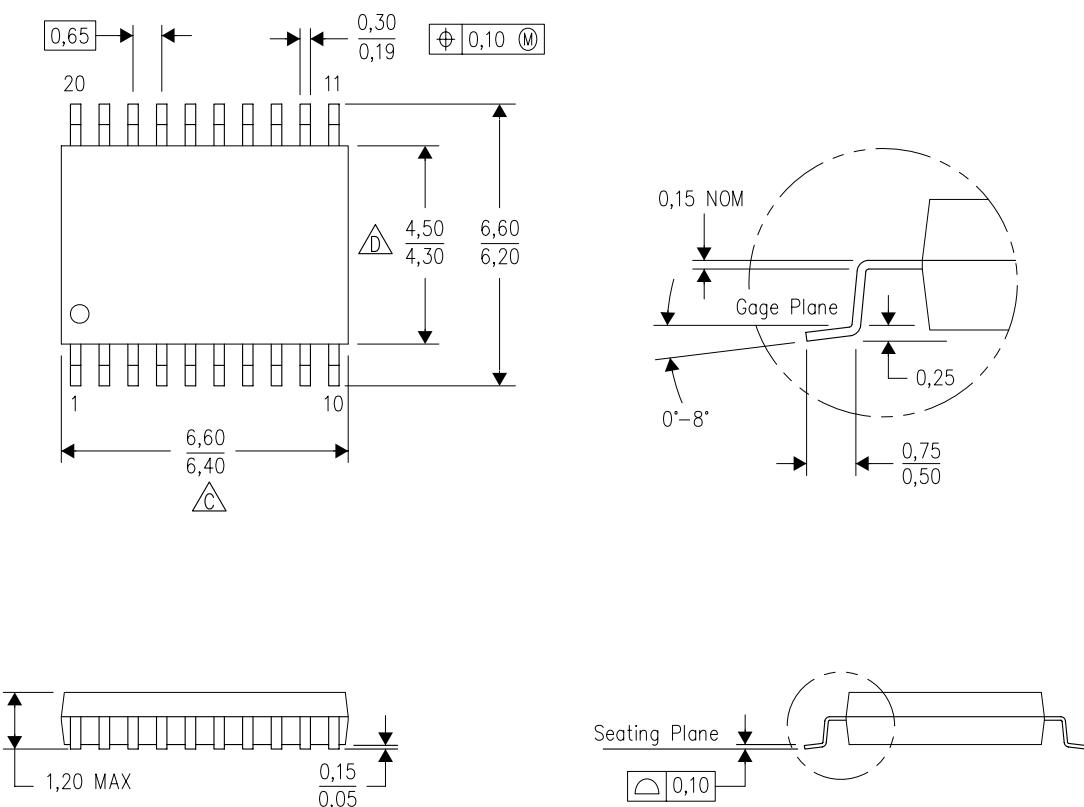


NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

 Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E Falls within JEDEC MO-153

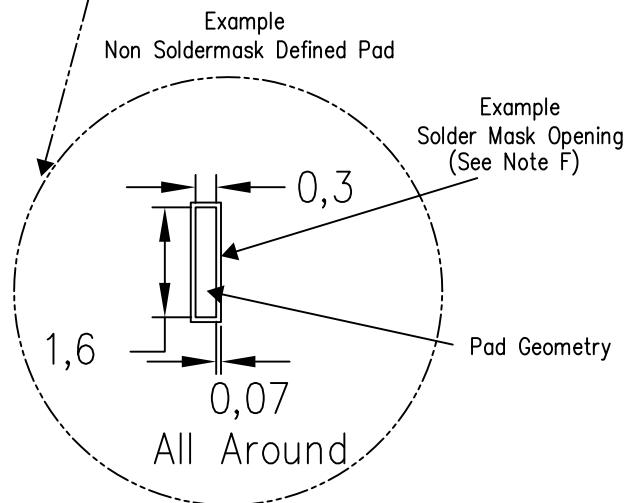
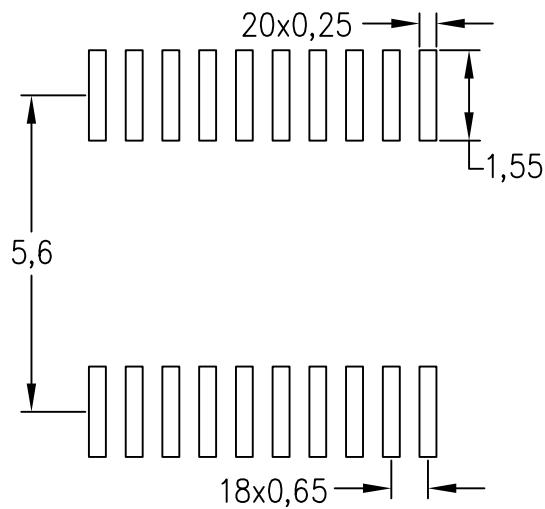
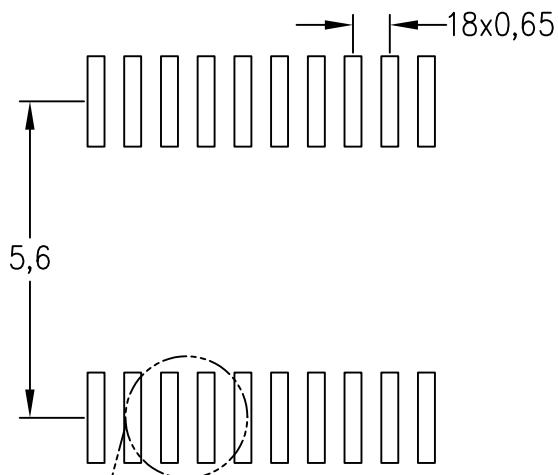
E. TADS within SLELC MU-155

## PW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE

## Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).



4211284-5/F 12/12

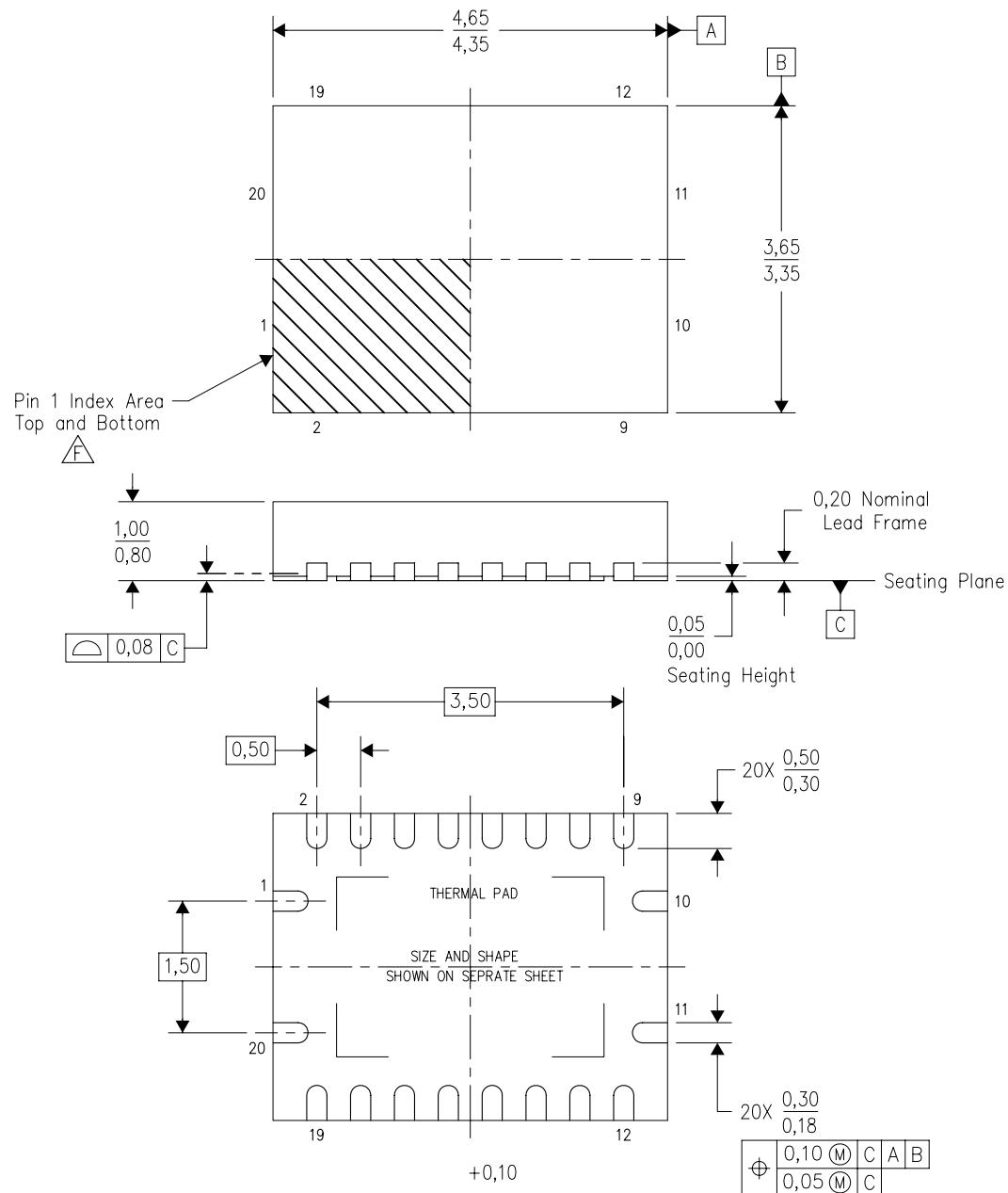
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-4/l 06/2011

NOTES:

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- QFN (Quad Flatpack No-Lead) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.
- See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

# THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N20)

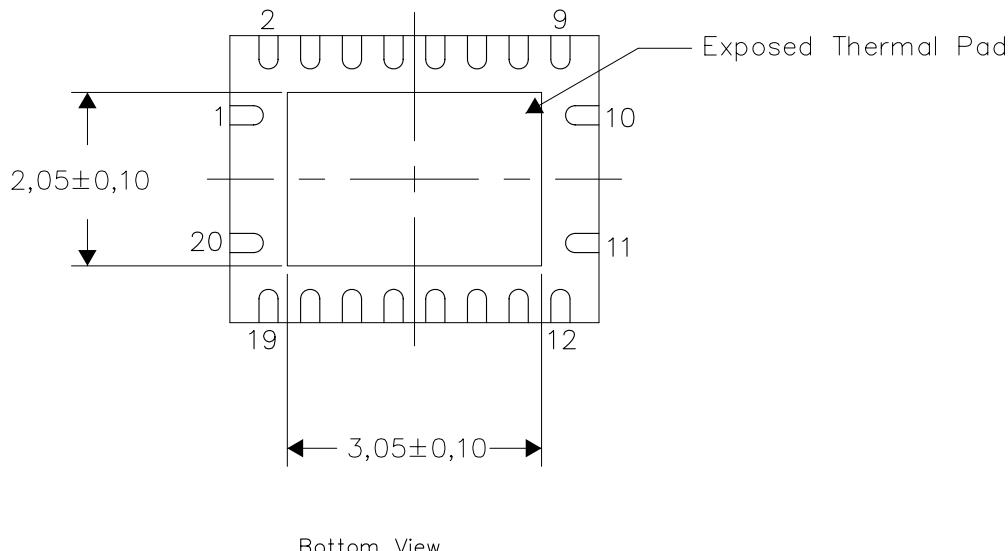
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



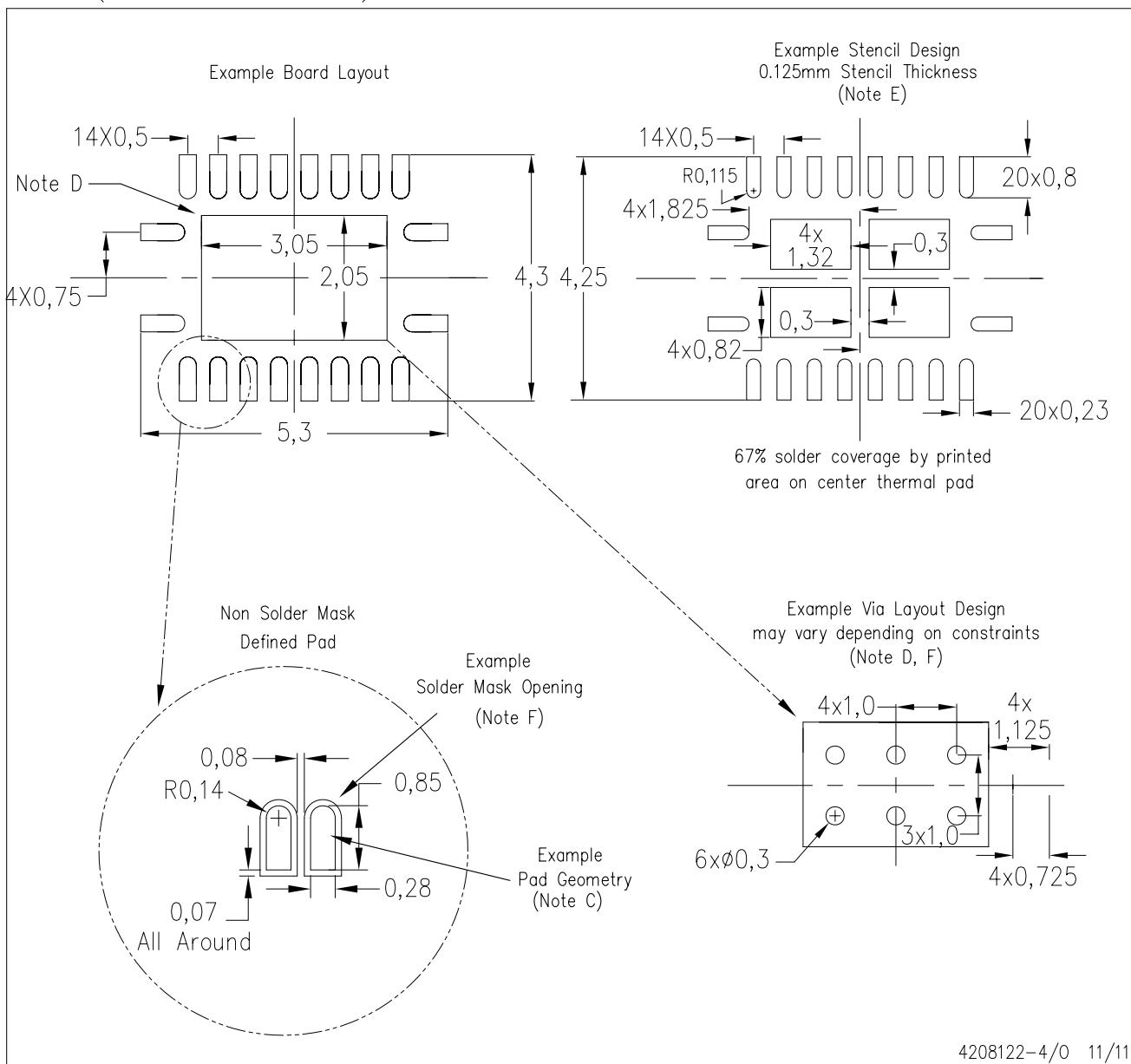
Exposed Thermal Pad Dimensions

4206353-4/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**



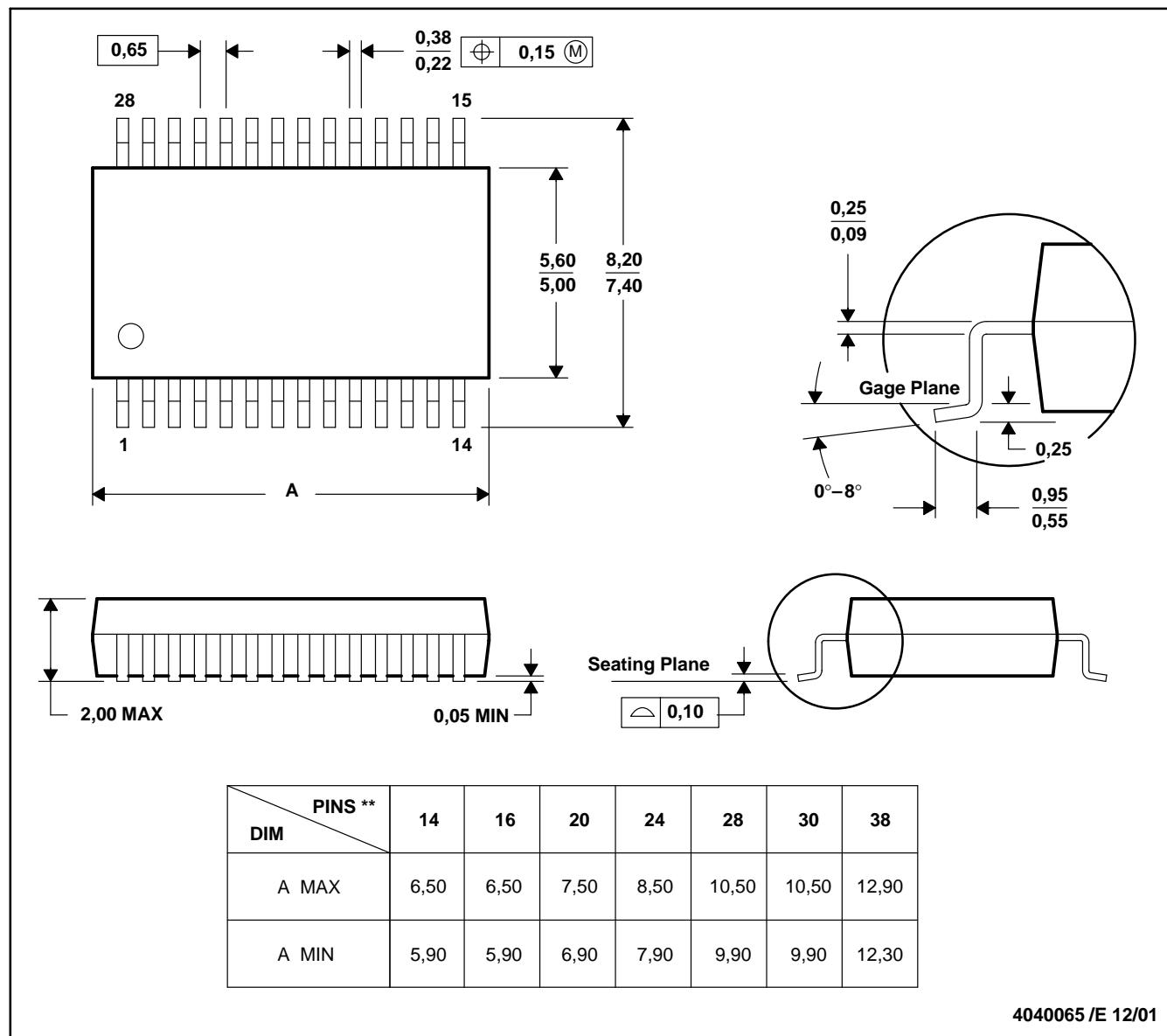
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products	Applications
Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
	<b>TI E2E Community</b>
	<a href="http://e2e.ti.com">e2e.ti.com</a>