

2N7002K

TrenchMOS™ logic level FET

Rev. 01 — 20 October 2003

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level compatible
- Subminiature surface mount package
- Very fast switching
- Gate-source ESD protection diodes.

1.3 Applications

- Relay driver
- High speed line driver.

1.4 Quick reference data

- $V_{DS} \leq 60 \text{ V}$
- $P_{tot} \leq 0.83 \text{ W}$
- $I_D \leq 340 \text{ mA}$
- $R_{DS(on)} \leq 3.9 \Omega$.

2. Pinning information

Table 1: Pinning - SOT23, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	source (s)		
3	drain (d)		

3. Ordering information

Table 2: Ordering information

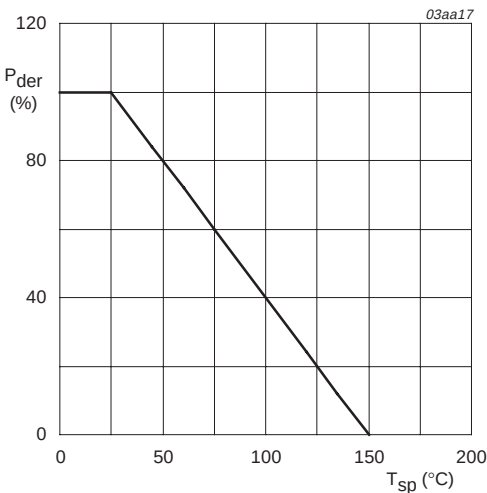
Type number	Package		
	Name	Description	Version
2N7002K	SOT23	Plastic surface mounted package; 3 leads.	SOT23

4. Limiting values

Table 3: Limiting values

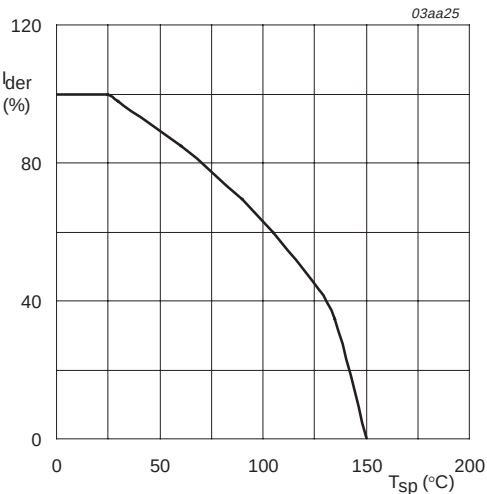
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage (DC)		-	± 15	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	340	mA
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	215	mA
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	680	mA
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	0.83	W
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	340	mA
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	680	mA
Electrostatic discharge voltage					
V_{esd}	electrostatic discharge voltage	Human Body Model 1; $C = 100\text{ pF}$; $R = 1.5\text{ k}\Omega$	-	1	kV



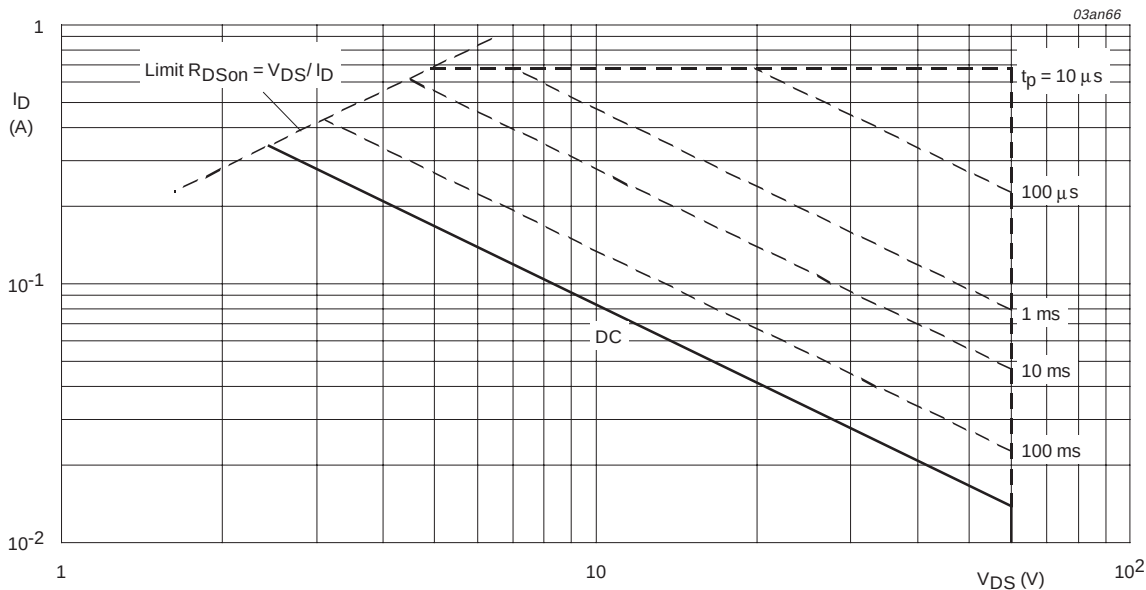
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25$ °C; I_{DM} is single pulse; $V_{GS} = 10$ V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	150	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	350	-	K/W

5.1 Transient thermal impedance

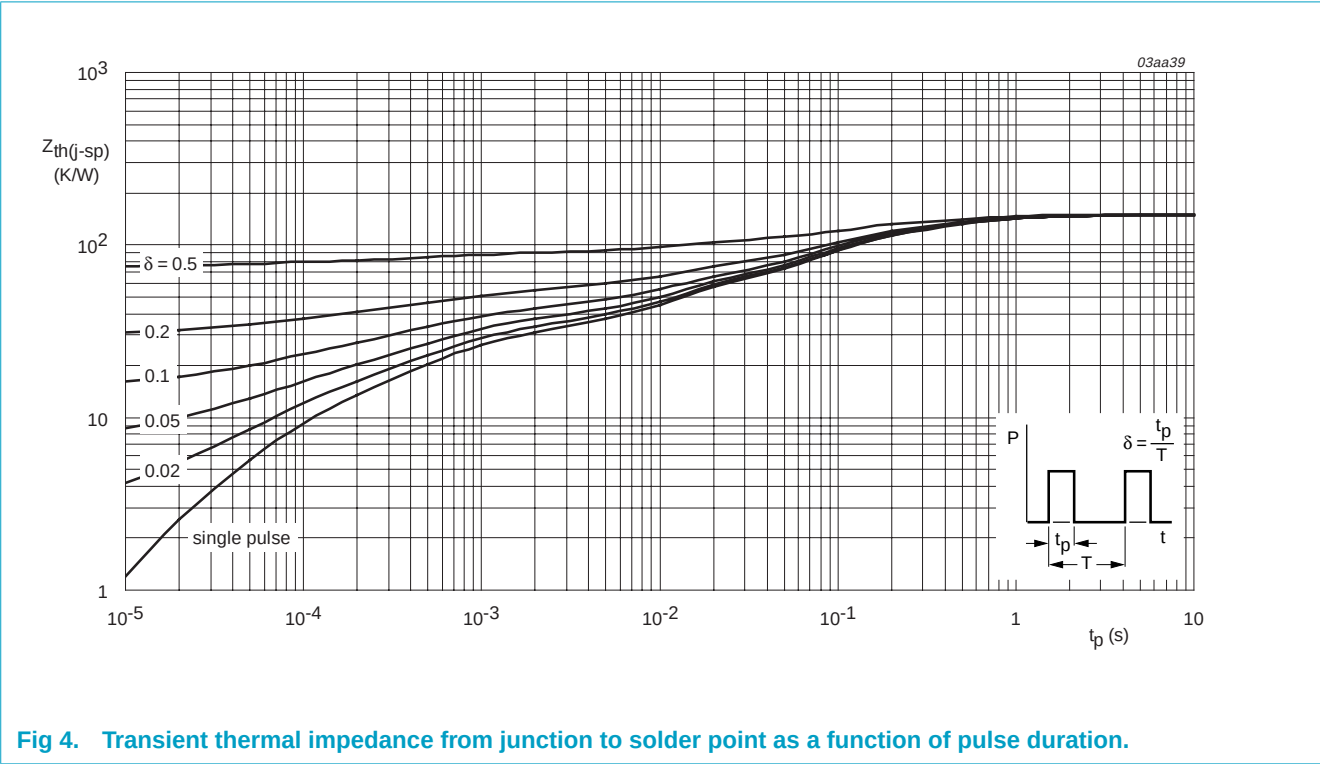


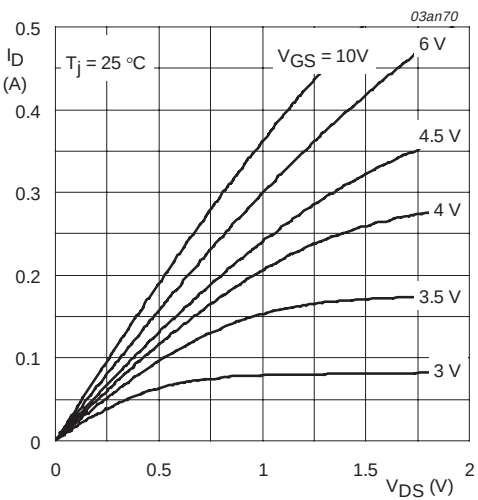
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

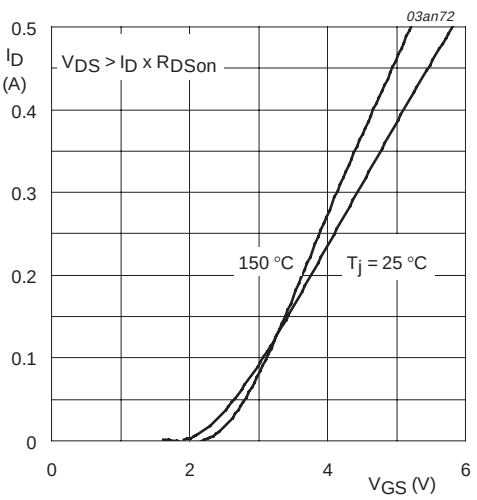
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 10 μA; V _{GS} = 0 V				
		T _J = 25 °C	60	75	-	V
		T _J = −55 °C	55	-	-	V
V _{(BR)GSS}	drain-source breakdown voltage	I _G = ±1 mA; V _{DS} = 0 V	16	22	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9				V
		T _J = 25 °C	1	2	-	V
		T _J = 150 °C	0.6	-	-	V
		T _J = −55 °C	-	-	3.5	V
I _{DSS}	drain-source leakage current	V _{DS} = 48 V; V _{GS} = 0 V				
		T _J = 25 °C	-	0.01	1	μA
		T _J = 150 °C	-	-	10	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	-	50	500	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 500 mA; Figure 7 and 8				
		T _J = 25 °C	-	2.8	3.9	Ω
		T _J = 150 °C	-	5.2	7.2	Ω
		V _{GS} = 4.5 V; I _D = 200 mA; Figure 7 and 8	-	3.8	5.3	Ω
Dynamic characteristics						
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 10 V; f = 1 MHz;	-	13	40	pF
C _{oss}	output capacitance	Figure 11	-	8	30	pF
C _{rss}	reverse transfer capacitance		-	4	10	pF
t _{on}	turn-on time	V _{DD} = 50 V; R _L = 250 Ω;	-	3	10	ns
t _{off}	turn-off time	V _{GS} = 10 V; R _G = 50 Ω; R _{GS} = 50 Ω	-	9	15	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 300 mA; V _{GS} = 0 V; Figure 12	-	0.93	1.5	V
t _{rr}	reverse recovery time	I _S = 300 mA; dI _S /dt = −100 A/μs;	-	30	-	ns
Q _r	recovered charge	V _{GS} = 0 V; V _R = 25 V	-	30	-	nC



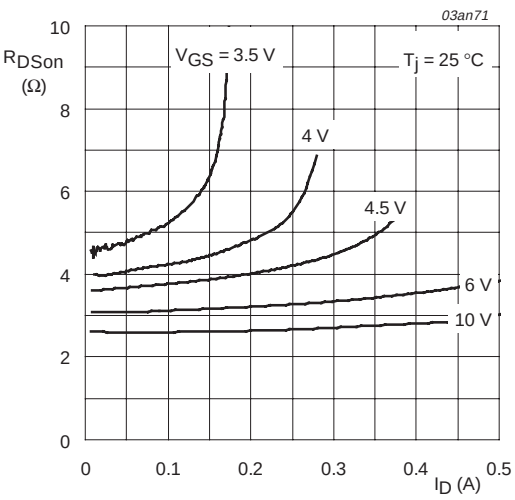
$T_J = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



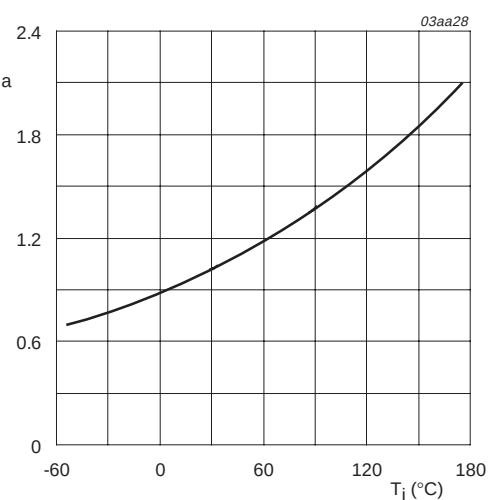
$T_J = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



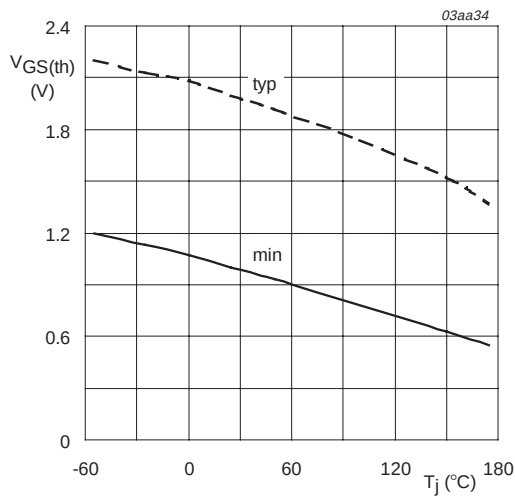
$T_J = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



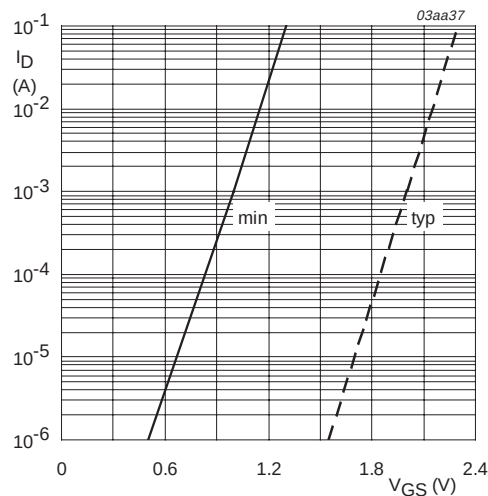
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



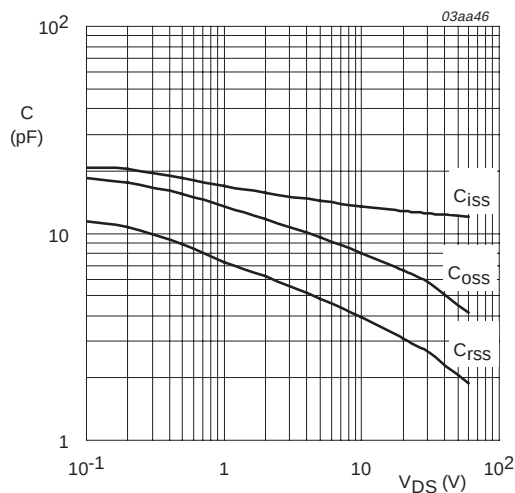
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



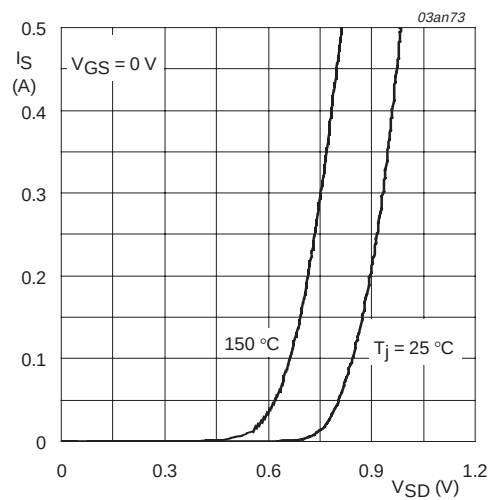
$T_J = 25\text{ °C}; V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



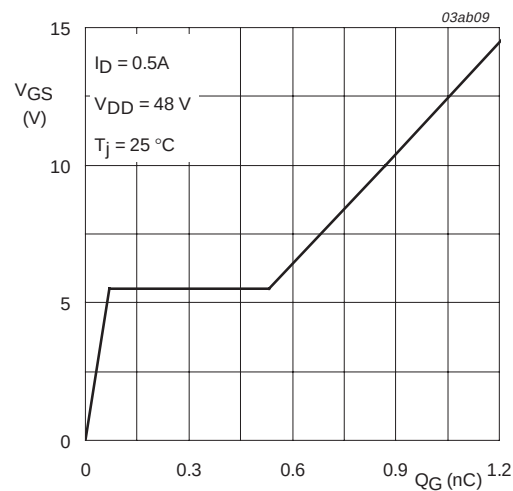
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^{\circ}\text{C}$ and $150\text{ }^{\circ}\text{C}$; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 0.5\text{ A}$; $V_{DD} = 48\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic surface mounted package; 3 leads

SOT23

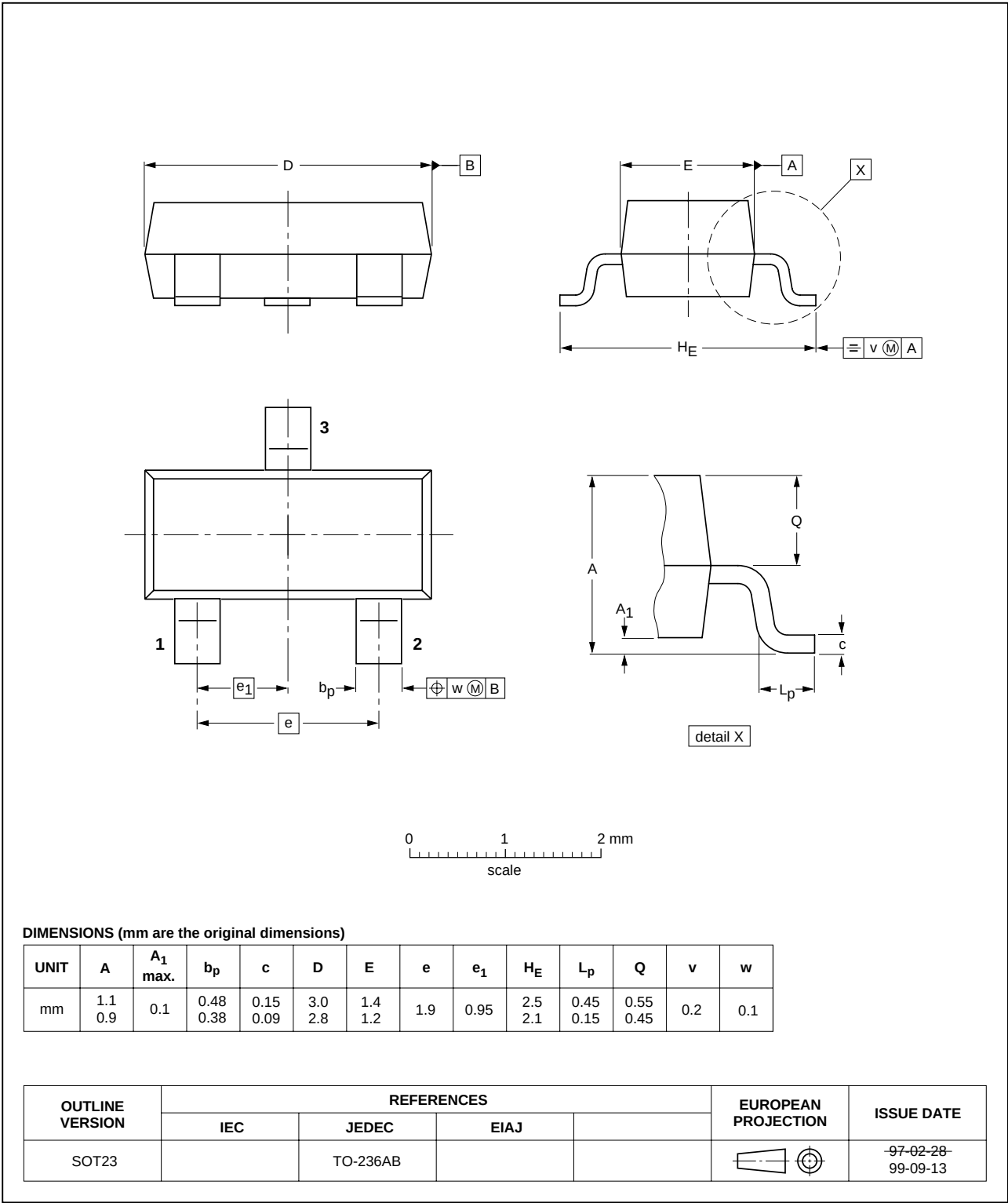


Fig 14. SOT23.

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20031020		Product data (9397 750 11703)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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