LM48511 3-W, Ultra-Low EMI, Filterless, Mono, Class D Audio Power Amplifier With Spread Spectrum

1 Features

- 3-W Output into 8 Ω at 5 V With THD+N = 1%
- Selectable spread spectrum mode reduces EMI
- 80% Efficiency
- Independent regulator and amplifier shutdown controls
- Dynamically Selectable Regulator Output Voltages
- Filterless Class D
- 3-V to 5.5-V Operation
- Low shutdown current
- Click and pop suppression
- Key specifications
  - Quiescent power supply current
    - V_{DD} = 3 V 9 mA (Typical)
    - V_{DD} = 5 V 13.5 mA (Typical)
  - P_O at V_{DD} = 5 V, PV1 = 7.8 V, R_L = 8 Ω, THD+N = 1% 3 W (Typical)
  - P_O at V_{DD} = 3 V, PV1 = 4.8 V, R_L = 8 Ω, THD+N = 1% 1 W (Typical)
  - P_O at V_{DD} = 5 V, PV1 = 7.8 V, R_L = 4 Ω, THD+N = 1% 5.4 W (Typical)
  - Shutdown Current at V_{DD} = 3 V, 0.01 µA (Typical)

2 Applications

- GPS
- Portable media
- Cameras
- Mobile phones
- Handheld games

3 Description

The LM48511 device integrates a boost converter with a high-efficiency Class D audio power amplifier to provide 3-W continuous power into an 8-Ω speaker when operating from a 5-V power supply.

When operating from a 3-V to 4-V power supply, the LM48511 can be configured to drive 1 to 2.5 W into an 8-Ω load with less than 1% distortion (THD+N). The Class D amplifier features a low-noise PWM architecture that eliminates the output filter, reducing external component count, board area consumption, system cost, and simplifying design. A selectable spread spectrum modulation scheme suppresses RF emissions, further reducing the need for output filters.

The switching regulator of the LM48511 is a current-mode boost converter operating at a fixed frequency of 1 MHz. Two selectable feedback networks allow the LM48511 regulator to dynamically switch between two different output voltages, improving efficiency by optimizing the amplifier's supply voltage based on battery voltage and output power requirements.

The LM48511 is designed for use in portable devices, such as GPS, mobile phones, and MP3 players. The high, 80% efficiency at 5 V, extends battery life when compared to Boosted Class AB amplifiers. Independent regulator and amplifier shutdown controls optimize power savings by disabling the regulator when high-output power is not required.

The gain of the LM48511 is set by external resistors, which allows independent gain control from multiple sources by summing the signals. Output short circuit and thermal overload protection prevent the device from damage during fault conditions. Superior click and pop suppression eliminates audible transients during power-up and shutdown.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM48511	WQFN (24)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

EMI Graph: LM48511 RF Emissions — 3-Inch Cable

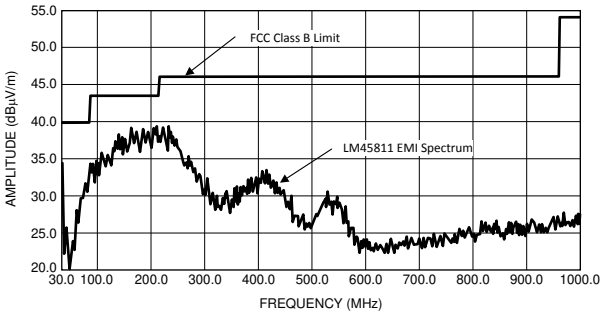


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (October 2017) to Revision K — **Page**

- Changed pin labels in Figure 24 ... 16

Changes from Revision I (August 2017) to Revision J — **Page**

- Changed Pin 20 From: FB_GND0 To: FB_GND1 in the Pin Image and *Pin Functions* table ... 4
- Changed Pin 21 From: FB_GND1 To: FB_GND0 in the Pin Image and *Pin Functions* table ... 4

Changes from Revision H (August 2015) to Revision I — **Page**

- Changed Pin 20 From: FB_GND1 To: FB_GND0 in the Pin Image and *Pin Functions* table ... 4
- Changed Pin 21 From: FB_GND0 To: FB_GND1 in the Pin Image and *Pin Functions* table ... 4

Changes from Revision G (May 2013) to Revision H — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision F (October 2012) to Revision G — **Page**

- Changed layout of National Data Sheet to TI format ... 20

Changes from Revision D (February 2012) to Revision E — **Page**

- Deleted the Typical limits (Vih and Vil) EC table ... 6

Changes from Revision C (November 2007) to Revision D **Page**

- Deleted the “Build of Materials” (BOM) table 20

Changes from Revision B (September 2007) to Revision C **Page**

- Edited the Notes section and added another P_O (@V_{DD} = 5 V, R_L = 4 Ω) section in the Key Specification division. 1

Changes from Revision A (July 2007) to Revision B **Page**

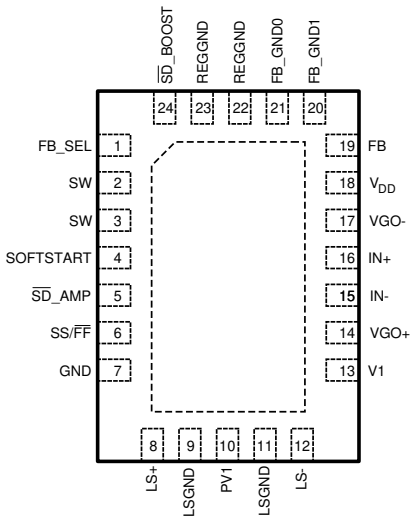
- Changed the Amplifier Voltage (Operating Ratings section) from 5 V to 4.8 V. 5

Changes from Original (July 2007) to Revision A **Page**

- Input some text edits 1

5 Pin Configuration and Functions

NHZ Package
24-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DAP	–	—	To be soldered to board for enhanced thermal dissipation. Connect to GND plane.
FB	19	—	Regulator feedback input Connect FB to an external resistive voltage divider to set the boost output voltage.
FB_GND0	21	—	Ground return for R_3, R_1 resistor divider
FB_GND1	20	—	Ground return for R_3, R_2 resistor divider
FB_SEL	1	I	Regulator feedback select Connect to VDD to select feedback network connected to FB_GND1. Connect to GND to select feedback network connected to FB_GND0.
GND	7	—	Signal ground
IN–	15	I	Amplifier inverting input
IN+	16	I	Amplifier noninverting input
LS+	8	O	Amplifier noninverting output
LS–	12	O	Amplifier inverting output
LSGND	9, 11	—	Amplifier H-Bridge ground
PV1	10	—	Amplifier H-Bridge power supply Connect to V1.
REGGND	22, 23	—	Power ground (booster)
$\overline{SD}$_AMP	5	I	Amplifier active-low shutdown Connect to V_{DD} for normal operation. Connect to GND to disable amplifier.
$\overline{SD}$_BOOST	24	I	Regulator active-low shutdown. Connect to V_{DD} for normal operation. Connect to GND to disable regulator.
SOFT-START	4	—	Soft-start capacitor
SS/$\overline{FF}$	6	I	Modulation mode select. Connect to V_{DD} for spread spectrum mode (SS). Connect to GND for fixed frequency mode (FF).
SW	2, 3	—	Drain of the internal FET switch
V1	13	—	Amplifier supply voltage Connect to PV1
VDD	18	—	Power supply
VG0+	14	O	Amplifier noninverting gain output
VG0–	17	O	Amplifier inverting gain output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2).

	MIN	MAX	UNIT
Supply voltage (V_{DD}, PV1, V_1)		9	V
Input voltage	−0.3	V_{DD} + 0.3	V
Power dissipation(3)	Internally limited		
Junction temperature	150		°C
Storage temperature	−65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The*Recommended Operating Conditions* indicate conditions at which the device is functional and the device must not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θJ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower. For the LM48511, see Figure 20 for additional information.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Machine model(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Machine model, applicable std. JESD22-A115-A.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Temperature range $T_{MIN} \le T_A \le T_{MAX}$	−40	85	°C
Supply voltage (V_{DD})	3	5.5	V
Amplifier voltage (PV_1, V_1)	4.8	8	V

6.4 Thermal Information

THERMAL METRIC(1)		LM48511 NHZ (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics V_{DD} = 5 V

The following specifications apply for V_{DD} = 5 V, PV_1 = 7.8 V (continuos mode), A_V = 2 V/V, R_3 = 25.5 kΩ, R_{LS} = 4.87 kΩ, R_L = 8 Ω, f = 1 kHz, SS/$\overline{FF}$ = GND, unless otherwise specified. Limits apply for T_A = 25°C.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, R_{LOAD} = ∞	Fixed Frequency Mode (FF)		13.5		mA
			Spread Spectrum Mode (SS)		14.5	22	mA
I_{SD}	Shutdown Current(3)	$V_{\overline{SD\_BOOST}}$ = $V_{\overline{SD\_AMP}}$ = SS = FB_SEL = GND			0.11	1	µA
V_{IH}	Logic Voltage Input High			1.4			V
V_{IL}	Logic Voltage Input Low					0.4	V
T_{WU}	Wake-up Time	C_{SS} = 0.1 µF			49		ms
V_{OS}	Output Offset Voltage	See (4)			0.04	3	mV
P_O	Output Power	R_L = 8 Ω, f = 1 kHz, BW = 22 kHz, THD+N = 1%	FF		3		W
			SS	2.6	3		
		R_L = 8 Ω, f = 1 kHz, BW = 22 kHz, THD+N = 10%	FF		3.8		W
			SS		3.8		
		R_L = 4 Ω, f = 1 kHz, BW = 22 kHz, THD+N = 1%	FF		5.4		W
			SS		5.4		
		R_L = 4 Ω, f = 1 kHz, BW = 22 kHz, THD+N = 10%	FF		6.7		W
			SS		6.7		
THD+N	Total Harmonic Distortion + Noise	P_O = 2 W, f = 1 kHz, R_L = 8 Ω	FF		0.03%		
			SS		0.03%		
		P_O = 3 W, f = 1 kHz, R_L = 4 Ω	FF		0.04%		
			SS		0.05%		
ε_{OS}	Output Noise	f = 20 Hz to 20 kHz, Inputs to AC GND, No weighting	FF		32		μV_{RMS}
			SS		32		
		f = 20 Hz to 20 kHz, Inputs to AC GND, A weighted	FF		22		μV_{RMS}
			SS		22		
PSRR	Power Supply Rejection Ratio (Input Referred)	V_{RIPPLE} = 200 mV_{P-P} Sine, f_{RIPPLE} = 217 Hz	FF		88		dB
			SS		87		
		V_{RIPPLE} = 200 mV_{P-P} Sine, f_{RIPPLE} = 1 kHz	FF		88		dB
			SS		85		
		V_{RIPPLE} = 200 mV_{P-P} Sine, f_{RIPPLE} = 10 kHz	FF		77		dB
			SS		76		
CMRR	Common-Mode Rejection Ratio (Input Referred)	V_{RIPPLE} = 1 V_{P-P}, f_{RIPPLE} = 217 Hz			73		dB
η	Efficiency	f = 1 kHz, R_L = 8 Ω, P_O = 1 W			80%		
V_{FB}	Feedback Pin Reference Voltage(5)				1.23		V

(1) R_L is a resistive load in series with two inductors to simulate an actual speaker load for R_L = 8Ω, the load is 15µH+8Ω+15µH. For R_L = 4 Ω, the load is 15 µH + 4 Ω + 15 µH.
(2) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.
(3) Shutdown current is measured with components R1 and R2 removed.
(4) Offset voltage is determined by: ($I_{DD\ (with\ load)}$ — $I_{DD\ (no\ load)}$) x R_L.
(5) Feedback pin reference voltage is measured with the Audio Amplifier disconnected from the Boost converter (the Boost converter is unloaded).

6.6 Electrical Characteristics V_{DD} = 3.6 V

The following specifications apply for V_{DD} = 3.6 V, PV1 = 7 V (continuous mode), A_V = 2 V/V, R_3 = 25.5 kΩ, R_{LS} = 5.36 kΩ, R_L = 8 Ω, f = 1 kHz, SS/$\overline{FF}$ = GND, unless otherwise specified. Limits apply for T_A = 25°C.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, R_{LOAD} = ∞	Fixed Frequency Mode (FF)		16		mA
			Spread Spectrum Mode (SS)		17.5	26.6	mA
I_{SD}	Shutdown Current(3)	$V_{\overline{SD\_BOOST}}$ = $V_{\overline{SD\_AMP}}$ = SS = FB_SEL = GND			0.03	1	µA
V_{IH}	Logic Voltage Input High			1.4	0.96		V
V_{IL}	Logic Voltage Input Low			0.4	0.84		V
T_{WU}	Wake-up Time	C_{SS} = 0.1 µF			50		ms
V_{OS}	Output Offset Voltage	See (4)			0.04		mV
P_O	Output Power	R_L = 8 Ω, f = 1 kHz, BW = 22 kHz THD+N = 1%	FF		2.5		W
			SS		2.5		
		R_L = 8 Ω, f = 1 kHz, BW = 22 kHz THD+N = 10%	FF		3		W
			SS		3		
		R_L = 4 Ω, f = 1 kHz, BW = 22 kHz THD+N = 1%	FF		4.3		W
			SS		4.2		
		R_L = 4 Ω, f = 1 kHz, BW = 22 kHz THD+N = 10%	FF		5.4		W
			SS		5.3		
THD+N	Total Harmonic Distortion + Noise	P_O = 1.5 W, f = 1 kHz, R_L = 8 Ω	FF		0.03%		
			SS		0.03%		
		P_O = 3 W, f = 1 kHz, R_L = 4 Ω	FF		0.04%		
			SS		0.05%		
ε_{OS}	Output Noise	f = 20 Hz to 20 kHz Inputs to AC GND, No weighting	FF		35		μV_{RMS}
			SS		36		
		f = 20 Hz to 20 kHz Inputs to AC GND, A weighted	FF		25		μV_{RMS}
			SS		26		
PSRR	Power Supply Rejection Ratio (Input Referred)	V_{RIPPLE} = 200 mV_{P-P} Sine, f_{RIPPLE} = 217 Hz	FF		85		dB
			SS		86		
		V_{RIPPLE} = 200 mV_{P-P} Sine, f_{RIPPLE} = 1 kHz	FF		87		dB
			SS		86		
		V_{RIPPLE} = 200 mV_{P-P} Sine, f_{RIPPLE} = 10 kHz	FF		78		dB
			SS		77		
CMRR	Common-Mode Rejection Ratio (Input Referred)	V_{RIPPLE} = 1 V_{P-P}, f_{RIPPLE} = 217 Hz			73		dB
η	Efficiency	f = 1 kHz, R_L = 8 Ω, P_O = 1 W			77%		
V_{FB}	Feedback Pin Reference Voltage(5)				1.23		V

(1) R_L is a resistive load in series with two inductors to simulate an actual speaker load for R_L = 8Ω, the load is 15µH+8Ω+15µH. For R_L = 4 Ω, the load is 15 µH + 4 Ω + 15 µH.
(2) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.
(3) Shutdown current is measured with components R1 and R2 removed.
(4) Offset voltage is determined by: ($I_{DD\ (with\ load)}$ — $I_{DD\ (no\ load)}$) x R_L.
(5) Feedback pin reference voltage is measured with the Audio Amplifier disconnected from the Boost converter (the Boost converter is unloaded).

6.7 Electrical Characteristics V_{DD} = 3 V

The following specifications apply for V_{DD} = 3 V, PV1 = 4.8 V (continuos mode), A_V = 2V/V, R_3 = 25.5 kΩ, R_{LS} = 9.31 kΩ, R_L = 8 Ω, f = 1 kHz, SS/$\overline{FF}$ = GND, unless otherwise specified. Limits apply for T_A = 25°C.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, R_{LOAD} = ∞	Fixed Frequency Mode (FF)		9		mA
			Spread Spectrum Mode (SS)		9.5		mA
I_{SD}	Shutdown Current(3)	$V_{\overline{SD}\_BOOST}$ = $V_{\overline{SD}\_AMP}$ = SS = FB_SEL = GND			0.01	1	µA
V_{IH}	Logic Voltage Input High				0.91		V
V_{IL}	Logic Voltage Input Low				0.79		V
T_{WU}	Wake-up Time	C_{SS} = 0.1µF			49		ms
V_{OS}	Output Offset Voltage(4)				0.04		mV
P_O	Output Power	R_L = 8 Ω, f = 1 kHz, BW = 22 kHz THD+N = 1%	FF		1		W
			SS	0.84	1		
		R_L = 8 Ω, f = 1 kHz, BW = 22 kHz THD+N = 10%	FF		1.3		W
			SS		1.3		
		R_L = 4 Ω, f = 1 kHz, BW = 22 kHz THD+N = 1%	FF		1.8		W
			SS		1.8		
		R_L = 4 Ω, f = 1 kHz, BW = 22 kHz THD+N = 10%	FF		2.2		W
			SS		2.2		
THD+N	Total Harmonic Distortion + Noise	P_O = 500 mW, f = 1 kHz, R_L = 8 Ω	FF		0.02%		
			SS		0.03%		
		P_O = 500 mW, f = 1 kHz, R_L = 4 Ω	FF		0.04%		
			SS		0.06%		
ε_{OS}	Output Noise	f = 20Hz to 20kHz Inputs to AC GND, No weighting	FF		35		μV_{RMS}
			SS		35		
		f = 20 Hz to 20 kHz Inputs to AC GND, A weighted	FF		25		μV_{RMS}
			SS		25		
PSRR	Power Supply Rejection Ratio (Input Referred)	V_{RIPPLE} = 200 mV_{P-P} Sine, f_{RIPPLE} = 217 Hz	FF		89		dB
			SS		89		
		V_{RIPPLE} = 200 mV_{P-P} Sine, f_{RIPPLE} = 1 kHz	FF		88		dB
			SS		88		
		V_{RIPPLE} = 200 mV_{P-P} Sine, f_{RIPPLE} = 10 kHz	FF		78		dB
			SS		78		
CMRR	Common-Mode Rejection Ratio (Input Referred)	V_{RIPPLE} = 1 V_{P-P}, f_{RIPPLE} = 217 Hz			71		dB
η	Efficiency	f = 1 kHz, R_L = 8 Ω, P_O = 1 W			75%		
V_{FB}	Feedback Pin Reference Voltage(5)				1.23		V

(1) R_L is a resistive load in series with two inductors to simulate an actual speaker load for R_L = 8Ω, the load is 15µH+8Ω+15µH. For R_L = 4 Ω, the load is 15 µH + 4 Ω + 15 µH.
(2) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not specified.
(3) Shutdown current is measured with components R1 and R2 removed.
(4) Offset voltage is determined by: ($I_{DD\ (with\ load)}$ — $I_{DD\ (no\ load)}$) x R_L.
(5) Feedback pin reference voltage is measured with the Audio Amplifier disconnected from the Boost converter (the Boost converter is unloaded).

6.8 Typical Characteristics

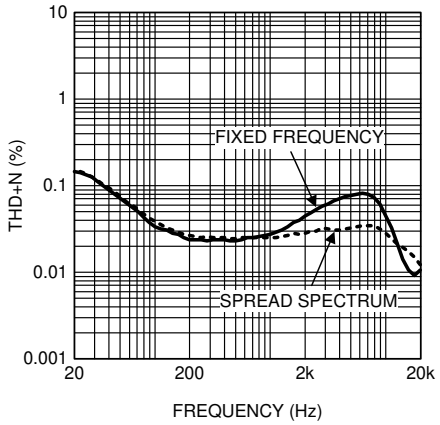


Figure 1. THD+N vs Frequency
V_{DD} = 5 V, R_L = 8 Ω
P_O = 2 W, Filter = 22 kHz, PV_1 = 7.8 V

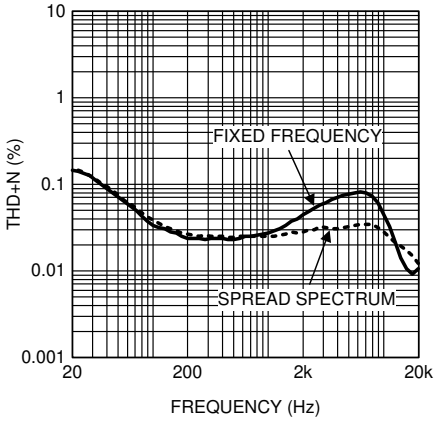


Figure 2. THD+N vs Frequency
V_{DD} = 3.6 V, R_L = 8 Ω
P_O = 500 mW, Filter = 22 kHz, PV_1 = 4.8 V

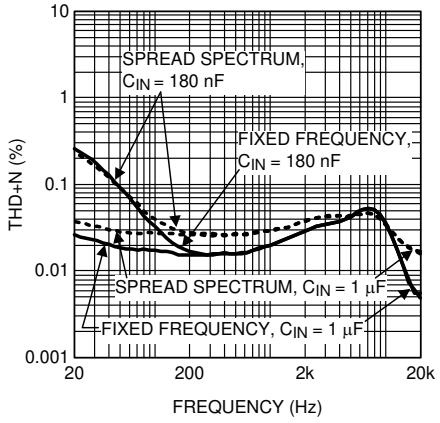


Figure 3. THD+N vs Frequency
V_{DD} = 3 V, R_L = 8 Ω
P_O = 1.5 W, Filter = 22 kHz, PV_1 = 7 V

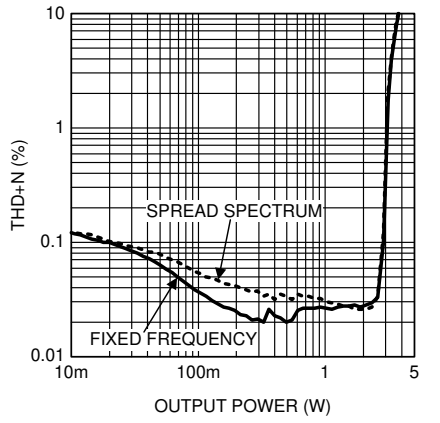


Figure 4. THD+N vs Output Power
V_{DD} = 5 V, R_L = 8 Ω
P_O = 1.5 W, f = 1 kHz, Filter = 22 kHz, PV_1 = 7.8 V

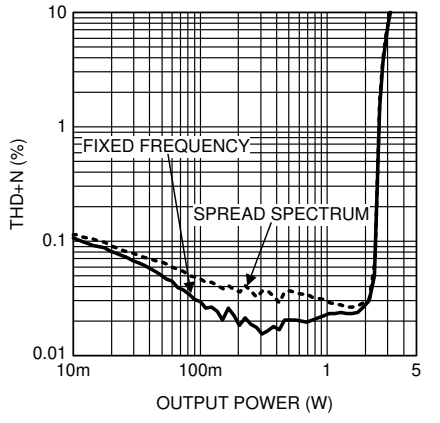


Figure 5. THD+N vs Output Power
V_{DD} = 3.6 V, R_L = 8 Ω
f = 1 kHz, Filter = 22 kHz, PV_1 = 7 V

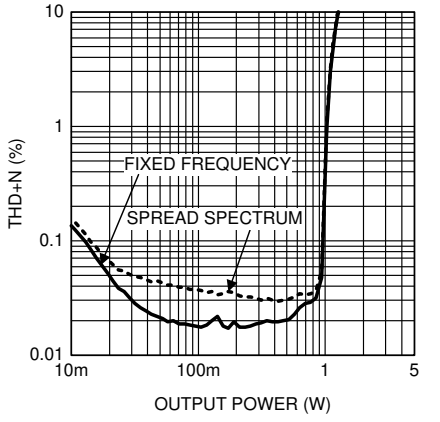


Figure 6. THD+N vs Output Power
V_{DD} = 3 V, R_L = 8 Ω
f = 1 kHz, Filter = 22 kHz, PV_1 = 4.8 V

Typical Characteristics (continued)

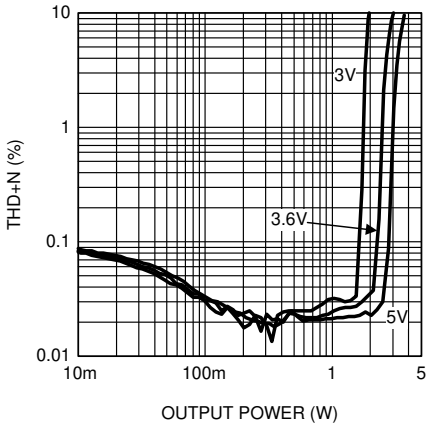


Figure 7. THD+N vs Output Power
V_{DD} = 3 V, 3.6 V, 5 V, R_L = 8 Ω
f = 1kHz, Filter = 22 kHz, R_1 = 4.87 kΩ, FF

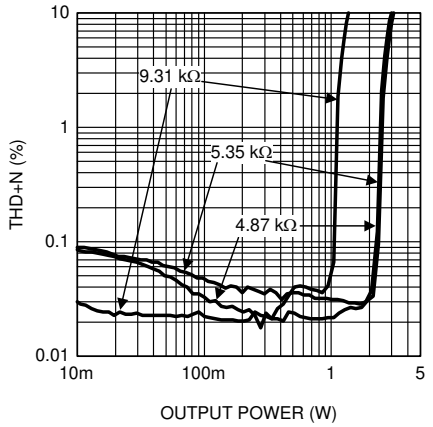


Figure 8. THD+N vs Output Power
V_{DD} = 3.6 V, R_L = 8 Ω
Filter = 22 kHz, PV_1 = 7.8 V, PV_1 = 7 V, PV_1 = 4.8 V, FF

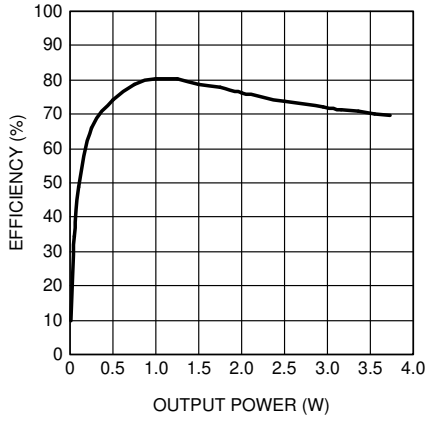


Figure 9. Boost Amplifier vs Output Power
V_{DD} = 5 V, R_L = 8 Ω
f = 1 kHz, PV_1 = 7.8 V

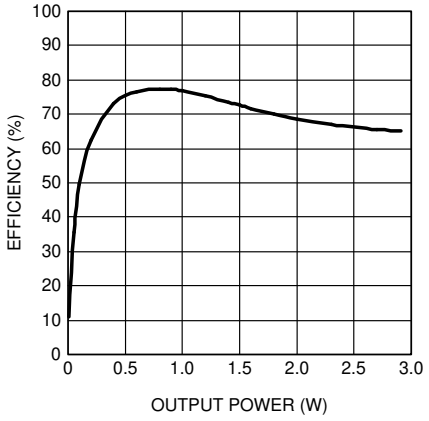


Figure 10. Boost Amplifier vs Output Power
V_{DD} = 3.6 V, R_L = 8 Ω
f = 1 kHz, PV_1 = 7 V

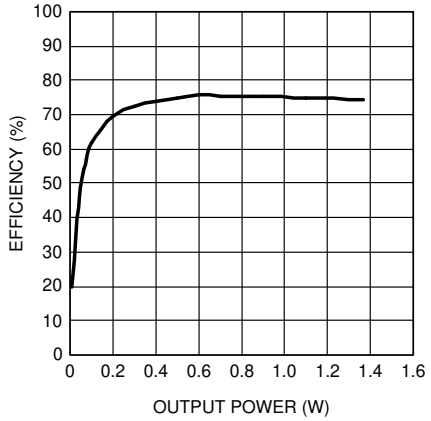


Figure 11. Boost Amplifier vs Output Power
V_{DD} = 3 V, R_L = 8 Ω
f = 1 kHz, PV_1 = 4.8 V

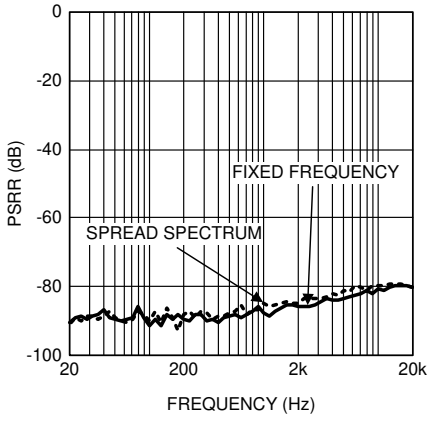


Figure 12. PSRR vs Frequency
V_{DD} = 5 V, R_L = 8 Ω
V_{RIPPLE} = 200 mV_{PP}, PV_1 = 7.8 V

Typical Characteristics (continued)

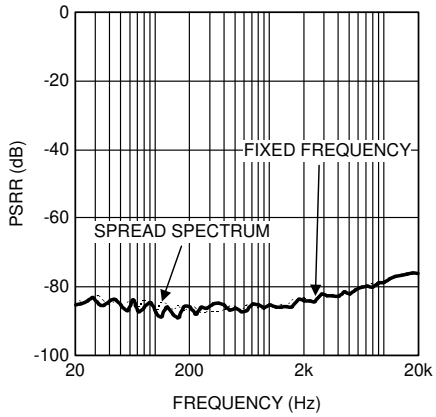


Figure 13. PSRR vs Frequency
V_{DD} = 3.6 V, R_L = 8 Ω
V_{RIPPLE} = 200 mV_{PP}, PV_1 = 7 V

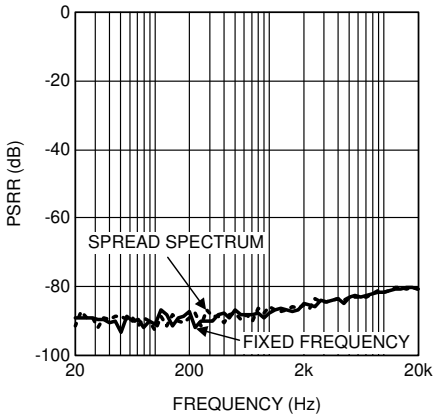


Figure 14. PSRR vs Frequency
V_{DD} = 3 V, R_L = 8 Ω
V_{RIPPLE} = 200 mV_{PP}, PV_1 = 4.8 V

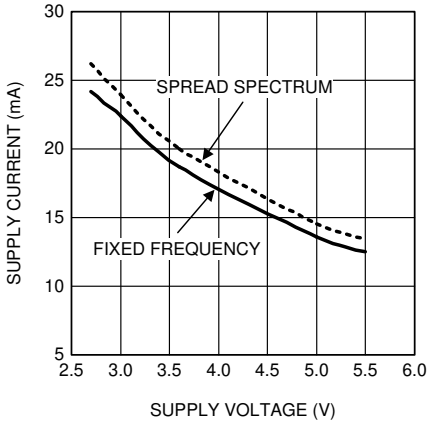


Figure 15. Supply Current vs Supply Voltage
PV_1 = 7.8 V

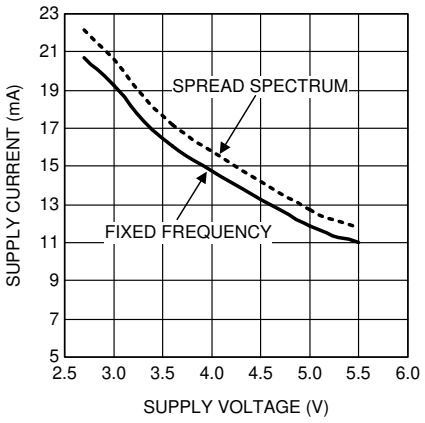


Figure 16. Supply Current vs Supply Voltage
PV_1 = 7 V

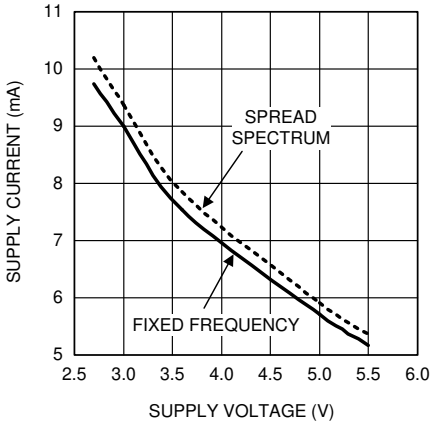


Figure 17. Supply Current vs Supply Voltage
PV_1 = 4.8 V

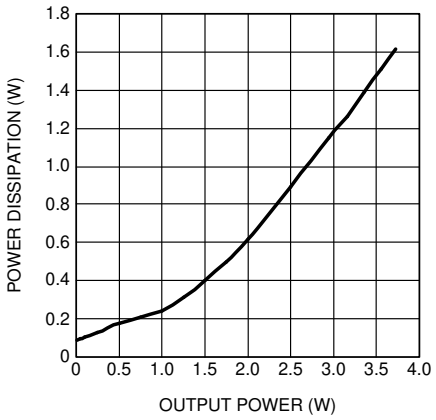


Figure 18. Power Dissipation vs Output Power
V_{DD} = 5 V, R_L = 8 Ω
PV_1 = 7.8 V, FF

Typical Characteristics (continued)

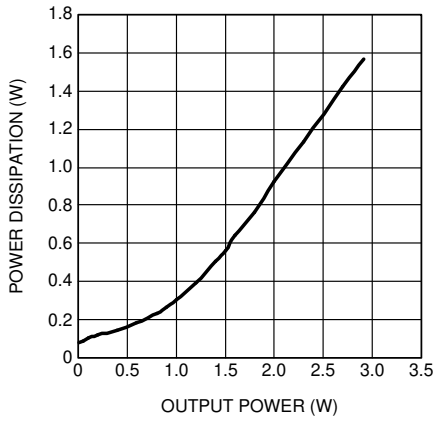


Figure 19. Power Dissipation vs Output Power
V_{DD} = 3.6 V, R_L = 8 Ω
PV_1 = 7 V, FF

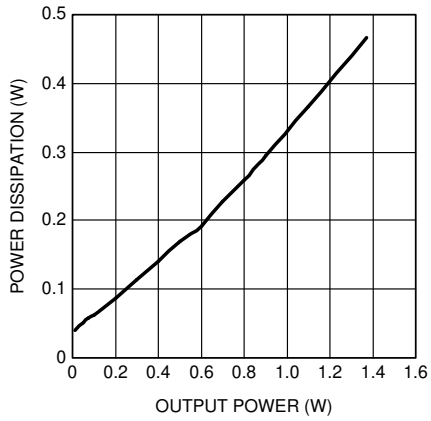


Figure 20. Power Dissipation vs Output Power
V_{DD} = 3 V, R_L = 8 Ω
PV_1 = 4.8 V, FF

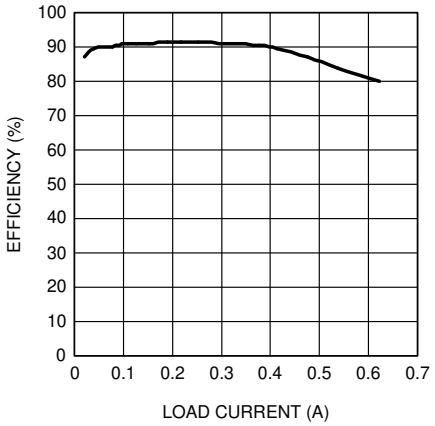


Figure 21. Boost Converter Efficiency vs $I_{LOAD(DC)}$
V_{DD} = 5 V, PV_1 = 7.8 V

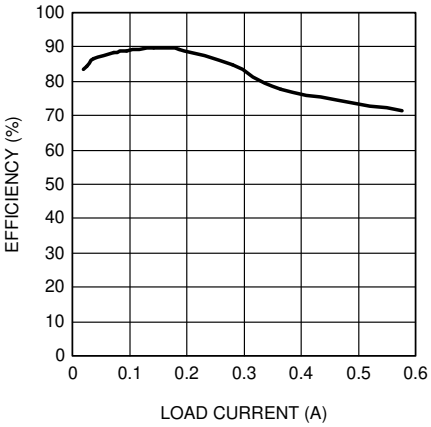


Figure 22. Boost Converter Efficiency vs $I_{LOAD(DC)}$
V_{DD} = 3.6 V, PV_1 = 7 V

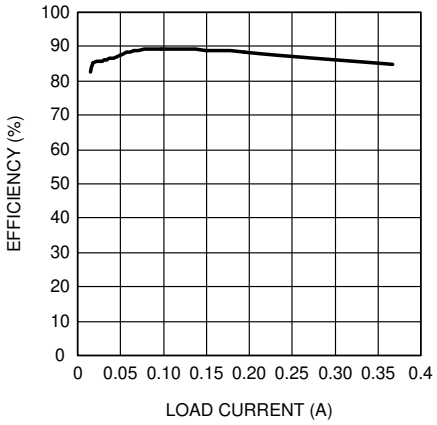


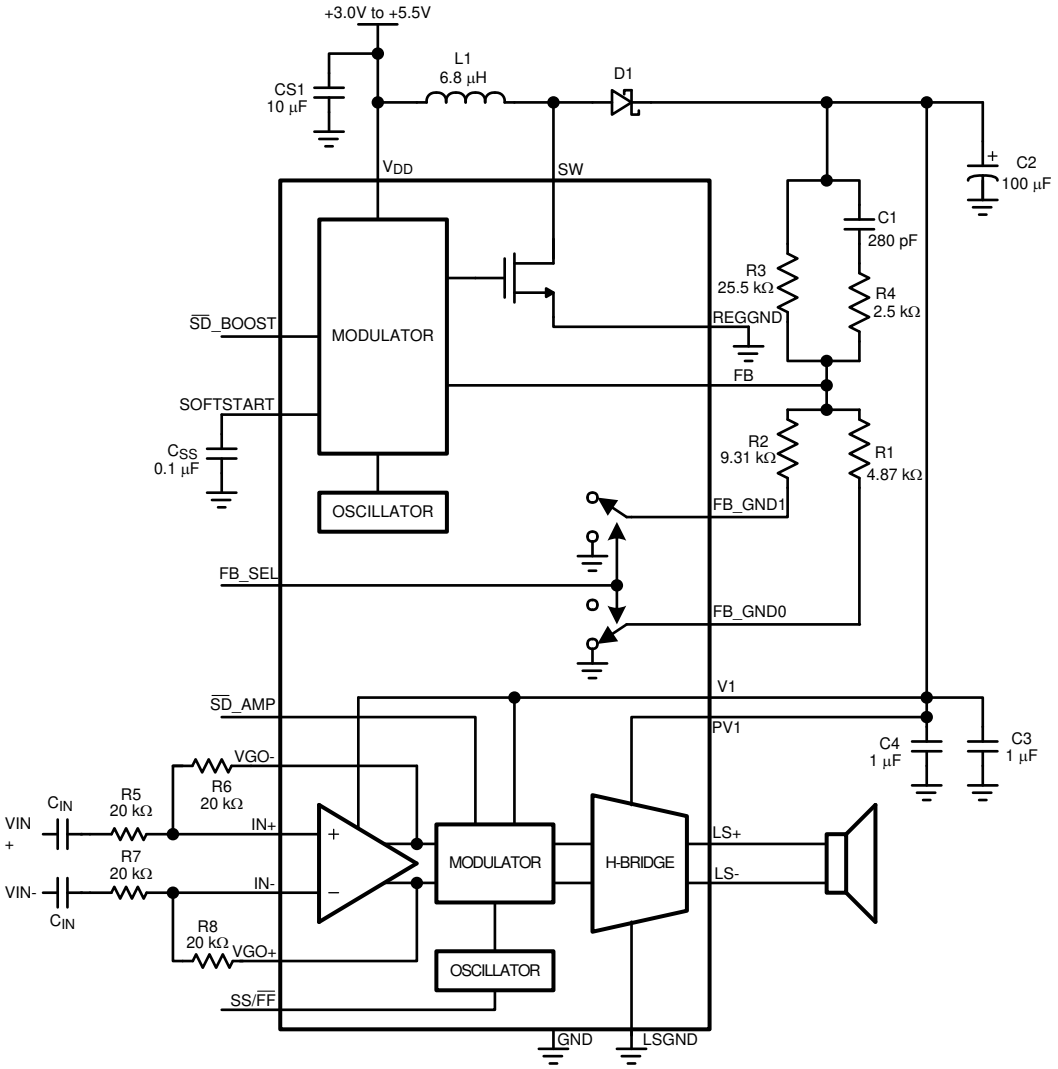
Figure 23. Boost Converter Efficiency vs $I_{LOAD(DC)}$
V_{DD} = 3 V, PV_1 = 4.8 V

7 Detailed Description

7.1 Overview

The LM48511 integrates a boost converter with a high-efficiency Class D audio power amplifier, which features a low-noise PWM architecture that eliminates the output filter, reducing external component count, board area consumption, system cost, and simplifying design. A selectable spread spectrum modulation scheme suppresses RF emissions, further reducing the need for output filters. Two selectable feedback networks allow the LM48511 regulator to dynamically switch between two different output voltages, improving efficiency by optimizing the amplifier's supply voltage based on battery voltage and output power requirements. The gain of the LM48511 is set by external resistors, which allows independent gain control from multiple sources by summing the signals. Output short circuit and thermal overload protection prevent the device from damage during fault conditions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 General Amplifier Function

The LM48511 features a Class D audio power amplifier that uses a filterless modulation scheme, reducing external component count, conserving board space and reducing system cost. The outputs of the device transition from PV1 to GND with a 300-kHz switching frequency. With no signal applied, the outputs (V_{LS+} and V_{LS-}) switch with a 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

With the input signal applied, the duty cycle (pulse width) of the LM48511 outputs changes. For increasing output voltage, the duty cycle of V_{LS+} increases, while the duty cycle of V_{LS-}decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yields the differential output voltage.

7.3.2 Differential Amplifier Explanation

The LM48511 includes fully differential amplifier that features differential input and output stages. A differential amplifier amplifies the difference between the two input signals. Traditional audio power amplifiers have typically offered only single-ended inputs resulting in a 6dB reduction in signal to noise ratio relative to differential inputs. The LM48511 also offers the possibility of DC input coupling which eliminates the two external AC coupling, DC blocking capacitors. The LM48511 can be used, however, as a single-ended input amplifier while still retaining the fully differential benefits of the device. In fact, completely unrelated signals may be placed on the input pins. The LM48511 simply amplifies the difference between the signals. A major benefit of a differential amplifier is the improved common-mode rejection ratio (CMRR) over single input amplifiers. The common-mode rejection characteristic of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in high noise applications.

7.3.3 Audio Amplifier Power Dissipation and Efficiency

The major benefit of a Class D amplifier is increased efficiency versus a Class AB. The efficiency of the LM48511 is attributed to the region of operation of the transistors in the output stage. The Class D output stage acts as current steering switches, consuming negligible amounts of power compared to their Class AB counterparts. Most of the power loss associated with the output stage is due to the IR loss of the MOSFET ON-resistance, along with switching losses due to gate charge.

7.3.4 Regulator Power Dissipation

At higher duty cycles, the increased ON-time of the switch FET means the maximum output current will be determined by power dissipation within the LM48511 FET switch. The switch power dissipation from ON-time conduction is calculated by:

$$P_{D(SWITCH)} = DC \times (I_{INDUCTOR(AVE)})^2 \times R_{DS(ON)} \text{ (W)} \quad (1)$$

where

- DC is the duty cycle.

7.3.5 Shutdown Function

The LM48511 features independent amplifier and regulator shutdown controls, allowing each portion of the device to be disabled or enabled independently. $\overline{SD}$_AMP controls the Class D amplifiers, while $\overline{SD}$_BOOST controls the regulator. Driving either inputs low disables the corresponding portion of the device, and reducing supply current.

When the regulator is disabled, both FB_GND switches open, further reducing shutdown current by eliminating the current path to GND through the regulator feedback network. Without the GND switches, the feedback resistors as shown in the Functional Block Diagram would consume an additional 165 μA from a 5-V supply. With the regulator disabled, there is still a current path from V_{DD}, through the inductor and diode, to the amplifier power supply. This allows the amplifier to operate even when the regulator is disabled. The voltage at PV1 and V1 will be:

$$(V_{DD} – [V_D + (I_L \times DCR)]$$

Where

- V_D is the forward voltage of the Schottky diode
- V_D is the forward voltage of the Schottky diode

Feature Description (continued)

- I_L is the current through the inductor
- DCR is the DC resistance of the inductor (2)

Additionally, when the regulator is disabled, an external voltage from 5 V to 8 V can be applied directly to PV1 and V1 to power the amplifier.

It is best to switch between ground and V_{DD} for minimum current consumption while in shutdown. The LM48511 may be disabled with shutdown voltages in between GND and V_{DD}, the idle current will be greater than the typical 0.1-µA value. Increased THD+N may also be observed when a voltage of less than V_{DD} is applied to SD_AMP .

7.3.6 Regulator Feedback Select

The LM45811 regulator features two feedback paths as shown in the Functional Block Diagram, which allow the regulator to easily switch between two different output voltages. The voltage divider consists of the high side resistor, R3, and the low side resistors (R_{LS}), R1 and R2. R3 is connected to the output of the boost regulator, the mid-point of each divider is connected to FB, and the low side resistors are connected to either FB_GND1 or FB_GND0. FB_SEL determines which FB_GND switch is closed, which in turn determines which feedback path is used. For example if FB_SEL = V_{DD}, the FB_GND1 switch is closed, while the FB_GND0 switch remains open, creating a current path through the resistors connected to FB_GND1. Conversely, if FB_SEL = GND, the FB_GND0 switch is closed, while the FB_GND1 switch remains open, creating a current path through the resistors connected to FB_GND0.

FB_SEL can be susceptible to noise interference. To prevent an accidental state change, either bypass FB_SEL with a 0.1µF capacitor to GND, or connect the higher voltage feedback network to FB_GND0, and the lower voltage feedback network to FB_GND1. Because the higher output voltage configuration typically generates more noise on V_{DD}, this configuration minimizes the V_{DD} noise exposure of FB_SEL, as FB_SEL = GND for FB_GND0 (high voltage output) and FB_SEL = V_{DD} for FB_GND1 (low voltage output).

The selectable feedback networks maximize efficiency in two ways. In applications where the system power supply voltage changes, such as a mobile GPS receiver, that transitions from battery power, to AC line, to a car power adapter, the LM48511 can be configured to generate a lower voltage when the system power supply voltages is lower, and conversely, generate a higher voltage when the system power supply is higher. See the *Setting the Regulator Output Voltage (PV1)* section.

In applications where the same speaker/amplifier combination is used for different purposes with different audio power requirements, such as a cell phone ear piece/speaker phone speaker, the ability to quickly switch between two different voltages allows for optimization of the amplifier power supply, increasing overall system efficiency. When audio power demands are low (ear piece mode) the regulator output voltage can be set lower, reducing quiescent current consumption. When audio power demands increase (speaker phone mode), a higher voltage increases the amplifier headroom, increasing the audio power delivered to the speaker.

7.4 Device Functional Modes

The LM48511 features two modulations schemes, a fixed frequency mode (FF) and a spread spectrum mode (SS).

7.4.1 7.4.1 Fixed Frequency

Select the fixed frequency mode by setting SS/FF = GND. In fixed frequency mode, the amplifier outputs switch at a constant 300 kHz. In fixed frequency mode, the output spectrum consists of the fundamental and its associated harmonics (see *Typical Characteristics*).

7.4.2 7.4.2 Spread Spectrum Mode

Set SS/FF = VDD for spread spectrum mode. The logic selectable spread spectrum mode eliminates the need for output filters, ferrite beads or chokes. In spread spectrum mode, the switching frequency varies randomly by 10% about a 330-kHz center frequency, reducing the wideband spectral contend, improving EMI emissions radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture of the LM48511 spreads that energy over a larger bandwidth (see *Typical Characteristics*). The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM48511 integrates a boost converter with a high-efficiency Class D audio power amplifier, which uses a filterless modulation scheme, reducing external component count, board area consumption and system cost. The major benefit of a Class D amplifier is increased efficiency versus a Class AB. The LM48511 regulator has two selectable feedback paths, which allow the regulator to dynamically switch between two different output voltages easily. In addition, the LM48511 regulator features two different switching modes, improving light load efficiency by minimizing losses due to MOSFET gate charge. The amplifier gain of the LM48511 is set by four external resistors. Careful matching of those resistor pairs is required for optimum performance.

8.2 Typical Application

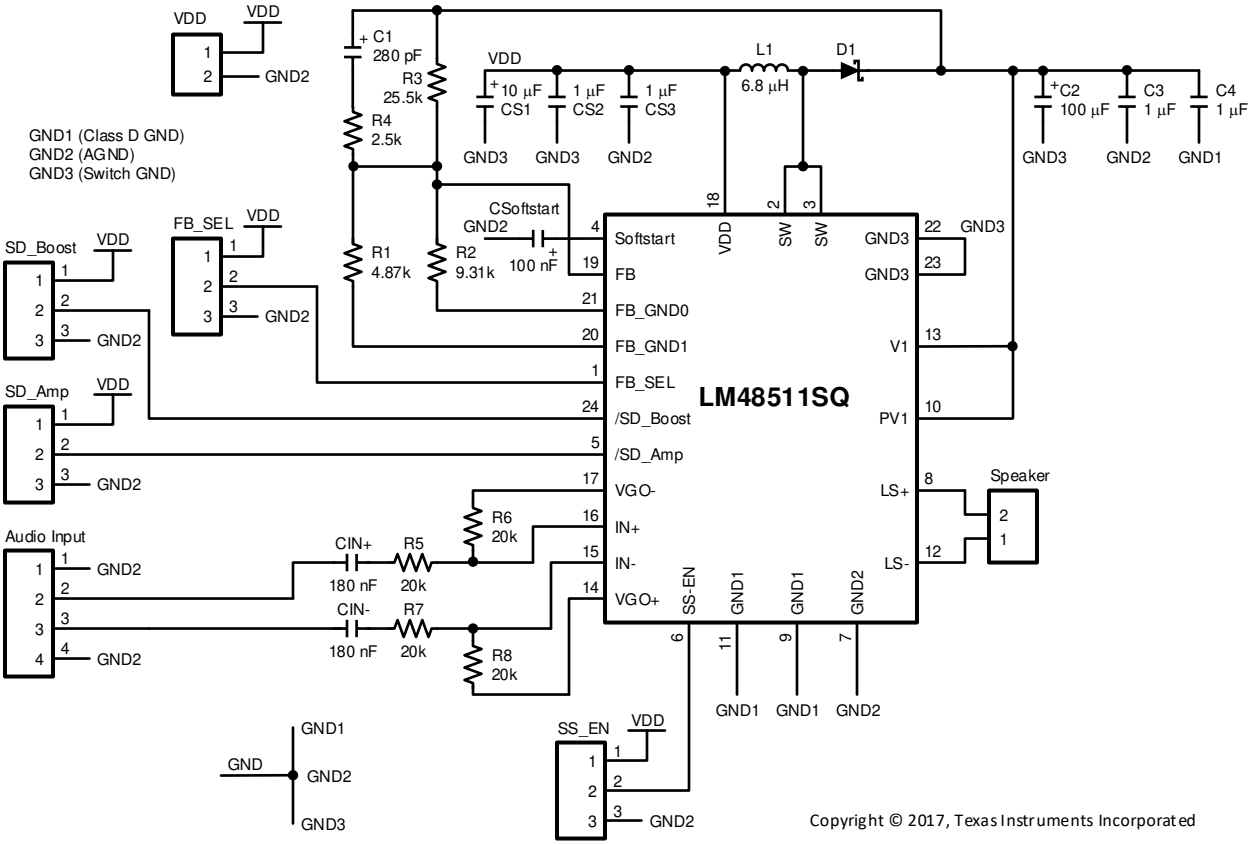


Figure 24. Typical LM48511 Audio Amplifier Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the design parameters for this example.

Table 1. Design Parameters

PARAMETERS	VALUES
Supply voltage range	3.0 V to 5.5 V
Amplifier range	4.8 V to 8 V
Temperature range	–40°C to 85°C

8.2.2 Detailed Design Procedure

8.2.2.1 Proper Selection of External Components

Proper selection of external components in applications using integrated power amplifiers, and switching DC-DC converters, is critical for optimizing device and system performance. Consideration to component values must be used to maximize overall system quality. The best capacitors for use with the switching converter portion of the LM48511 are multi-layer ceramic capacitors. They have the lowest ESR (equivalent series resistance) and highest resonance frequency, which makes them optimum for high-frequency switching converters. When selecting a ceramic capacitor, only X5R and X7R dielectric types must be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult capacitor manufacturer's data curves before selecting a capacitor. High-quality ceramic capacitors can be obtained from Taiyo-Yuden and Murata.

8.2.2.2 Power Supply Bypassing

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both PV1, V1 and V_{DD} pins must be as close to the device as possible.

8.2.2.3 Audio Amplifier Gain Setting Resistor Selection

The amplifier gain of the LM48511 is set by four external resistors, the input resistors, R5 and R7, and the feed back resistors R6 and R8.. The amplifier gain is given by:

Where R_{IN} is the input resistor and R_F is the feedback resistor.

$$A_{VD} = 2 \times R_F / R_{IN} \quad (3)$$

Careful matching of the resistor pairs, R6 and R8, and R5 and R7, is required for optimum performance. Any mismatch between the resistors results in a differential gain error that leads to an increase in THD+N, decrease in PSRR and CMRR, as well as an increase in output offset voltage. Resistors with a tolerance of 1% or better are recommended.

The gain setting resistors must be placed as close to the device as possible. Keeping the input traces close together and of the same length increases noise rejection in noisy environments. Noise coupled onto the input traces which are physically close to each other will be common mode and easily rejected.

8.2.2.4 Audio Amplifier Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48511. The input capacitors create a highpass filter with the input resistors R_{IN}. The -3dB point of the highpass filter is found by:

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (4)$$

In single-ended configurations, the input capacitor value affects click-and-pop performance. The LM48511 features a 50-mg turnon delaly. Choose the input capacitor / input resistor values such that the capacitor is charged before the 50-ms turnon delay expires. A capacitor value of 0.18 μF and a 20-kΩ input resistor are recommended. In differential applications, the charging of the input capacitor does not affect click-and-pop significantly.

The input capacitors can also be used to remove low-frequency content from the audio signal. Highpass filtering the audio signal helps protect speakers that can not reproduce or may be damaged by low frequencies. When the LM48511 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the highpass filter point above the power supply noise frequencies, 217 Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

8.2.2.5 Selecting Regulator Output Capacitor

A single 100-µF low ESR tantalum capacitor provides sufficient output capacitance for most applications. Higher capacitor values improve line regulation and transient response. Typical electrolytic capacitors are not suitable for switching converters that operate above 500 kHz because of significant ringing and temperature rise due to self-heating from ripple current. An output capacitor with excessive ESR reduces phase margin and causes instability.

8.2.2.6 Selecting Regulating Bypass Capacitor

A supply bypass capacitor is required to serve as an energy reservoir for the current which must flow into the coil each time the switch turns on. This capacitor must have extremely low ESR, so ceramic capacitors are the best choice. A nominal value of 10 µF is recommended, but larger values can be used. Because this capacitor reduces the amount of voltage ripple seen at the input pin, it also reduces the amount of EMI passed back along that line to other circuitry.

8.2.2.7 Selecting the Soft-Start (C_{SS}) Capacitor

The soft-start function charges the boost converter reference voltage slowly. This allows the output of the boost converter to ramp up slowly thus limiting the transient current at start-up. Selecting a soft-start capacitor (C_{SS}) value presents a trade off between the wake-up time and the start-up transient current. Using a larger capacitor value will increase wake-up time and decrease start-up transient current while the apposite effect happens with a smaller capacitor value. A general guideline is to use a capacitor value 1000 times smaller than the output capacitance of the boost converter (C2). A 0.1-uF soft-start capacitor is recommended for a typical application.

Table 2 shows the relationship between C_{SS} start-up time and surge current.

Table 2. Soft-Start Capacitor Start-Up Time and Surge Current (1)

C_{SS} (µF)	BOOST SET-UP TIME (ms)	INPUT SURGE CURRENT (mA)
0.1	5.1	330
0.22	10.5	255
0.47	21.7	220

(1) V_{DD} = 5 V, PV_1 = 7.8 V (continuous mode)

8.2.2.8 Selecting Diode (D1)

Use a Schottkey diode, as shown in Figure 24. A 30-V diode such as the DFLS230LH from Diodes Incorporated is recommended. The DFLS230LH diodes are designed to handle a maximum average current of 2 A.

8.2.2.9 Duty Cycle

The maximum duty cycle of the boost converter determines the maximum boost ratio of output-to-input voltage that the converter can attain in continuous mode of operation. The duty cycle for a given boost application is defined by:

$$\text{Duty Cycle} = (PV1 + V_D - V_{DD}) / (PV1 + V_D - V_{SW}) \quad (5)$$

This applies for continuous mode operation.

8.2.2.10 Selecting Inductor Value

Inductor value involves trade-offs in performance. Larger inductors reduce inductor ripple current, which typically means less output voltage ripple (for a given size of output capacitor). Larger inductors also mean more load power can be delivered because the energy stored during each switching cycle is:

$$E = L / 2 \times (I_P)^2$$

Where

- I_P is the peak inductor current (6)

The LM48511 will limit its switch current based on peak current. With I_P fixed, increasing L will increase the maximum amount of power available to the load. Conversely, using too little inductance may limit the amount of load current which can be drawn from the output. Best performance is usually obtained when the converter is operated in “continuous” mode at the load current range of interest, typically giving better load regulation and less output ripple. Continuous operation is defined as not allowing the inductor current to drop to zero during the cycle. Boost converters shift over to discontinuous operation if the load is reduced far enough, but a larger inductor stays continuous over a wider load current range.

8.2.2.11 Inductor Supplies

The recommended inductor for the LM48511 is the IHLP-2525CZ-01 from Vishay Dale. When selecting an inductor, the continuous current rating must be high enough to avoid saturation at peak currents. A suitable core type must be used to minimize switching losses, and DCR losses must be considered when selecting the current rating. Use shielded inductors in systems that are susceptible to RF interference.

8.2.2.12 Setting the Regulator Output Voltage (PV1)

The output voltage of the regulator is set through one of two external resistive voltage-dividers (R3 in combination with either R1 or R2) connected to FB (Figure 24). The resistor, R4 is only for compensation purposes and does not affect the regulator output voltage. The regulator output voltage is set by the following equation:

$$PV1 = V_{FB} [1 + R3 / R_{LS}]$$

Where

- V_{FB} is 1.23 V, and R_{LS} is the low side resistor (R1 or R2) (7)

To simplify resistor selection:

$$R_{LS} = (R3V_{FB}) / (PV1 – V_{FB}) \quad (8)$$

A value of approximately 25.5 kΩ is recommended for R3.

The quiescent current of the boost regulator is directly related to the difference between its input and output voltages, the larger the difference, the higher the quiescent current. For improved power consumption the following regulator input/output voltage combinations are recommended:

Table 3. Recommended Regulator Input and Output Voltages (1)

V_{DD} (V)	PV1 (V)	R3 (kΩ)	R_{LS} (kΩ)	P_{OUT} into 8 Ω (W)
3.0	4.8	25.5	9.31	1
3.6	7.1	25.5	5.35	2.5
5	7.8	25.5	4.87	3

(1) The values of PV1 are for continuous mode operation.

For feedback path selection, see *Regulator Feedback Select*.

8.2.2.13 Discontinuous and Continuous Operation

The LM48511 regulator features two different switching modes. Under light-load conditions, the regulator operates in a variable frequency, discontinuous, pulse-skipping mode, that improves light load efficiency by minimizing losses due to MOSFET gate charge. Under heavy loads, the LM48511 regulator automatically switches to a continuous, fixed-frequency PWM mode, improving load regulation. In discontinuous mode, the regulator output voltage is typically 400 mV higher than the expected (calculated) voltage in continuous mode.

8.2.2.14 I_{SW} Feed-Forward Compensation for Boost Converter

Although the LM48511 regulator is internally compensated, an external feed-forward capacitor, (C1) may be required for stability. The compensation capacitor places a zero in regulator loop response. The recommended frequency of the zero (f_Z) is 22.2 kHz. The value of C1 is given by:

$$C1 = 1 / 2\pi R3 f_Z \quad (9)$$

In addition to C1, a compensation resistor, R4 is required to cancel the zero contributed by the ESR of the regulator output capacitor. Calculate the zero frequency of the output capacitor by:

$$f_{CO} = 1 / 2\pi R_{CO} C_O$$

where

- R_{CO} is the ESR of the output capacitor (10)

The value of R_{FB3} is given by:

$$R4 = 1 / 2\pi f_{CO} C1 \quad (11)$$

8.2.2.15 Calculating Regulator Output Current

The load current of the boost converter is related to the average inductor current by the relation:

$$I_{AMP} = I_{INDUCTOR(AVE)} \times (1 - DC) \text{ (A)}$$

where

- DC is the duty cycle of the application (12)

The switch current can be found by:

$$I_{SW} = I_{INDUCTOR(AVE)} + 1/2 (I_{RIPPLE}) \text{ (A)} \quad (13)$$

Inductor ripple current is dependent on inductance, duty cycle, supply voltage and frequency:

$$I_{RIPPLE} = DC \times (V_{DD} - V_{SW}) / (f \times L) \text{ (A)}$$

where

- f = switching frequency = 1MHz (14)

combining all terms, we can develop an expression which allows the maximum available load current to be calculated:

$$I_{AMP(max)} = (1–DC) \times [I_{SW(max)} – DC (V – V_{SW})] / 2fL \text{ (A)} \quad (15)$$

The equation shown to calculate maximum load current takes into account the losses in the inductor or turnoff switching losses of the FET and diode.

8.2.2.16 Design Parameters V_{SW} and I_{SW}

The value of the FET "ON" voltage (referred to as V_{SW} in Equation 9 thru Equation 12) is dependent on load current. A good approximation can be obtained by multiplying the ON-resistance ($R_{DS(ON)}$ of the FET times the average inductor current. The maximum peak switch current the device can deliver is dependent on duty cycle.

8.2.3 Application Curve

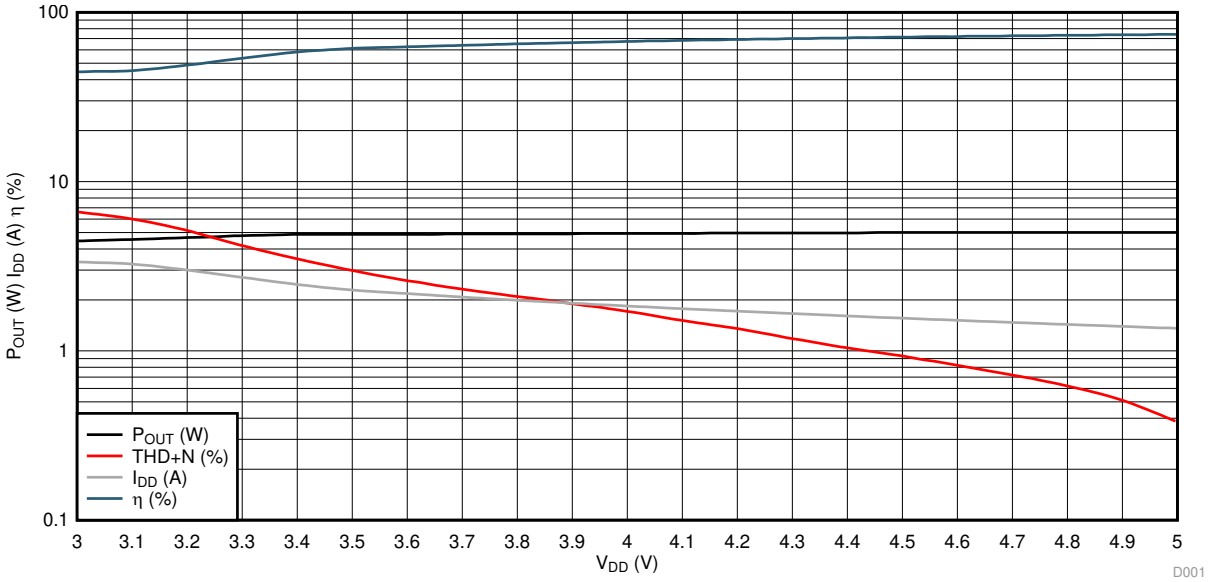


Figure 25. V_{DD} vs P_{OUT}, I_{DD}, and Efficiency With 4-Ω Load

9 Power Supply Recommendations

The devices are designed to operate from an input supply voltage (VDD) operating range from 3 V to 5.5 V, but the absolute maximum rating is 9 V.

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both PV1, V1 and VDD pins must be as close to the device as possible.

10 Layout

10.1 Layout Guidelines

This section provides general practical guidelines for PCB layouts that use various power and ground traces. Designers must note that these are only *rule-of-thumb* recommendations and the actual results are predicated on the final layout.

10.1.1 Power and Ground Circuits

Star trace routing techniques can have a major positive impact on low-level signal performance. Star trace routing refers to using individual traces that radiate from a signal point to feed power and ground to each circuit or even device.

10.1.2 Layout Helpful Hints

- Avoid routing traces under the inductor.
- Use three separate grounds that eventually connect to one point:
  - Signal or quiet ground (GND)
  - Ground for the LM48511 device (LSGND)
  - SW (REGGND) (switch ground). This trace for the switch ground carries the heaviest current (3 A) and therefore is the nosiest. Make this trace as wide and short as possible and keep at a distance from the quiet ground and device ground. Give distance priority to the quiet ground.

10.2 Layout Example

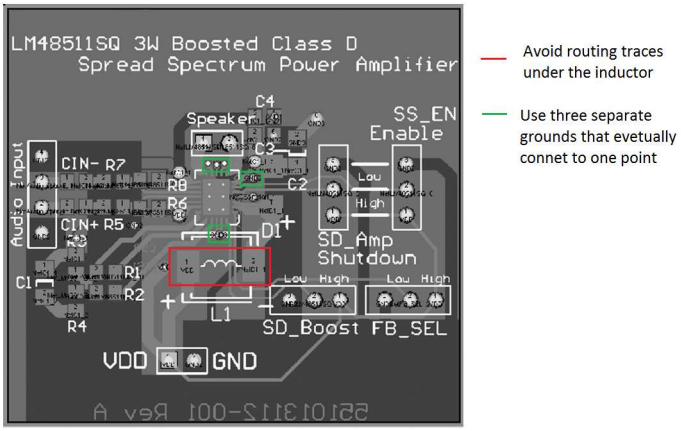


Figure 26. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM48511SQ/NOPB	Active	Production	WQFN (NHZ) | 24	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	48511SQ
LM48511SQ/NOPB.A	Active	Production	WQFN (NHZ) | 24	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	48511SQ
LM48511SQX/NOPB	Active	Production	WQFN (NHZ) | 24	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	48511SQ
LM48511SQX/NOPB.A	Active	Production	WQFN (NHZ) | 24	4500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	48511SQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

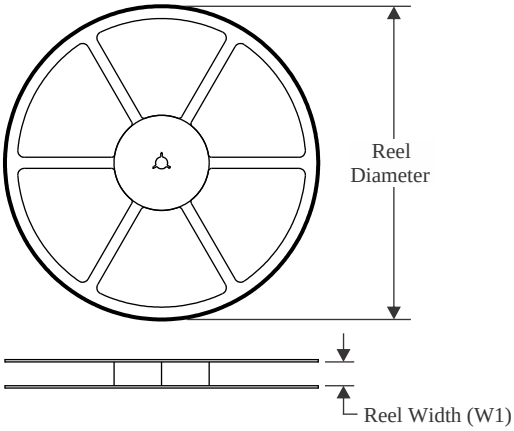
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

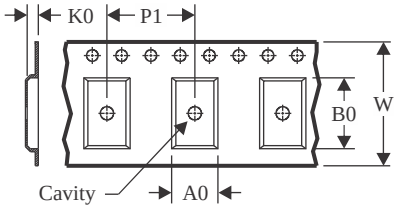
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

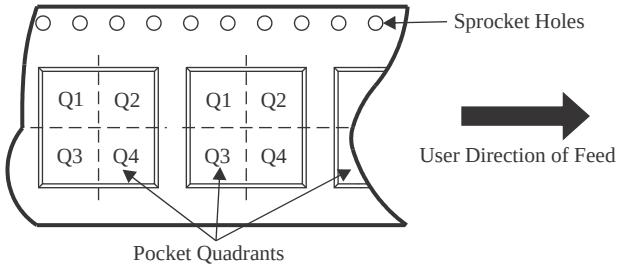


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

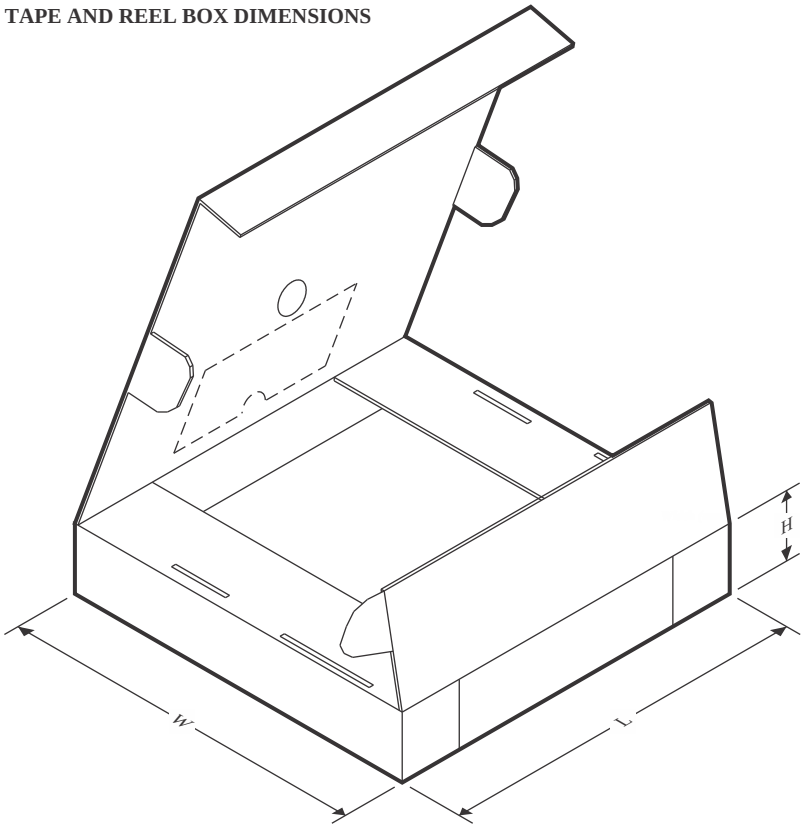
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48511SQ/NOPB	WQFN	NHZ	24	1000	177.8	12.4	4.3	5.3	1.3	8.0	12.0	Q1
LM48511SQX/NOPB	WQFN	NHZ	24	4500	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

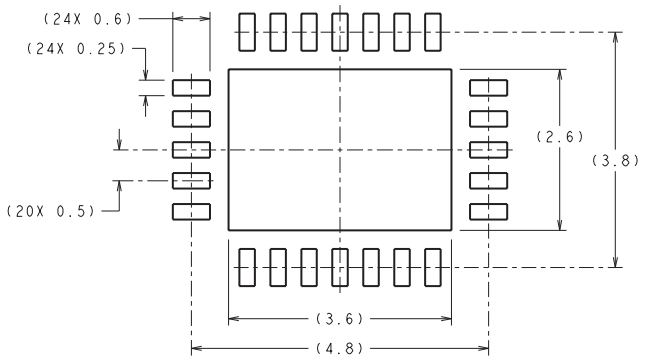
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

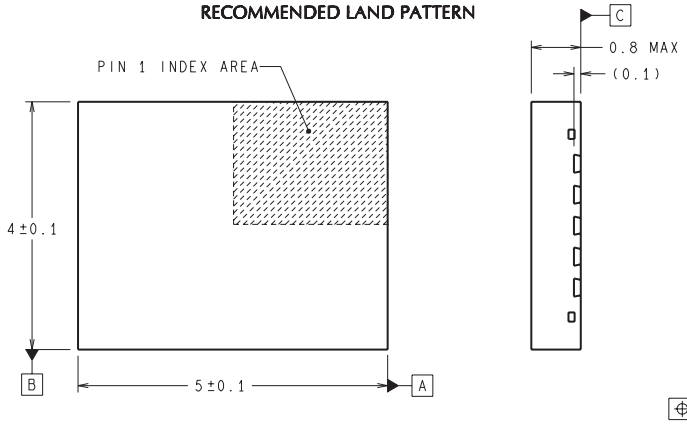
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48511SQ/NOPB	WQFN	NHZ	24	1000	208.0	191.0	35.0
LM48511SQX/NOPB	WQFN	NHZ	24	4500	367.0	367.0	35.0

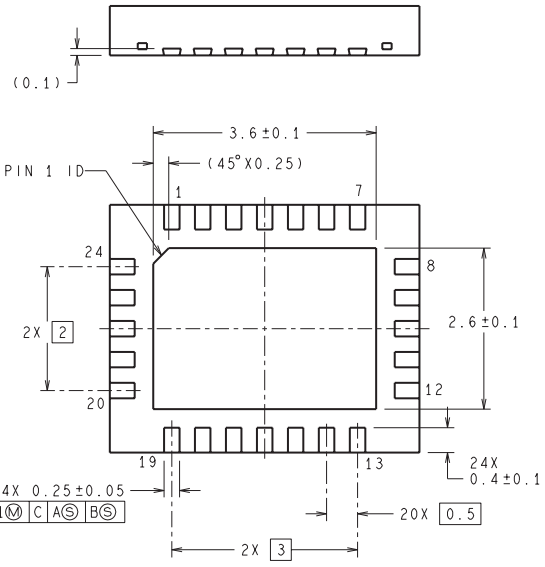
NHZ0024B



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY





SQA24B (Rev A)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265