



CYPRESS

PLDC20G10B/PLDC20G10

## CMOS Generic 24-Pin Reprogrammable Logic Device

### Features

- **Fast**
  - Commercial:  $t_{PD} = 15$  ns,  $t_{CO} = 10$  ns,  $t_s = 12$  ns
  - Military:  $t_{PD} = 20$  ns,  $t_{CO} = 15$  ns,  $t_s = 15$  ns
- **Low power**
  - $I_{CC}$  max.: 70 mA, commercial
  - $I_{CC}$  max.: 100 mA, military
- **Commercial and military temperature range**
- **User-programmable output cells**
  - Selectable for registered or combinational operation
  - Output polarity control
  - Output enable source selectable from pin 13 or product term

- **Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8**
- **Eight product terms and one OE product term per output**
- **CMOS EPROM technology for reprogrammability**
- **Highly reliable**
  - Uses proven EPROM technology
  - Fully AC and DC tested
  - Security feature prevents logic pattern duplication
  - $\pm 10\%$  power supply voltage and higher noise immunity

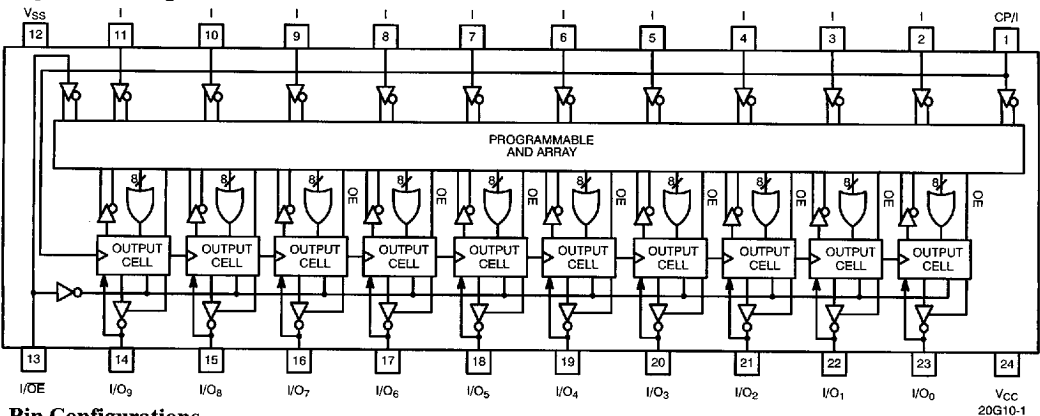
### Functional Description

Cypress PLD devices are high-speed electrically programmable logic devices. These devices utilize the sum-of-products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

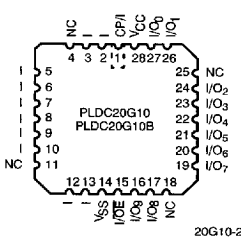
Cypress PLDC20G10 uses an advanced 0.8-micron CMOS technology and a proven EPROM cell as the programmable element. This technology and the inherent

### Logic Block Diagram

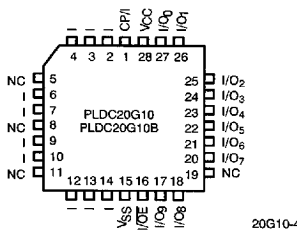


### Pin Configurations

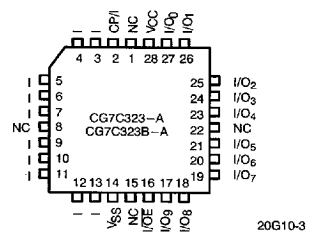
LCC  
Top View



STD PLCC  
Top View



JEDEC PLCC<sup>[1]</sup>  
Top View



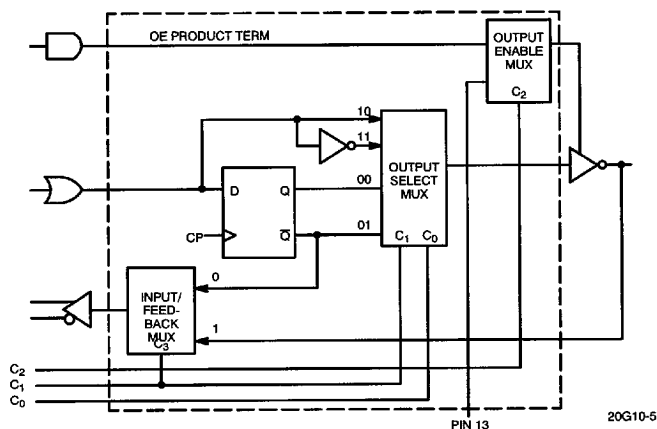
### Note:

1. The CG7C323 is the PLDC20G10 packaged in the JEDEC-compatible 28-pin PLCC pinout. Pin function and pin order is identical for

both PLCC pinouts. The difference is in the location of the "no connect" or NC pins.

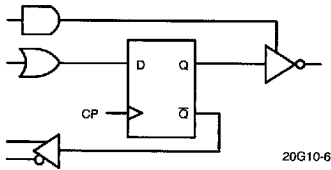
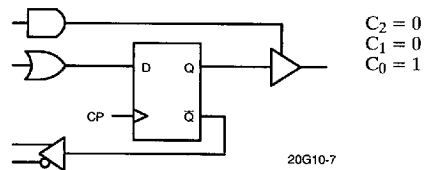
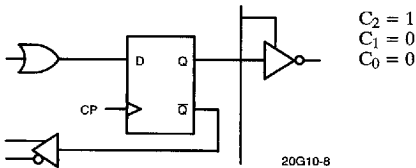
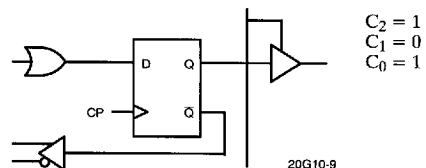
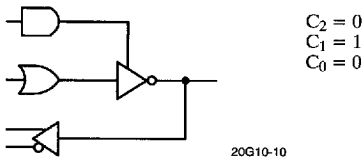
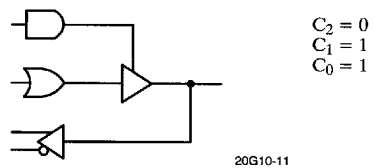
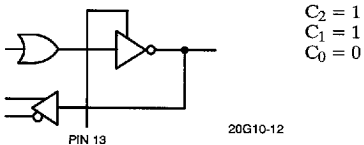
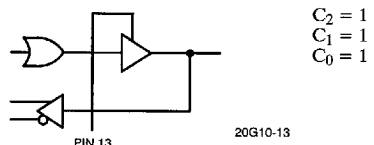


Generic Part Number	I <sub>CC</sub> (mA)		t <sub>PD</sub> (ns)		t <sub>S</sub> (ns)		t <sub>CO</sub> (ns)	
	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
20G10B-15	70		15		12		10	
20G10B-20	70	100	20	20	12	15	12	15
20G10B-25		100		25		18		15
20G10-25	55		25		15		15	
20G10-30		80		30		20		20
20G10-35	55		35		30		25	
20G10-40		80		40		35		25



**Configuration Table**

Figure	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	Configuration
1	0	0	0	Product Term OE/Registered/Active LOW
2	0	0	1	Product Term OE/Registered/Active HIGH
5	0	1	0	Product Term OE/Combinatorial/Active LOW
6	0	1	1	Product Term OE/Combinatorial/Active HIGH
3	1	0	0	Pin 13 OE/Registered/Active LOW
4	1	0	1	Pin 13 OE/Registered/Active HIGH
7	1	1	0	Pin 13 OE/Combinatorial/Active LOW
8	1	1	1	Pin 13 OE/Combinatorial/Active HIGH

**Registered Output Configurations**

**Figure 1. Product Term OE/Active LOW**

**Figure 2. Product Term OE/Active HIGH**

**Figure 3. Pin 13 OE/Active LOW**

**Figure 4. Pin 13 OE/Active HIGH**
**Combinatorial Output Configurations<sup>[2]</sup>**

**Figure 5. Product Term OE/Active LOW**

**Figure 6. Product Term OE/Active HIGH**

**Figure 7. Pin 13 OE/Active LOW**

**Figure 8. Pin 13 OE/Active HIGH**

Note:

2. Bidirectional I/O configurations are possible only when the combinatorial output option is selected

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
Output Current into Outputs (LOW)	16 mA
DC Programming Voltage	
PLDC20G10B and CG7C323B-A	13.0V
PLDC20G10 and CG7C323-A	14.0V

Latch-Up Current	>200 mA
Static Discharge Voltage (per MIL-STD-883, Method 8015)	>500V

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +75°C	5V ±10%
Military <sup>[3]</sup>	-55°C to +125°C	5V ±10%
Industrial	-40°C to +85°C	5V ±10%

**Electrical Characteristics Over the Operating Range (Unless Otherwise Noted)<sup>[4]</sup>**

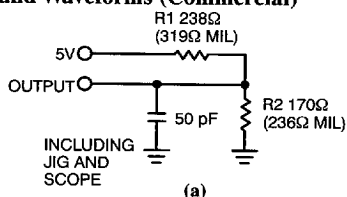
Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -3.2 mA I <sub>OH</sub> = -2 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 12 mA		0.5	V
V <sub>IH</sub>	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[5]</sup>	2.0		V
V <sub>IL</sub>	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs <sup>[5]</sup>		0.8	V
I <sub>IX</sub>	Input Leakage Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-10	+10	μA
I <sub>SC</sub>	Output Short Circuit Current	V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[6, 7]</sup>		-90	mA
I <sub>CC</sub>	Power Supply Current	0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA Unprogrammed Device	Com'l/Ind -15, -20 Com'l/Ind -25, -35 Military -20, -25 Military -30, -40	70 55 100 80	mA
I <sub>OZ</sub>	Output Leakage Current	V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>	-100	100	μA

**Capacitance<sup>[7]</sup>**

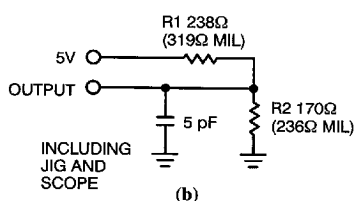
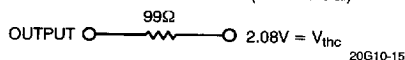
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>IN</sub> = 2.0V, V <sub>CC</sub> = 5.0V	10	pF

**Notes:**

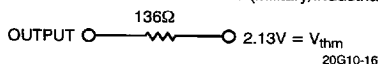
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms (Commercial)**


Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military/Industrial)


**Switching Characteristics Over Operating Range<sup>[3, 8, 9]</sup>**

Parameter	Description	Commercial								Unit
		B-15		B-20		-25		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPD	Input or Feedback to Non-Registered Output		15		20		25		35	ns
tEA	Input to Output Enable		15		20		25		35	ns
tER	Input to Output Disable		15		20		25		35	ns
tPZX	Pin 11 to Output Enable		12		15		20		25	ns
tPXZ	Pin 11 to Output Disable		12		15		20		25	ns
tCO	Clock to Output		10		12		15		25	ns
tS	Input or Feedback Set-Up Time	12		12		15		30		ns
tH	Hold Time	0		0		0		0		ns
tp <sup>[10]</sup>	Clock Period	22		24		30		55		ns
tWH	Clock High Time	8		10		12		17		ns
tWL	Clock Low Time	8		10		12		17		ns
fMAX <sup>[11]</sup>	Maximum Frequency	45.4		41.6		33.3		18.1		MHz

**Notes:**

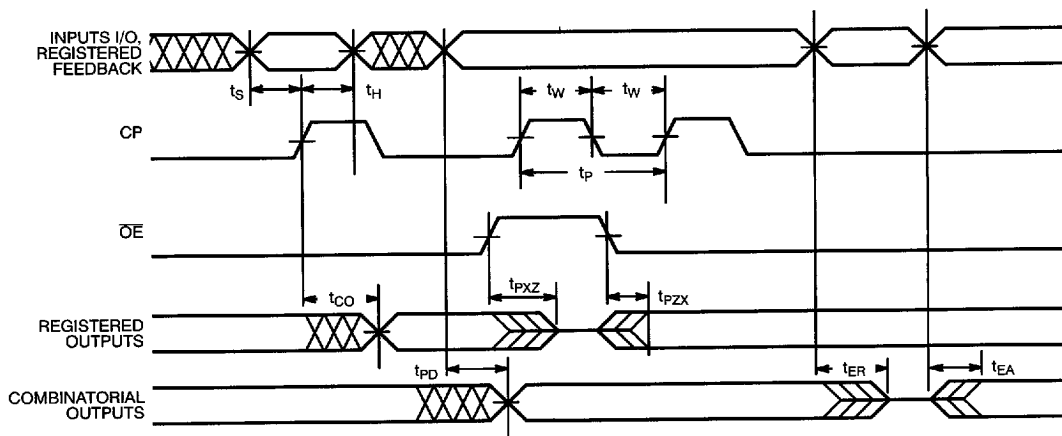
- Part (a) of AC Test Loads and Waveforms used for all parameters except t<sub>ER</sub>, t<sub>PZX</sub>, and t<sub>PXZ</sub>. Part (b) of AC Test Loads and Waveforms used for t<sub>ER</sub>, t<sub>PZX</sub>, and t<sub>PXZ</sub>.
- The parameters t<sub>ER</sub> and t<sub>PXZ</sub> are measured as the delay from the input disable logic threshold transition to V<sub>OH</sub> - 0.5V for an enabled HIGH output or V<sub>OL</sub> + 0.5V for an enabled LOW input.
- t<sub>P</sub> minimum guaranteed clock period is that guaranteed for state machine operation and is calculated from t<sub>P</sub> = t<sub>S</sub> + t<sub>CO</sub>. The minimum

 guaranteed period for registered data path operation (no feedback) can be calculated as the greater of (t<sub>WH</sub> + t<sub>WL</sub>) or (t<sub>S</sub> + t<sub>H</sub>).

- f<sub>MAX</sub>, minimum guaranteed operating frequency, is that guaranteed for state machine operation and is calculated from f<sub>MAX</sub> = 1/(t<sub>S</sub> + t<sub>CO</sub>). The minimum guaranteed f<sub>MAX</sub> for registered data path operation (no feedback) can be calculated as the lower of 1/(t<sub>WH</sub> + t<sub>WL</sub>) or 1/(t<sub>S</sub> + t<sub>H</sub>).

**Switching Characteristics** Over Operating Range<sup>[3, 8, 9]</sup> (continued)

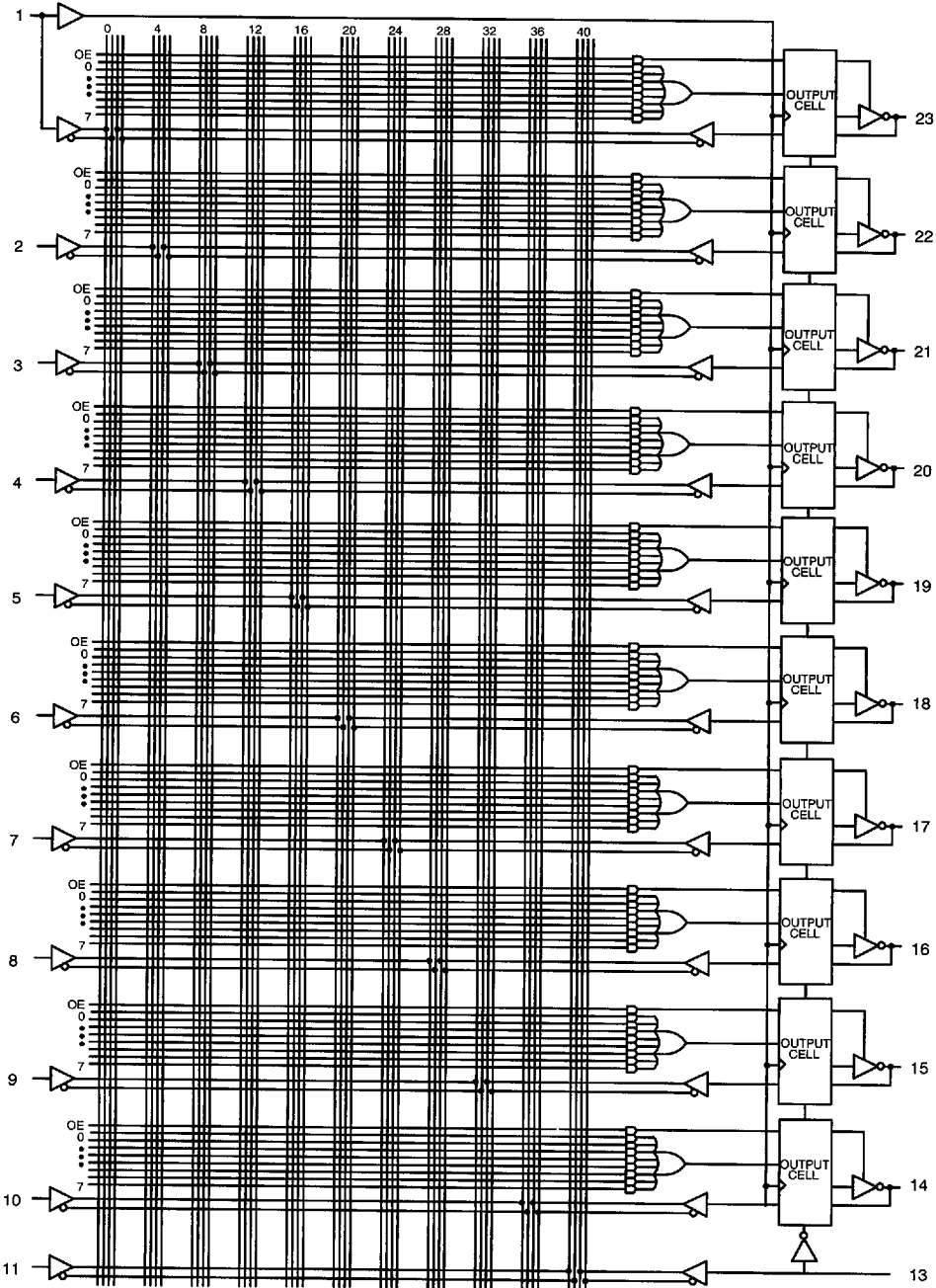
Parameter	Description	Military/Industrial								Unit
		B-20		B-25		-30		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PD</sub>	Input or Feedback to Non-Registered Output		20		25		30		40	ns
t <sub>EA</sub>	Input to Output Enable		20		25		30		40	ns
t <sub>ER</sub>	Input to Output Disable		20		25		30		40	ns
t <sub>PZX</sub>	Pin 11 to Output Enable		17		20		25		25	ns
t <sub>PXZ</sub>	Pin 11 to Output Disable		17		20		25		25	ns
t <sub>CO</sub>	Clock to Output		15		15		20		25	ns
t <sub>S</sub>	Input or Feedback Set-Up Time	15		18		20		35		ns
t <sub>H</sub>	Hold Time	0		0		0		0		ns
t <sub>p</sub> <sup>[10]</sup>	Clock Period	30		33		40		60		ns
t <sub>WH</sub>	Clock High Time	12		14		16		22		ns
t <sub>WL</sub>	Clock Low Time	12		14		16		22		ns
f <sub>MAX</sub> <sup>[11]</sup>	Maximum Frequency	33.3		30.3		25.0		16.6		MHz

**Switching Waveform**


20G10-17



Functional Logic Diagram



2-33

20G10-18

2589662 0016537 671

**Ordering Information**

t <sub>PD</sub> (ns)	t <sub>S</sub> (ns)	t <sub>CO</sub> (ns)	I <sub>CC</sub> (mA)	Ordering Code	Package Name	Package Type	Operating Range
15	12	10	70	PLDC20G10B-15JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	Commercial/ Industrial
				PLDC20G10B-15PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20G10B-15WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C323B-A15JC/JI <sup>[1]</sup>	J64	28-Lead Plastic Leaded Chip Carrier	
20	12	12	70	PLDC20G10B-20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	Commercial/ Industrial
				PLDC20G10B-20PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20G10B-20WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C323B-A20JC/JI <sup>[1]</sup>	J64	28-Lead Plastic Leaded Chip Carrier	
20	15	15	100	PLDC20G10B-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10B-20LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10B-20WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
25	15	15	55	PLDC20G10-25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	Commercial/ Industrial
				PLDC20G10-25PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20G10-25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C323-A25JC/JI <sup>[1]</sup>	J64	28-Lead Plastic Leaded Chip Carrier	
25	18	15	100	PLDC20G10B-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10B-25LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10B-25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
30	20	20	80	PLDC20G10-30DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10-30LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10-30WMB	W14	24-Lead (300-Mil) Windowed CerDIP	
35	30	25	55	PLDC20G10-35JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	Commercial/ Industrial
				PLDC20G10-35PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PLDC20G10-35WC	W14	24-Lead (300-Mil) Windowed CerDIP	
				CG7C323-A35JC/JI <sup>[1]</sup>	J64	28-Lead Plastic Leaded Chip Carrier	
40	35	25	80	PLDC20G10-40DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PLDC20G10-40LMB	L64	28-Square Leadless Chip Carrier	
				PLDC20G10-40WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL</sub>	1, 2, 3
I <sub>IX</sub>	1, 2, 3
I <sub>OZ</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
t <sub>PD</sub>	9, 10, 11
t <sub>PZX</sub>	9, 10, 11
t <sub>CO</sub>	9, 10, 11
t <sub>S</sub>	9, 10, 11
t <sub>H</sub>	9, 10, 11

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