

# SN54CBT16244, SN74CBT16244 16-BIT FET BUS SWITCHES

SCDS031I – MAY 1996 – REVISED OCTOBER 2000

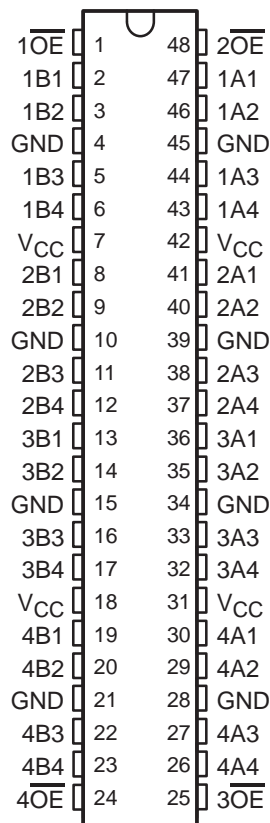
- Members of Texas Instruments' Widebus™ Family
- Standard '16244-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

## description

The 'CBT16244 devices provide 16 bits of high-speed TTL-compatible bus switching in a standard '16244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

These devices are organized as four 4-bit low-impedance switches with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the switch is on, and data can flow from port A to port B, or vice versa. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the two ports.

## SN54CBT16244 . . . WD PACKAGE SN74CBT16244 . . . DGG, DGV, OR DL PACKAGE (TOP VIEW)



## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBT16244DL	CBT16244
		Tape and reel	SN74CBT16244DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16244DGGR	CBT16244
	TVSOP – DGV	Tape and reel	SN74CBT16244DGVR	CY244
–55°C to 125°C	CFP – WD	Tube	SNJ54CBT16244WD	SNJ54CBT16244WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each 4-bit bus switch)

INPUT $\overline{OE}$	OUTPUTS A, B
L	A port = B port
H	Disconnect



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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The four diagrams illustrate the internal structure of a 4-to-1 multiplexer using 2N7000 NMOS transistors and inverters. Each diagram shows a different input combination (1A, 2A, 3A, 4A) and the resulting output (1B, 2B, 3B, 4B).

- Diagram 1 (Top Left):** Input 1A is connected to the gate of the first NMOS transistor. Input 1A4 is connected to the gate of the second NMOS transistor. The output of the first inverter is connected to the gate of the third NMOS transistor. The output of the second inverter is connected to the gate of the fourth NMOS transistor. The output of the first inverter is also connected to the gate of the second NMOS transistor. The output of the second inverter is also connected to the gate of the third NMOS transistor. The output of the first inverter is also connected to the gate of the fourth NMOS transistor. The output of the second inverter is also connected to the gate of the first NMOS transistor.
- Diagram 2 (Top Right):** Input 2A is connected to the gate of the first NMOS transistor. Input 2A4 is connected to the gate of the second NMOS transistor. The output of the first inverter is connected to the gate of the third NMOS transistor. The output of the second inverter is connected to the gate of the fourth NMOS transistor. The output of the first inverter is also connected to the gate of the second NMOS transistor. The output of the second inverter is also connected to the gate of the third NMOS transistor. The output of the first inverter is also connected to the gate of the fourth NMOS transistor. The output of the second inverter is also connected to the gate of the first NMOS transistor.
- Diagram 3 (Bottom Left):** Input 3A is connected to the gate of the first NMOS transistor. Input 3A4 is connected to the gate of the second NMOS transistor. The output of the first inverter is connected to the gate of the third NMOS transistor. The output of the second inverter is connected to the gate of the fourth NMOS transistor. The output of the first inverter is also connected to the gate of the second NMOS transistor. The output of the second inverter is also connected to the gate of the third NMOS transistor. The output of the first inverter is also connected to the gate of the fourth NMOS transistor. The output of the second inverter is also connected to the gate of the first NMOS transistor.
- Diagram 4 (Bottom Right):** Input 4A is connected to the gate of the first NMOS transistor. Input 4A4 is connected to the gate of the second NMOS transistor. The output of the first inverter is connected to the gate of the third NMOS transistor. The output of the second inverter is connected to the gate of the fourth NMOS transistor. The output of the first inverter is also connected to the gate of the second NMOS transistor. The output of the second inverter is also connected to the gate of the third NMOS transistor. The output of the first inverter is also connected to the gate of the fourth NMOS transistor. The output of the second inverter is also connected to the gate of the first NMOS transistor.

Supply voltage range, V <sub>CC</sub>	-0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I/O</sub> < 0)	-50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DGG package	70°C/W
DGV package	58°C/W
DL package	63°C/W
Storage temperature range, T <sub>stg</sub>	-65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51-7.

		SN54CBT16244		SN74CBT16244		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4	5.5	4	5.5	V
V <sub>IH</sub>	High-level control input voltage	2		2		V
V <sub>IL</sub>	Low-level control input voltage		0.8		0.8	V
T <sub>A</sub>	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54CBT16244		SN74CBT16244		UNIT
				MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = −18 mA		−1.2		−1.2		V
I <sub>I</sub>		V <sub>CC</sub> = 0	V <sub>I</sub> = 5.5 V	10		10		μA
		V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 5.5 V or GND	±1		±1		
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0,		3.2		3		μA
ΔI <sub>CC</sub> ‡	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND		2.5		2.5		mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 3 V or 0		2.5		2.5		pF
C <sub>io</sub> (OFF)		V <sub>O</sub> = 3 V or 0, $\overline{OE}$ = V <sub>CC</sub>		4.5		4.5		pF
r <sub>on</sub> §		V <sub>CC</sub> = 4 V, V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA		20		20		Ω
		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0, I <sub>I</sub> = 64 mA	5	10	5	7	
			V <sub>I</sub> = 0, I <sub>I</sub> = 30 mA	5	10	5	7	
			V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA	8	14	8	12	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBT16244				SN74CBT16244				UNIT
			V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub> <sup>¶</sup>	A or B	B or A			0.8*		0.35		0.25	ns	
t <sub>en</sub>	$\overline{OE}$	A or B		10.3	1	9.2		5.5	1	5.1	ns
t <sub>dis</sub>	$\overline{OE}$	A or B		9.7	1	8.2		5.2	1	5.4	ns

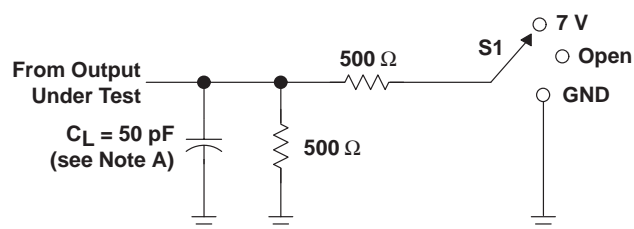
\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

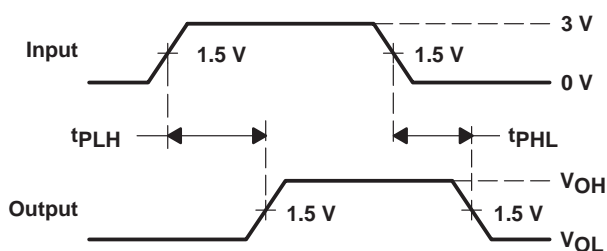
# SN54CBT16244, SN74CBT16244 16-BIT FET BUS SWITCHES

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## PARAMETER MEASUREMENT INFORMATION

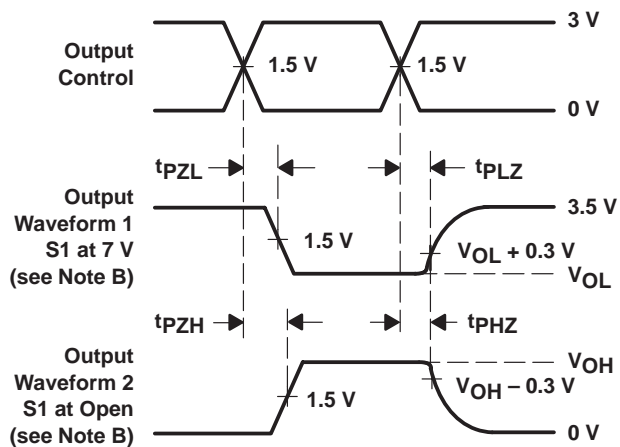


LOAD CIRCUIT



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9855301QXA	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9855301QX A SNJ54CBT16244W D	<a href="#">Samples</a>
74CBT16244DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	<a href="#">Samples</a>
74CBT16244DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	<a href="#">Samples</a>
74CBT16244DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY244	<a href="#">Samples</a>
74CBT16244DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY244	<a href="#">Samples</a>
SN74CBT16244DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	<a href="#">Samples</a>
SN74CBT16244DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY244	<a href="#">Samples</a>
SN74CBT16244DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	<a href="#">Samples</a>
SN74CBT16244DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	<a href="#">Samples</a>
SN74CBT16244DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	<a href="#">Samples</a>
SN74CBT16244DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT16244	<a href="#">Samples</a>
SNJ54CBT16244WD	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9855301QX A SNJ54CBT16244W D	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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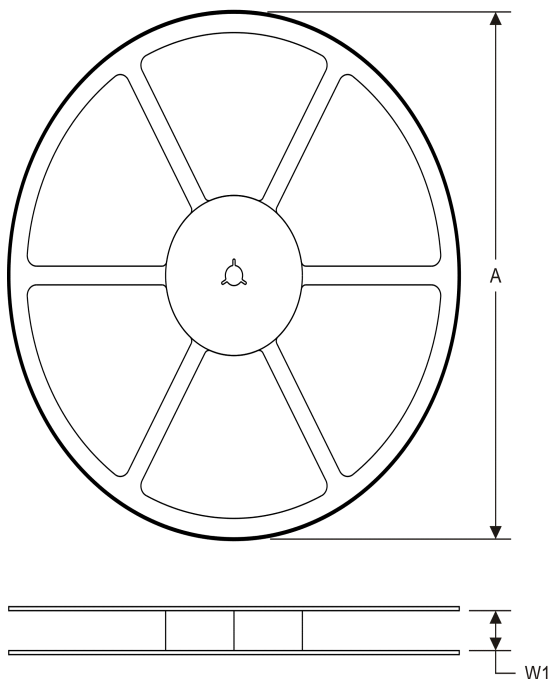
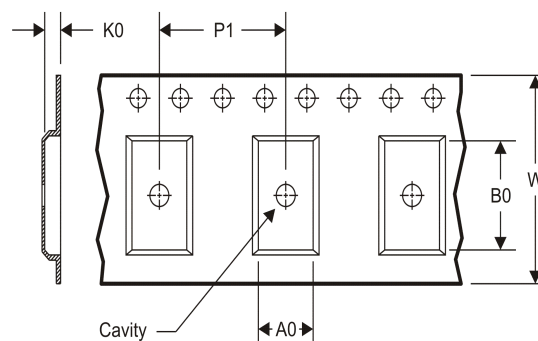
#### **OTHER QUALIFIED VERSIONS OF SN54CBT16244, SN74CBT16244 :**

● Catalog: [SN74CBT16244](#)

● Military: [SN54CBT16244](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


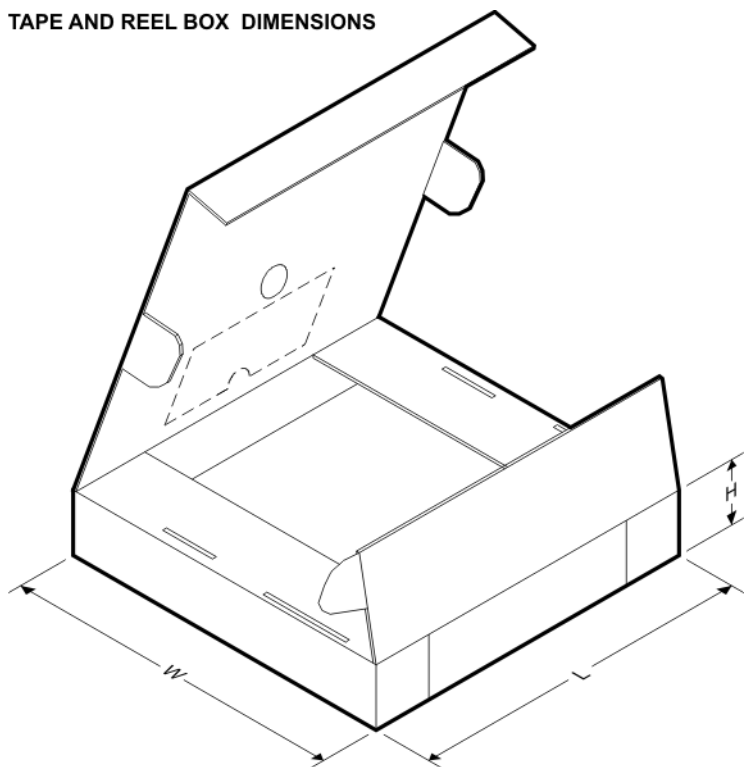
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74CBT16244DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74CBT16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

## TAPE AND REEL BOX DIMENSIONS



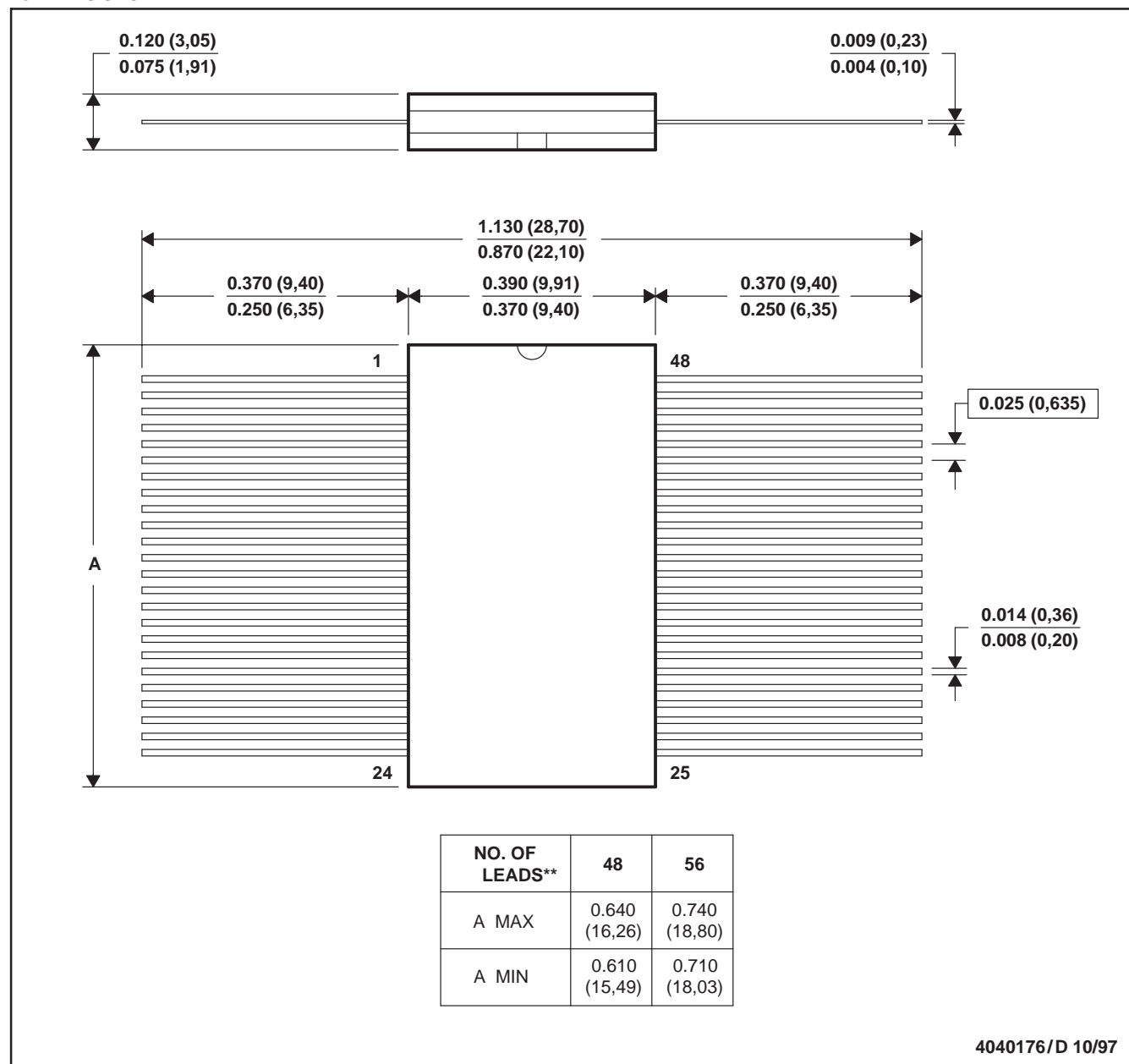
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT16244DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74CBT16244DGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74CBT16244DLR	SSOP	DL	48	1000	367.0	367.0	55.0

## WD (R-GDFP-F\*\*)

## CERAMIC DUAL FLATPACK

48 LEADS SHOWN

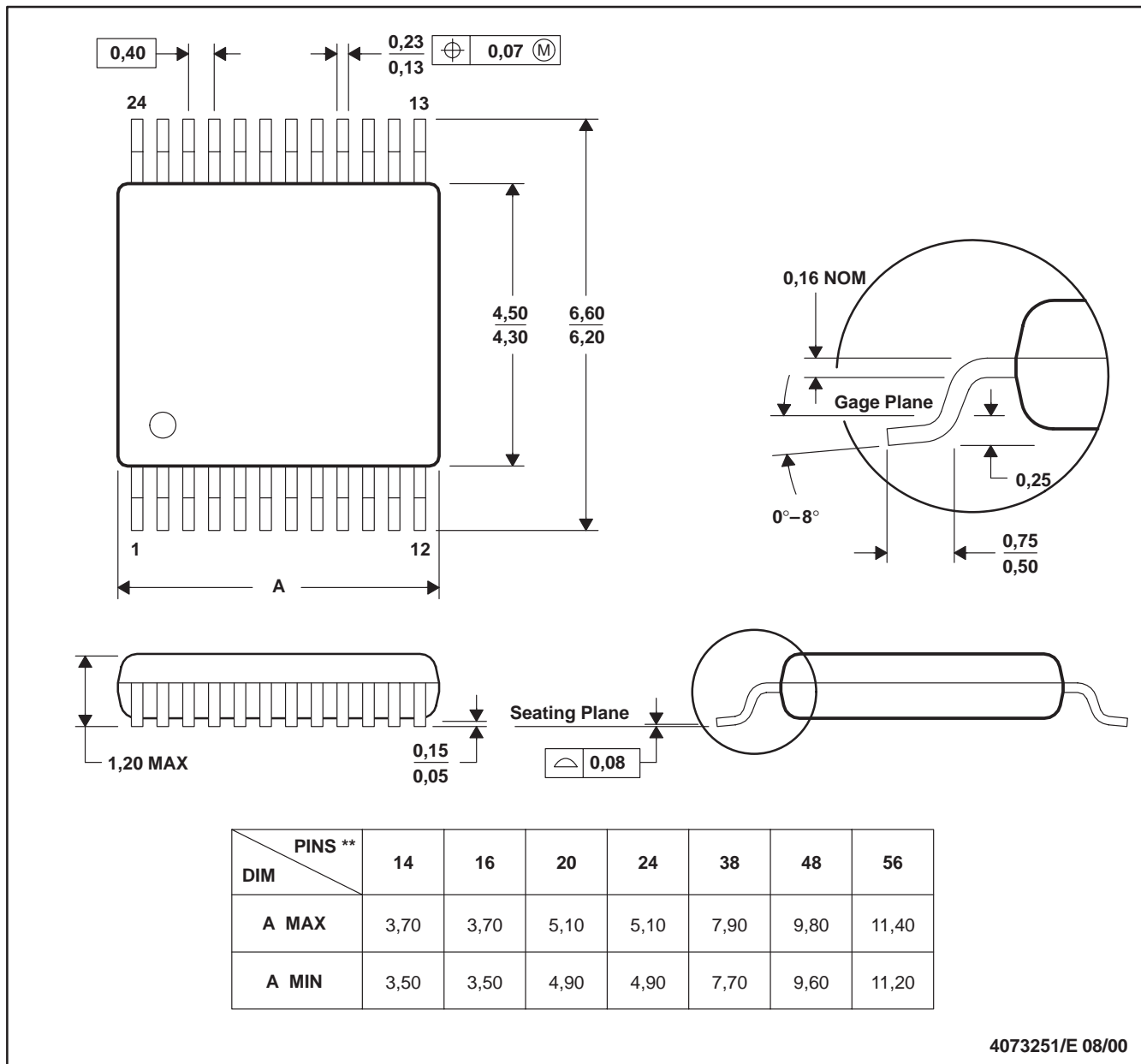


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

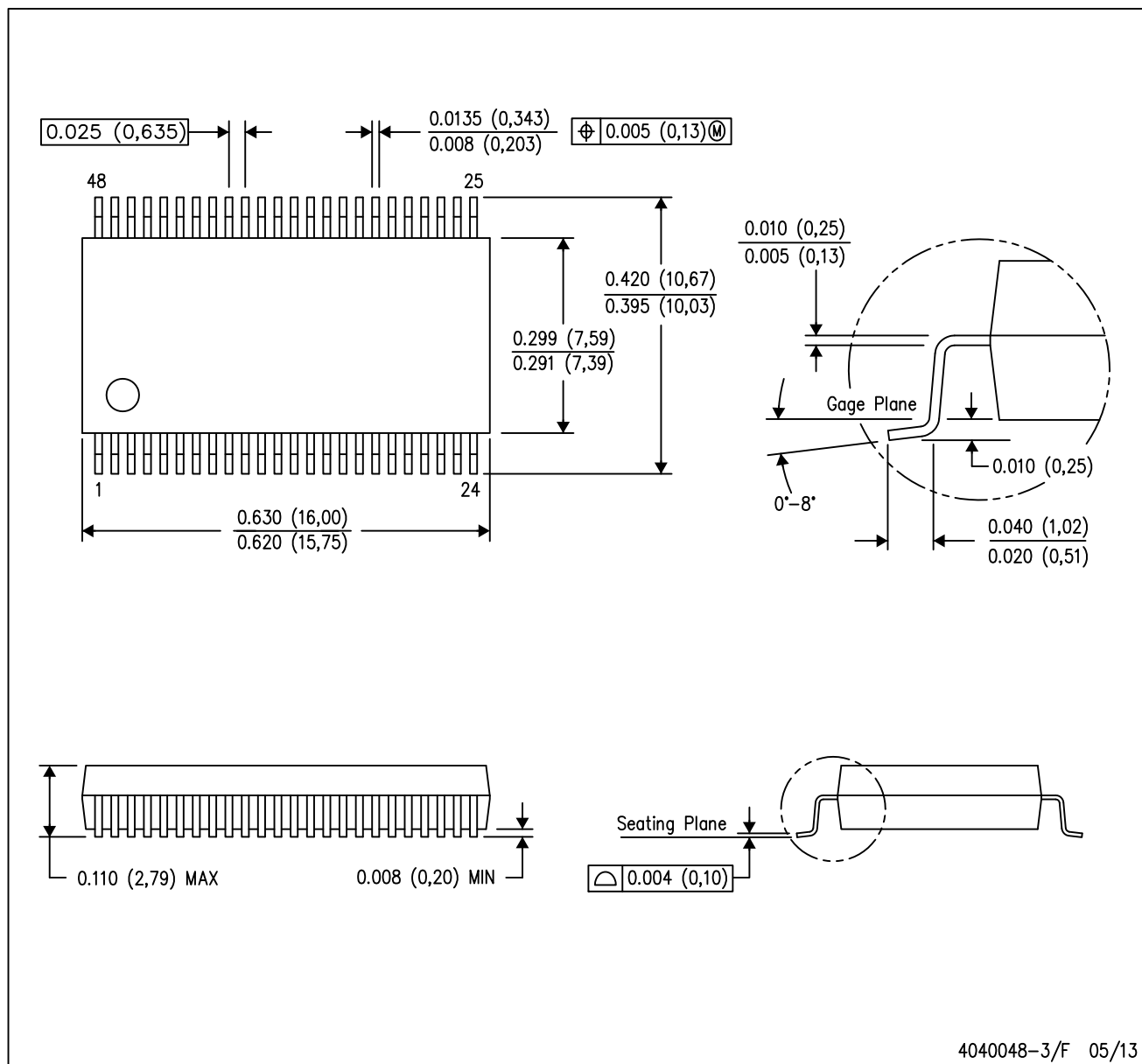
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE

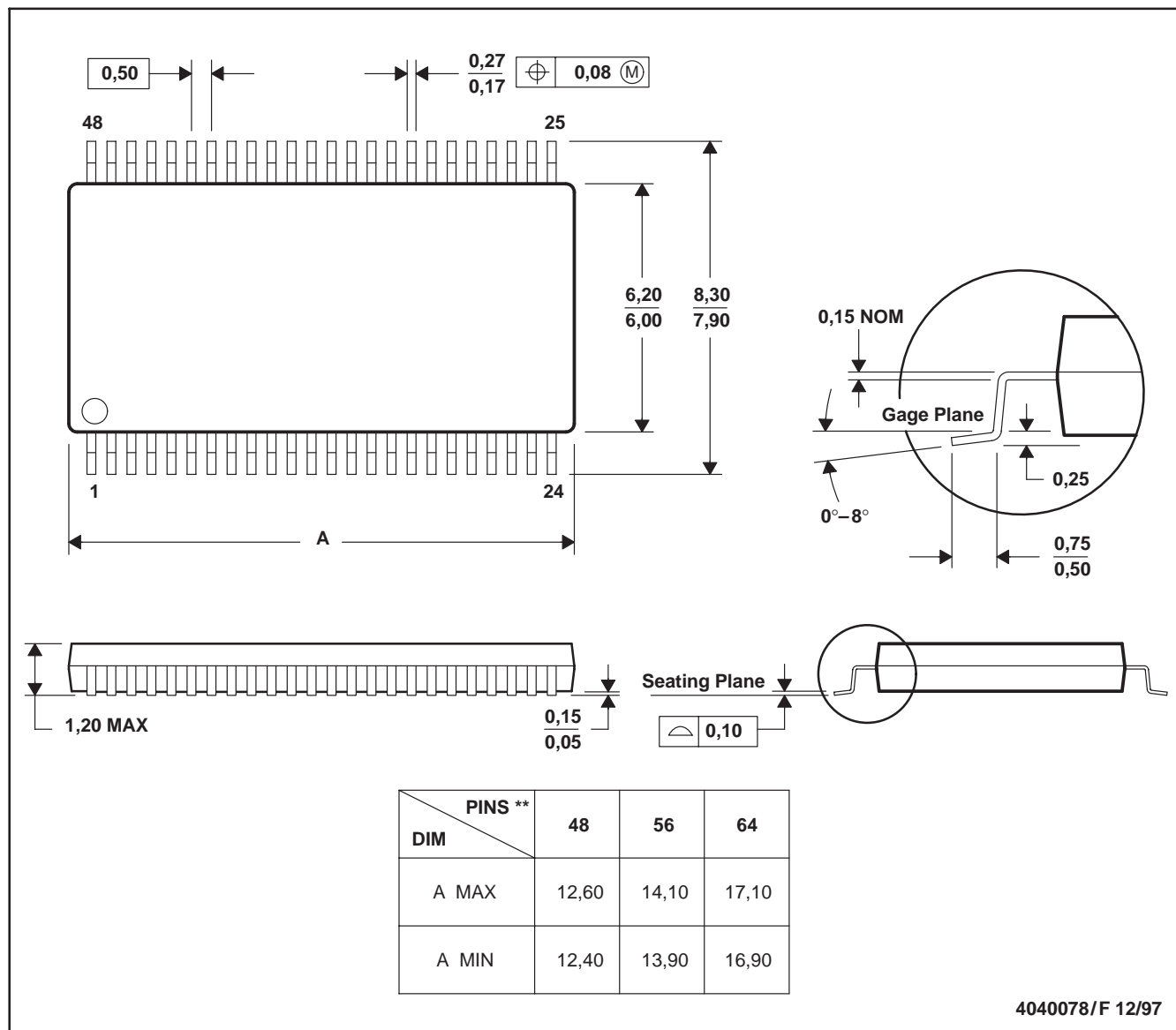


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
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