

MM74HC259

8-Bit Addressable Latch/3-to-8 Line Decoder

General Description

The MM74HC259 device utilizes advanced silicon-gate CMOS technology to implement an 8-bit addressable latch, designed for general purpose storage applications in digital systems.

The MM74HC259 has a single data input (D), 8 latch outputs (Q1–Q8), 3 address inputs (A, B, and C), a common enable input (G), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken LOW the data flows through to the addressed output. The data is stored when ENABLE transitions from LOW-to-HIGH. All unaddressed latches will remain unaffected. With enable in the HIGH state the device is deselected, and all latches remain in their previous state, unaffected by changes on the data or address

inputs. To eliminate the possibility of entering erroneous data into the latches, the enable should be held HIGH (inactive) while the address lines are changing.

If enable is held HIGH and CLEAR is taken LOW all eight latches are cleared to a LOW state. If enable is LOW all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

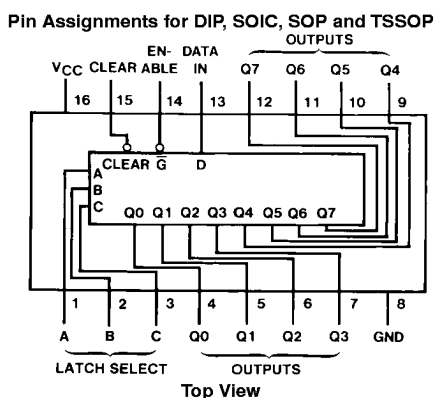
- Typical propagation delay: 18 ns
- Wide supply range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum (74HC Series)

Ordering Code:

Order Number	Package Number	Package Description
MM74HC259M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC259SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC259MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC259N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Latch Selection Table

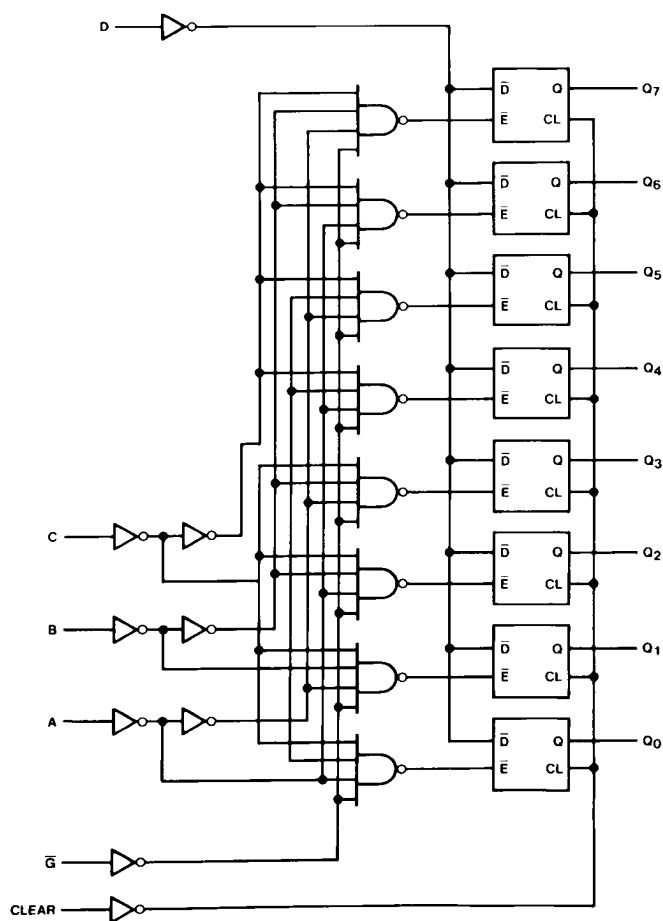
Select Inputs			Latch
C	B	A	Addressed
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = HIGH level, L = LOW level
D = the level at the data input
Q_i the level of Q_i (i = 0, 1...7, as appropriate)
before the indicated steady-state input conditions were established.

Truth Table

Inputs		Outputs of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch Memory 8-Line Decoder Clear
H	H	Q_{i0}	Q_{i0}	
L	L	D	L	
L	H	L	L	

Logic Diagram



Absolute Maximum Ratings				Recommended Operating Conditions			
(Note 2)							
Supply Voltage (V _{CC})		-0.5 to +7.0V		Min	Max	Units	
DC Input Voltage (V _{IN})		-1.5 to V _{CC} +1.5V		2	6	V	
DC Output Voltage (V _{OUT})		-0.5 to V _{CC} +0.5V		0	V _{CC}	V	
Clamp Diode Current (I _{IK} , I _{OK})		±20 mA		(V _{IN} , V _{OUT})			
DC Output Current, per pin (I _{OUT})		±25 mA		Operating Temperature Range (T _A)			
DC V _{CC} or GND Current, per pin (I _{CC})		±50 mA		Input Rise or Fall Times			
Storage Temperature Range (T _{STG})		-65°C to +150°C		(t _r , t _f) V _{CC} = 2.0V			
Power Dissipation (P _D)				V _{CC} = 4.5V			
(Note 3)		600 mW		V _{CC} = 6.0V			
S.O. Package only		500 mW					
Lead Temperature (T _L)				Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.			
(Soldering 10 seconds)		260°C		Note 2: Unless otherwise specified all voltages are referenced to ground.			
				Note 3: Power Dissipation temperature derating — plastic "N" package: — 12 mW/°C from 65°C to 85°C			

DC Electrical Characteristics								(Note 4)
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

($V_{CC} = 5.0V$, $T_A = 25^\circ C$, $t_r = t_f = 6\text{ ns}$, $C_L = 15\text{ pF}$ unless otherwise specified.)

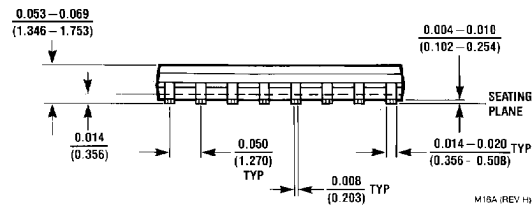
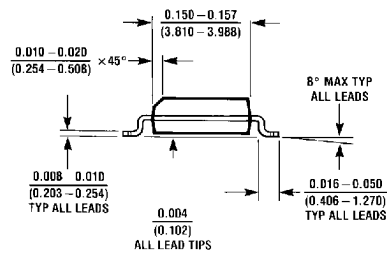
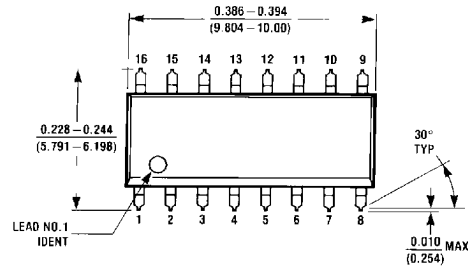
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		18	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		20	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		20	35	ns
t_{PHL}	Maximum Propagation Delay Clear to Output		17	27	ns
t_W	Minimum Enable Pulse Width		10	16	ns
t_W	Minimum Clear Pulse Width		10	16	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	ns
t_s	Minimum Setup Time Select or Data to Enable		15	20	ns
t_H	Minimum Hold Time Data or Address to Enable		-2	0	ns

AC Electrical Characteristics

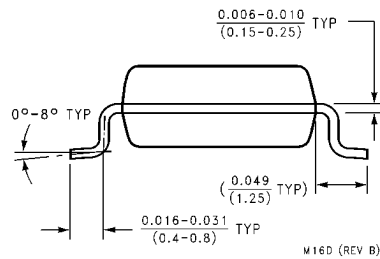
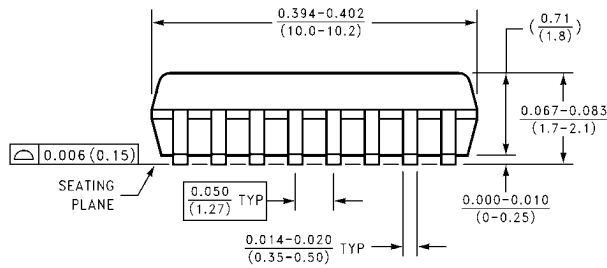
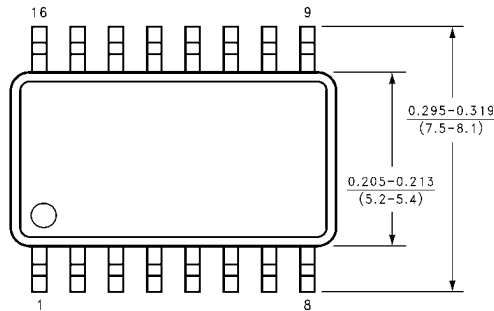
$t_r = t_f = 6\text{ ns}$, $C_L = 50\text{ pF}$, $V_{CC} = 2.0V - 6.0V$

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
				Typ	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay Data to Output		2.0V	60	180	225	250	ns
			4.5V	19	37	46	52	ns
			6.0V	17	32	40	45	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Select to Output		2.0V	72	220	275	310	ns
			4.5V	21	43	54	60	ns
			6.0V	18	37	46	52	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Enable to Output		2.0V	65	200	250	280	ns
			4.5V	27	40	50	58	ns
			6.0V	23	35	44	50	ns
t _{PHL}	Maximum Propagation Delay Clear to Output		2.0V	50	150	190	210	ns
			4.5V	18	31	39	44	ns
			6.0V	16	26	32	37	ns
t _W	Minimum Pulse Width Clear or Enable		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t _s	Minimum Setup Time Address or Data to Enable		2.0V		100	125	150	ns
			4.5V		20	25	28	ns
			6.0V		15	19	25	ns
t _H	Minimum Hold Time Address or Data to Enable		2.0V	-10	0	0	0	ns
			4.5V	-2	0	0	0	ns
			6.0V	-2	0	0	0	ns
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C _{IN}	Input Capacitance			5	10	10	10	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	(per package)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} S V_{CC} f + I_{CC}$.

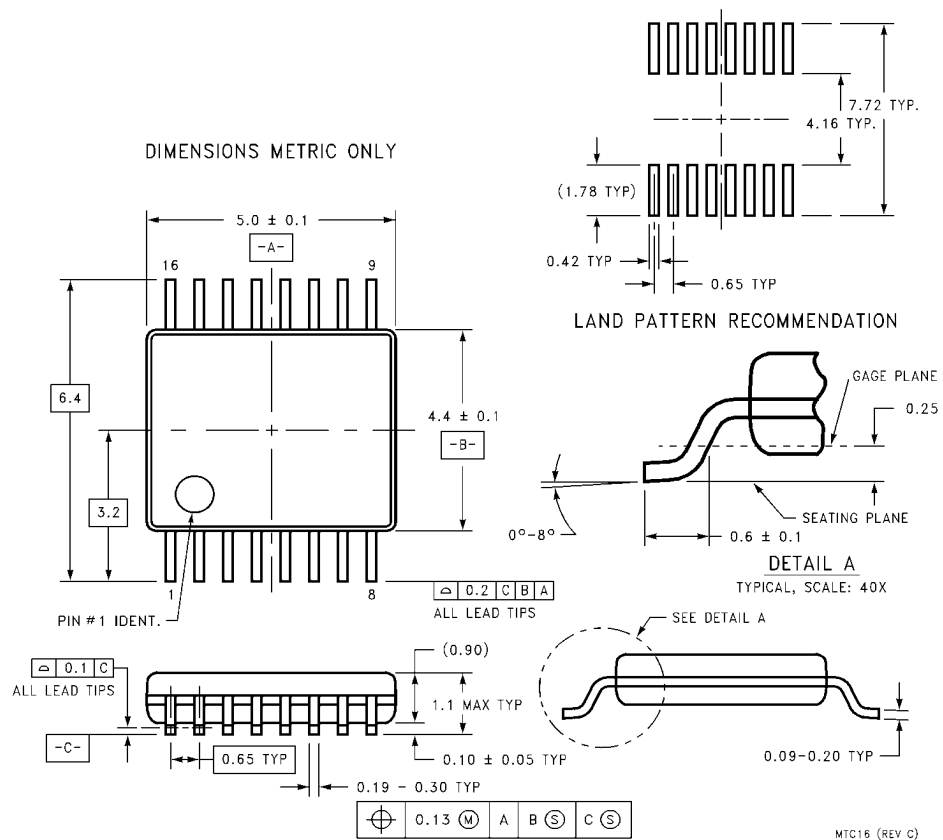
Physical Dimensions inches (millimeters) unless otherwise noted


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

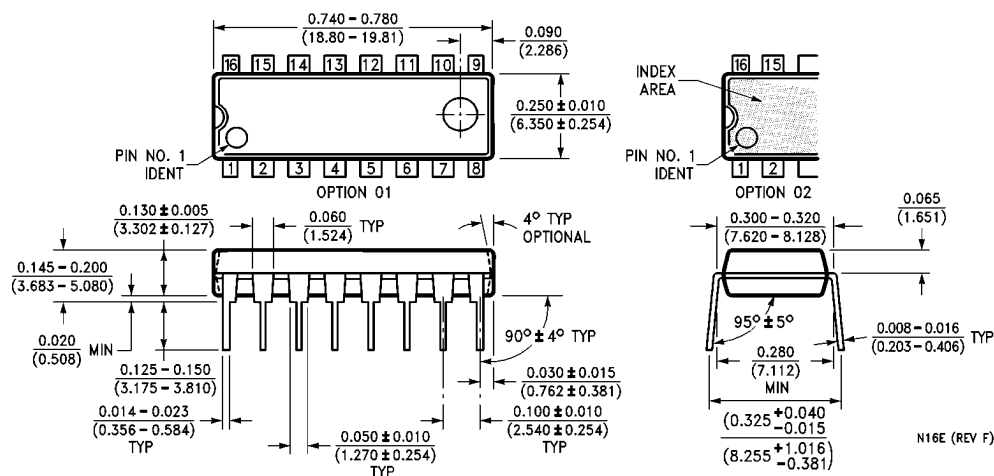


**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.