9-BIT HOLD REGISTER

FEATURES

- **700MHz min. operating frequency**
- **9 bits wide for byte-parity applications**
- **Asynchronous Master Reset**
- **Dual clocks**
- **ESD protection of 2000V**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Extended 100E VEE range of –4.2V to –5.46V**
- **Internal 75kΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E143**

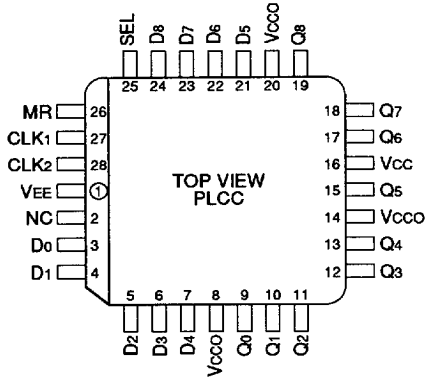
DESCRIPTION

The SY10E143 and SY100E143 are high-speed 9-bit hold registers designed for use in new, high-performance ECL systems. The E143 can hold current data or load new data. The nine inputs, D_0-D_8, accept parallel input data.

The SEL (Select) control pin serves to determine the mode of operation; either HOLD or LOAD. The input data has to meet the set-up time before being clocked into the nine input registers on the rising edge of CLK_1 or CLK_2. The MR (Master Reset) control signal asynchronously resets all nine registers to a logic LOW when a logic HIGH is applied to MR.

The E143 is designed for applications requiring high-speed registers, pipeline registers, synchronous operation, and is also suitable for byte-wide parity.

PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0-D_8	Parallel Data Inputs
SEL	Mode Select Input
CLK_1, CLK_2	Clock Inputs
MR	Master Reset
Q_0-Q_8	Data Outputs
NC	No Connection

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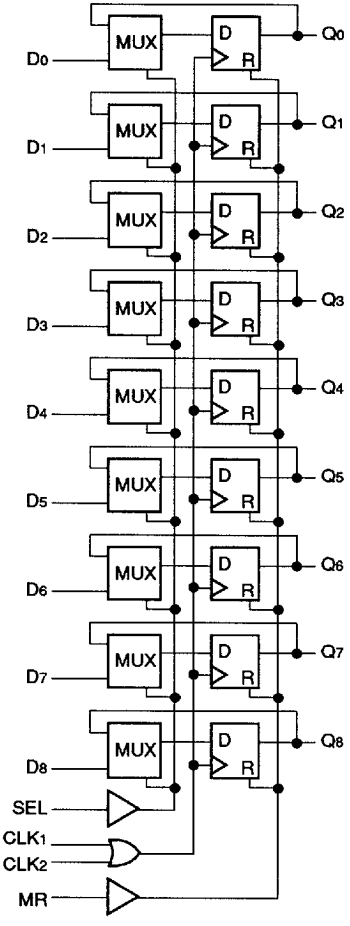
BLOCK DIAGRAM



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TRUTH TABLE

SEL	MODE
L	LOAD
H	HOLD

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	120	145	—	120	145	—	120	145		
	100E	—	120	145	—	120	145	—	138	165		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Toggle Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK	600	800	1000	600	800	1000	600	800	1000		
	MR	600	800	1000	600	800	1000	600	800	1000		
t_s	Set-up Time										ps	—
	D	50	–100	—	50	–100	—	50	–100	—		
	SEL	300	150	—	300	150	—	300	150	—		
t_h	Hold Time										ps	—
	D	300	100	—	300	100	—	300	100	—		
	SEL	75	–150	—	75	–150	—	75	–150	—		
t_{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{SKEW}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E143JC	J28-1	Commercial
SY100E143JC	J28-1	Commercial

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