SiW3000

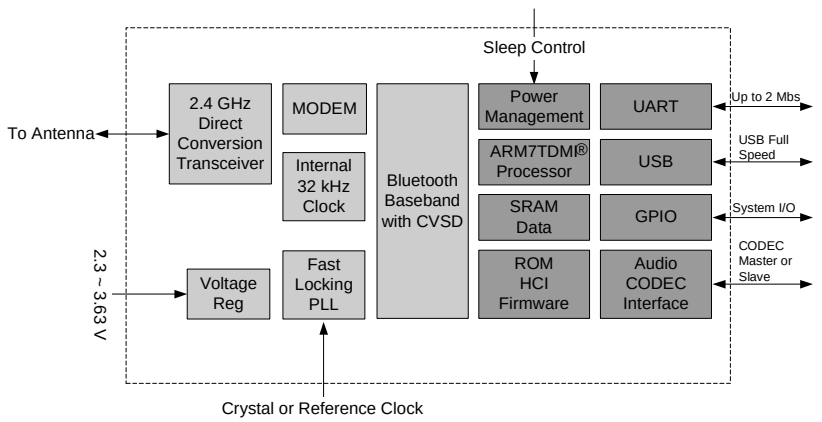
ULTIMATEBLUE™ SOC

Features

- Single-chip IC with 2.4 GHz transceiver, baseband processor, and on-chip protocol stack for Bluetooth® wireless technology
- Compliant with Bluetooth specification 1.2 features.
- Low cost 0.18 µm CMOS process technology.
- 1.8 V analog and digital core voltages; 1.62 V to 3.63 V external I/O interface voltage.
- Typical -85 dBm receiver sensitivity, +2 dBm transmitter power for up to 100 meters nominal range.
- On-chip VCO and PLL support multiple GSM/GPRS and CDMA cellular reference clock frequencies.
- Hardware AGC dynamically adjusts receiver performance in changing environments.
- Integrated 32-bit ARMTDMI® processor for extended features.
- Full piconet connectivity with support for up to 7 active and 8 parked slaves.
- Scatternet compatible with Microsoft® HID devices.
- Supports three SCO voice channels.
- Channel Quality Driven Data Rate (CQDDR) controls multi-slot packets to minimize packet overhead and maximize data throughput.
- Option for Bluetooth + Wi-Fi coexistence.

Applications

- Mobile phones.
- Notebook and desktop PCs.
- Cordless headsets.
- Personal digital assistants (PDAs).
- Computer accessories, peripherals, and wireless printers/ keyboards/mice).



Block Diagram

Product Description

The SiW3000 UltimateBlue™ SoC is a recent innovation for Bluetooth® wireless technology. It combines the industry's best performing and most highly integrated radio design with an ARMTDMI® processor using CMOS technology. The SiW3000 uses direct conversion (zero-IF) architecture. This allows digital filtering for excellent interference rejection as compared to low IF solutions and also results in fewer spurious responses.

The lower-layer protocol stack software is integrated into the on-chip ROM. Optional external Flash memory is also supported. The SiW3000 is compliant with Bluetooth specification 1.2 features.

The device is available in multiple packages and bare die form with a guaranteed operating temperature range from -40°C to +85°C.

Optimum Technology Matching® Applied

☐ Si BJT	☐ GaAs HBT	☐ GaAs MESFET
☐ Si Bi-CMOS	☐ SiGe HBT	☑ Si CMOS
☐ GaInP/HBT	☐ GaN HEMT	☐ SiGe Bi-CMOS

Ordering Information

SiW3000	UltimateBlue™ SoC

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60 0049 R01Erf SiW3000 SoC DS
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Radio Features

- Direct-conversion architecture with no external IF filter or VCO resonator components.
- Single ended RF I/O reduces system bill of materials (BOM) costs by eliminating the need to use external balun and switch circuits.
- On-chip VCO and PLL support multiple GSM, CDMA, GPRS standard reference clock frequencies.
- Low out-of-band spurious emission transmitter prevents blocking of sensitive mobile phone RF circuits.
- No tuning during production.
- Internal temperature compensation circuit stabilizes performance across wide operating temperature.
- Fast settling synthesizer reduces power consumption.
- Up to 100 meter operating range in standard configuration without using an external PA.

Baseband Features

- ARM7TDMI processor core running at 16 MHz.
- Digital GFSK modem for maximum performance and lower packet error rate.
- On-chip CVSD conversion with hardware based gain adjustments to enhance audio quality.
- Sleep control interface for low power operation modes.
- Software execution from ROM or external FLASH memory.

Standard Protocol Stack Features

- Full piconet connectivity with support for up to 7 active and 8 parked slaves.
- Able to establish up to 3 SCO connections.
- Scatternet capable and compatible with Microsoft HID devices.
- Standard Bluetooth test modes.
- Low power connection states supported with hold, sniff, and park modes.

Additional Protocol Stack Features

- Channel Quality Driven Data Rate (CQDDR) optimizes data transfer rate in noisy or weak signal environments
- Audio (SCO) routing over HCI interface for VOIP applications.
- Support for Bluetooth + Wi-Fi coexistence technology.
- Verified compatibility with multiple upper-layer stack vendors.
- Extensive vendor specific HCI commands enables hardware specific controls.
- Optional upper-layer stack and profiles can be licensed and integrated into the IC.

Bluetooth 1.2 Features

- Adaptive frequency hopping (AFH).
- Faster connections.
- LMP improvements.

External System Interfaces

Host HCI Transport (H:2 USB)

The USB device interface provides a physical transport between the SiW3000 and the host for the transfer of Bluetooth control signals and data. This transport layer is fully compliant with Section H:2 of the Bluetooth specification with all end points supported. The SiW3000 USB interface encompasses three I/O signals: USB_DPLS, USB_DMNS, and USB_DPLS_PULLUP. If the USB transport is not used, the USB_DPLS and USB_DMNS pins should be grounded to reduce current consumption.

Host HCI Transport (H:4 UART)

The high speed UART interface provides the physical transport between the SiW3000 and the application host for the transfer of Bluetooth control signals and data compliant to Section H:4 of the Bluetooth specification. The table below shows the supported baud rates. The default baud rate is 115,200, but can be configured depending on the application.

SiW3000 HCI UART Parameters	Required Host Setting
Number of data bits	8
Parity bit	No parity
Stop bit	1 stop bit
Flow control	RTS/CTS
Host flow-off response requirement from the SiW3000	8 bytes
SiW3000 IC flow-off response requirement from host	2 bytes
Supported baud rates	9.6k, 19.2k, 38.4k, 57.6k, 115.2k[a], 230.4k, 460.8k, 500k, 921.6k, 1M, 1.5M, 2M

a.Default baud rate.

Host HCI Transport (H:5 3-Wire UART)

To reduce the number of signals and increase reliability of the HCI UART interface, a 3-wire UART using either the Bluetooth H:5 or BCSP protocol is supported. The selection between H:4, H:5, and BCSP is done automatically by the SiW3000, or can be set in NVM.

SiW3000 HCI 3-Wire UART Parameters	Required Host Setting
Number of data bits	8
Parity bit	Even
Stop bit	1 stop bit
Error detection	Slip and checksum
Sleep modes	Shallow and deep

Audio CODEC Interface

The SiW3000 supports direct interface to an external audio CODEC or PCM host device. The interface is easily configured to support:

- Standard 64-kHz PCM clock rate.
- Up to 2-MHz clock rates with support for multi-slot handshakes and synchronization.
- Either master or slave (Motorola SSI) mode.

Configuration of the CODEC interface is done by the firmware during boot-up by reading non-volatile memory (NVM) parameters. The following are examples of supported CODEC modes:

- Generic 64-kHz audio CODEC (e.g., OKI MSM-7702).
- Motorola MC145481 or similar CODEC as master.
- QUALCOMM MSM chip set audio port.
- GSM/GPRS baseband IC audio ports.

Programmable I/O (PIO)

Up to twenty-nine (29) programmable IO (PIO) ports are available for customer use in the SiW3000. Three of these PIOs are dedicated and the remaining PIOs are shared with other functions. Availability of PIOs will depend on system configuration. The table below identifies the all twenty-nine PIOs and their usage. The PIO ports can be set to input or output. Reading, writing, and controlling the PIO pins by the host application software can be done via vendor specific HCI commands.

PIO#	Shared I/O	Sampled at Reset
0	None	Yes
1	None	Yes
2	None	Yes
3	D[8]	No
4	D[4]	No
5	D[5]	No
6	D[6]	No
7	D[7]	No
8	PWR_REG_EN	No
9	D[15]	No
10	WE_N	No
11	A[16]	No
12	A[17]	No
13	A[11]	No
14	USB_DPLS_PULLUP	No

PIO#	Shared I/O	Sampled at Reset
15	PCM_OUT	No
16	PCM_IN	No
17	PCM_CLK	No
18	PCM_SYNC	No
19	EXT_WAKE	No
20	HOST_WAKEUP	No
21	UART_RXD	No
22	UART_TXD	No
23	UART_CTS	No
24	UART_RTS	No
25	A[18]	No
26	TX_RX_SWITCH	No
27	D[9]	No
28	D[10]	No

External Memory Interface

The UltimateBlue SiW3000 is a true single chip device and does not require additional memory for standard below HCI protocol functions. An external memory interface is available for adding optional memory. If external Flash memory will be used, the read access time of the device must be 100 ns or less.

The external memory interface permits connection to Flash and SRAM devices. The interface has an 18-bit address bus and a 16-bit data bus for a total addressable memory of 512 KB. In certain embedded applications, both SRAM and Flash can be installed by using the high order address bit as an alternate chip select.

Signal	Description
Address A[1] - A[18]	18-bit address bus
Data D[0] - D[15]	16-bit data bus
FCS_N	Chip select
OE_N	Output enable
WE_N	Write enable

External EEPROM Controller and Interface

This interface is intended for use with ROM-based solutions. The EEPROM is not required for configurations with external flash. The EEPROM is the non-volatile memory (NVM) in the system and contains the system configuration parameters such as the Bluetooth device address, the CODEC type, as well as other parameters. These default parameters are set at the factory, and some parameters will change depending on the system configuration. Optionally, the non-volatile memory parameters can be downloaded from the host processor at boot up eliminating the need for EEPROM. Please consult the application support team for details. The EEPROMs should have a serial I^2C interface with a minimum size of 2 Kbits and 16-byte page write buffer capabilities.

Power Management

The HOST_WAKEUP and EXT_WAKE signals are used for power management. HOST_WAKEUP is an output signal used to wake up the host. EXT_WAKE is an input signal used by the host to wake up the SiW3000 SoC from sleep mode. For more information on the usage of HOST_WAKE and EXT_WAKE, please refer to RFMD application note 62 0031.

General System Requirements

System Reference Clock

The SiW3000 chip can use either an external crystal or a reference clock as the system clock input. The supported frequencies are: 9.6 MHz, 12 MHz, 12.8 MHz, 13 MHz, 14.4 MHz, 15.36 MHz, 16 MHz, 16.8 MHz, 19.2 MHz, 19.68 MHz, 19.8 MHz, 26 MHz, 32 MHz, 38.4 MHz, and 48 MHz. The default reference frequency can be selected by setting the proper system configuration parameter in the non-volatile memory (NVM). If the USB HCI transport will be used, the reference clock must be 32 MHz.

The system reference crystal/clock must have accuracy of ±20 PPM or better to meet the specification of Bluetooth. To facilitate design and production, the SiW3000 processor incorporates internal crystal calibration circuits to allow factory calibration of initial crystal frequency accuracy.

Low Power Clock

For the Bluetooth low power clock, a 32.768-kHz crystal may be used to drive the SiW3000 oscillator circuit, or alternatively, a 32.768-kHz reference clock signal can be used instead of a crystal. If the lowest power consumption is not required during low-power modes such as sniff, hold, park, and idle modes, the 32.768-kHz crystal may be omitted in the design. If the 32.768-kHz clock source will be used, the clock source should be connected to the CLK32_IN pin and must meet the following requirements:

- For AC-coupled via 100 pF or greater (peak-to-peak voltage):
  400 mV_{P-P} < CLK32_IN < V_{DD_C}
- For DC-coupled:
  CLK32_IN minimum peak voltage < VIL
  CLK32_IN maximum peak voltage > VIH
  Where V_{IL} = 0.3 * V_{DD_C}
  Where V_{IH} = 0.7 * V_{DD_C}

For both cases, the signal is not to exceed:
-0.3 V < CLK32_IN < V_{DD_C} + 0.3 V

Also, the CLK32_OUT pin must be coupled to V_{DD_P} or GND through a 100 nF capacitor.

Power Supply Description

The SiW3000 operates at 1.8 V core voltage for internal analog and digital circuits. The chip has internal analog and digital voltage regulators simplifying power supply requirements to the chip. The internal voltage regulators can be supplied directly from a battery or from other system voltage sources. Optionally, the internal regulators can be by-passed if 1.8 V regulated source is available on the system.

Function	Internal Analog Regulator	Internal Digital Regulator
Regulator input pin	V_{BATT_ANA} = 2.3 to 3.63 V	V_{BATT_DIG} = 2.3 to 3.63 V
Regulator output pin	V_{CC_OUT} = 1.8 V	V_{DD_C} = 1.8 V

Internal Regulator Used

Function	Analog Core Circuits	Digital Core Circuits
Circuit voltage supply pin	V_{CC} = 1.8 V	V_{DD_C} = 1.8 V

Internal Regulator Bypassed

Note: Both regulators can be bypassed if external regulation is desired. When bypassing the analog regulator, the VBATT_ANA and VCC_OUT pins must be tied together and the external analog voltage (1.8 V) should be applied to the VBATT_ANA pin. When bypassing the digital regulator, the VBATT_DIG pin should be left unconnected and the external digital voltage (1.8 V) should be applied to VBB_OUT pin.

The power for the I/Os is taken from a separate source (V_{DD_P}). V_{DD_P} can range from 1.62 to 3.63 Volts to maintain compatibility with a wide range of peripheral devices. Please check the pin list for the exact pins that are powered from the V_{DD_P} source. Power for the USB circuits is taken from a separate source (V_{DD_USB}).

RF I/O Description

The SiW3000 employs single-ended RF input and output pins for reduced external components. In typical Class-2 (0 dBm nominal) applications, simple LC network matching circuits will be required to combine the two ports into a single antenna port and provide impedance matching. Please refer to the RF impedance table and the application circuits for values and matching circuit examples. The SiW3000 can be used to design Class-1 (+20 dBm) products with the addition of power amplifier circuits. Control signals are available to facilitate the design of the external PA circuit.

Reset

The SiW3000 can be reset by asserting the RESET_N signal to the chip (active low). Upon applying power, the RESET_N must be asserted until voltage supply and internal voltage regulators have stabilized. A simple RC circuit can be used to provide the power-on reset signal to the SiW3000.

On-Chip Memory

The SiW3000 integrates both SRAM and ROM. The ROM is pre-programmed with Bluetooth protocol stack software (HCI software) and boot code that executes automatically upon reset. The boot code serves to control the boot sequence as well as to direct the execution to the appropriate memory for continued operation.

Configuration Selection

HCI Transport Interface Selection

The HCI transport (USB or UART) is selected on power up by sampling PIO2. If UART is selected, the selection of the particular UART transport (H:4 or H:5) is performed automatically by the software.

Value (PIO 2)	Description
0	UART
1	USB

Reference Frequency Selection

The SiW3000 is designed to operate with multiple reference frequencies. During boot up the processor samples PIO pins to determine the default reference frequency. If the USB transport is selected, the default reference frequency will always be 32 MHz. If the UART transport is selected, the reference frequency setting will be set according to the following table:

PIO 1	USB_DPLS_PULLUP	Reference Frequency Selection
1	Don't Care	Reference frequency per NVM system configuration setting, or if NVM is not set, defaults to 32 MHz.
0	0	13 MHz
0	1	26 MHz

Application Software Memory Selection

The SiW3000 can support application (protocol stack) software execution from internal ROM and external FLASH memory. To run from internal ROM, D[9] and D[10] pins must be connected together as shown in the application circuit section of this document. To run from external FLASH memory the FLASH must be connected as shown in the application circuit diagram and contain valid application code. If an external memory does not have valid program data, the device enters a download mode in which a valid program may be loaded into the external memory through a sequence of commands over the HCI transport layer.

Pin Description

The following table provides detailed listings of pin descriptions arranged by functional groupings.

Name	Pad Type	Ball	Description
Radio (Power from VCC)			
RF_IN	Analog	A2	RF signal input into the receiver.
RF_OUT	Analog	A4	RF signal output from the transmitter.
VTUNE	Analog	A6	Pin for reference PLL loop filter, only used if reference frequency is not integer multiples of 4 MHz.
CHG_PUMP	Analog	F1	Pin for RF loop filter.
XTAL_N	Analog	A7	System clock crystal negative input. If a reference clock is used, this pin should be left unconnected.
XTAL_P/CLK	Analog	B7	System clock crystal positive input or reference clock input.
IDAC	Analog	B1	Power control to external power amplifier. This output provides a variable current source that can be used to control the external power amp. Leave unconnected if not used.
VREFP_CAP	Analog	C1	Decoupling capacitor for internal A/D converter voltage reference.
VREFN_CAP	Analog	C2	Decoupling capacitor for internal A/D converter voltage reference.
Low Power Oscillator and Reset (Power from VDD_P)			
CLK32K_IN	Analog	K10	For crystal or external clock input (32.768 kHz).
CLK32K_OUT	Analog	L11	Drive for crystal.
RESET_N	Analog	C6	System level reset (active low).
Power Control Interface (Power from VDD_P)			
PWR_REG_EN/PIO[8]	CMOS bi-directional	G1	Enable for an external voltage regulator. Programmable active high or active low. Also used as PIO[8], which is the default mode until the appropriate configuration bit is set. Tie to ground if not used.
TX_RX_SWITCH	CMOS output	J9	Output signal used to indicate the current state of the radio. This could be used as a direction control for an external power amplifier.The polarity is programmable with the default set as: Low = Transmit mode High = Receive mode

Table 1. SiW3000 Pin List

Name	Pad Type	Ball	Description
Programmable I/O (Power from VDD_P)			
PIO[0]	CMOS bi-directional	K5	Programmable input/output. Needs to be low until internal reset goes high or tie to ground if not used.
PIO[1]	CMOS bi-directional	B8	Programmable input/output. Sampled following reset for frequency selection: If UART transport is selected and PIO[1] = 0, frequency is selected by the state of USB_DPLS_PULLUP pin. If UART transport is selected and PIO[1] = 1, frequency is selected by NVM parameter. Default for proper UART operation will be configured as 32 MHz. If USB transport is selected, PIO[1] is ignored and the frequency will be configured as 32 MHz.
PIO[2]	CMOS bi-directional	J10	Programmable input/output. Sampled following reset for transport selection: PIO[2] = 0, selects UART transport PIO[2] = 1, selects USB transport
PCM Interface (Power from VDD_P)			
PCM_IN	CMOS output	E10	PCM data to the PCM CODEC.
PCM_OUT	CMOS input	F10	PCM data from the remote device. Normally an input.
PCM_CLK	CMOS bi-directional	G10	PCM synchronous data clock to the remote device. Normally an output. Input for Motorola SSI slave mode.
PCM_SYNC	CMOS bi-directional	H10	PCM synchronization data strobe to the remote device. Normally an output. Input for Motorola SSI slave mode.
UART Interface (Power from VDD_P)			
UART_RXD	CMOS input	K7	UART receive data.
UART_TXD	CMOS output	K3	UART transmit data.
UART_CTS	CMOS input	K6	UART flow control clear to send.
UART_RTS	CMOS output	G9	UART flow control ready to send.
EXT_WAKE	CMOS input	F3	Wake up signal from host.
HOST_WAKEUP	CMOS output	G2	Wake up signal to host.
USB Interface (Power from VDD_USB)			
USB_DPLS	Analog	K9	USB differential pair positive signal.
USB_DMNS	Analog	K8	USB differential pair negative signal.
USB_DPLS_ PULLUP	CMOS bi-directional	J8	Output signal for controlling the on/off of the pull-up of the USB_DPLS line. For UART transport, this pin is sampled following reset for frequency selection if PIO[1] = 0: USB_DPLS_ PULLUP = 0, selects 13 MHz USB_DPLS_ PULLUP = 1, selects 26 MHz

Table 1. SiW3000 Pin List (Continued)

Name	Pad Type	Ball	Description
External Memory Interface (power from VDD_P)			
A[18] A[17]/EEPROM_SCL A[16]/EEPROM_SDA A[15] A[14] A[13] A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1]	CMOS output	L1 G3 H1 A8 H2 C9 H3 J1 K4 J7 L4 A11 L7 F9 E11 E9 D11 D9	Address lines. Note: A[17] and A[16] can be used to support an optional external serial EEPROM when using the internal ROM in place of the external Flash memory.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8]/PIO[3] D[7]/PIO[7] D[6]/PIO[6] D[5]/PIO[5] D[4]/PIO[4] D[3] D[2] D[1] D[0]	CMOS bi-directional with internal pull-down	B11 C10 C11 B10 G11 H11 H9 J2 J11 D10 L3 L2 J4 J3 K2 K1	Data lines. **Note**: D[4] through D[8] can be used as programmable I/O when using the internal ROM in place of the external Flash memory. **Note**: Connect D[9] to D[10] to use internal ROM.
OE_N	CMOS output	A10	Output enable for external memory (active low).
WE_N/EEPROM_WP	CMOS output	K11	Write enable for external memory (active low). Note: Can be used to support an optional external serial EEPROM when using the internal ROM in place of external Flash memory.
FCS_N	CMOS output	B9	Chip select for external memory (active low).
Power and Ground			
VBATT_ANA	Power	D3	Positive supply to internal analog voltage regulator.
VBATT_DIG	Power	L8	Positive supply to internal digital voltage regulator.
VCC_OUT	Power	D1	Regulated output from internal analog voltage regulator.
VDD_P	Power	F11 L5	Positive supply for digital input/output ports including peripheral interface, external memory interface, and UART interface.
VDD_USB	Power	L10	Positive supply for USB Interface.
VDD_C	Power	A9 L6	Positive supply for digital circuitry or output of internal digital voltage.
VCC	Power	A1 B6 C4 C5 E1 E3	Positive supply for RF and analog circuitry.
VSS_P	GND	C7 J5	Ground connections for digital input/output ports including peripheral interface, external memory interface, and UART Interface.
VSS_C	GND	C8 J6	Ground connections for internal digital circuitry.
VSS_USB	GND	L9	Ground connections for USB Interface.

Table 1. SiW3000 Pin List (Continued)

Name	Pad Type	Ball	Description
GND	GND	A3 A5 B2 B3 B4 B5 C3 D2 E2 F2	Ground connections for RF and analog circuitry.

Table 1. SiW3000 Pin List (Continued)

System Specifications

Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
V_{CC}	Analog circuit supply voltage	-0.3	3.63	V
V_{DD_IO}	I/O supply voltage	-0.3	3.63	V
V_{BATT_ANA}	Analog regulator supply voltage	-0.3	3.63	V
V_{BATT_DIG}	Digital regulator supply voltage	-0.3	3.63	V
T_{ST}	Storage temperature	-55	+125	°C
RF_{MAX}	Maximum RF input level	–	+5	dBm

Absolute maximum ratings indicate limits beyond which the useful life of the device may be impaired or damage may occur.

Recommended Operating Conditions

Parameter	Description	Min	Max	Unit
T_{OP}	Operating temperature (industrial grade)	-40	+85	°C
T_{EOP}	Extended operating temperature	-40	+105	°C
V_{BATT_ANA}	Unregulated supply voltage into internal analog regulator	2.3	3.63	V
V_{BATT_DIG}	Unregulated supply voltage into internal digital regulator	2.3	3.63	V
V_{CC}	Regulated supply voltage directly into analog circuits	1.71	1.89	V
V_{DD_C}	Regulated supply voltage directly into digital circuits	1.62	2.16	V
V_{DD_P}	Digital interface I/O supply voltage	1.62	3.63	V
V_{DD_USB}	Regulated supply voltage for USB Interface to meet USB specification requirements	3.1	3.63	V

ESD Rating

Symbol	Description	Rating
ESD	ESD protection - all pins	2000 V

Note: This device is a high performance RF integrated circuit with an ESD rating of 2,000 volts (HBM conditions per Mil-Std-883, Method 3015). Handling and assembly of this device should only be done using appropriate ESD controlled processes.

Electrical Characteristics

DC Specification (T_{OP}=+25 °C, V_{DD_P}=3.0 V)

Symbol	Description	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	GND-0.1	–	$0.3 \cdot V_{DD\_P}$	V
V_{IH}	Input high voltage	$0.7 \cdot V_{DD\_P}$	–	V_{DD_P}	V
V_{OL}	Output low voltage	GND	–	$0.2 \cdot V_{DD\_P}$	V
V_{OH}	Output high voltage	$0.8 \cdot V_{DD\_P}$	–	V_{DD_P}	V
I_{OH}	Output high current	–	1	–	mA
	Output high current (ball J8)	–	4	–	mA
I_{OL}	Output low current	–	1	–	mA
	Output low current (ball J8)	–	4	–	mA
I_{ILI}	Input leakage current	–	1	–	µA

AC Characteristics (T_{OP}= +25 °C, V_{DD_P}=3.0 V, C_{LOAD}=15 pF)

Symbol	Description	Max.	Unit
t_r	Rise time	30	ns
t_f	Fall time	24	ns

Current Consumption (T_{OP}= +25 ˚C, V_{BATT}=3.0 V using internal regulators)

Operating Mode	Average	Unit
Standby	25	µA
Parked slave, 1.28 sec. interval	160	µA
Page/Inquiry scan, 1.28 sec. interval	1.5	mA
ACL connection, sniff mode, 100 ms interval	1.2	mA
ACL data transfer 720 kbps, DH5 continuous packets	60	mA
SCO connection, HV1 packets	60	mA
SCO connection, HV3 packets	32	mA

Digital Regulator Specification (T_{OP} = 25 ˚C)

Parameter	Description	Min	Typ	Max	Unit
Output voltage	(I_{OUT} = 10 mA)	1.62	1.85	2.16	V
Line regulation	(I_{OUT} = 0 mA, V_{BATT_DIG} = 2.3 V to 3.63 V)	–	8.0	–	mV
Load regulation	(I_{OUT} = 3 mA to 80 mA)	–	9.0	–	mV
Dropout voltage	(I_{OUT} = 10 mA)	–	–	250	mV
Output maximum current	–	–	–	80	mA
Quiescent current	–	–	10	–	µA
Ripple rejection	f_{RIPPLE} = 400 Hz	–	40	–	dB

Radio Specification

Parameter	Description	Min	Typ	Max	Unit
VCO Operating Range	Frequency	2402	–	2480	MHz
PLL lock time	–	–	55	100	µs

RF Impedances

Parameter[a]	Description	Min	Typ	Max	Unit
RF impedance	TX on	–	769//1.1	–	Ω/pF
	TX off	–	26//2.4	–	Ω/pF
	RX on	–	142//1.8	–	Ω/pF
	RX off	–	45.7//0	–	Ω/pF

a.The impedance values are for typical samples in 96-pin VFBGA package.

Receiver Specification (V_{BATT} = 3.3 V, V_{CC}=int. analog reg. output, nominal Bluetooth test conditions)

Parameter	Description	Min	Typ	Max	Unit
Receiver sensitivity	BER < 0.1%	–	-85	-80	dBm
Maximum usable signal	BER < 0.1%	–	0	–	dBm
C/I co-channel (0.1% BER)	Co-channel selectivity	–	8	11	dB
C/I 1 MHz (0.1% BER)	Adjacent channel selectivity	–	-4	0	dB
C/I 2 MHz (0.1% BER)	2nd adjacent channel selectivity	–	-38	-35	dB
C/I ≥ 3 MHz (0.1% BER)	3rd adjacent channel selectivity	–	-43	-40	dB
Out-of-band blocking	30 MHz - 2000 MHz	-10	–	–	dBm
	2000 MHz - 2399 MHz	-27	–	–	dBm
	2498 MHz - 3000 MHz	-27	–	–	dBm
	3000 MHz - 12.75 GHz	-10	–	–	dBm
Intermodulation	Max interferer level to maintain 0.1% BER, interference signals at 3 and 6 MHz offset.	-39	-36	–	dBm
Receiver spurious emission	30 MHz to 1 GHz	–	–	-57	dBm
	1 GHz to 12.75 GHz	–	–	-47	dBm

Note: Nominal and extreme Bluetooth test conditions as defined by the Bluetooth Test and Interoperability Working Group published RF Test Specification 1.1.

Transmitter Specification (V_{BATT} = 3.3 V, V_{CC} = int. analog reg. output, nom. Bluetooth test conditions)

Parameter	Description	Min	Typ	Max	Units
Output RF transmit power	At maximum power output level	-2	+2	+6	dBm
Modulation index	–	0.28	0.306	0.35	–
Initial carrier frequency accuracy	–	-75	–	+75	kHz
Carrier frequency drift	One slot packet	-25	–	+25	kHz
	Two slot packet	-40	–	+40	kHz
	Five slot packet	-40	–	+40	kHz
	Max drift rate	–	–	400	Hz/µs
20 dB occupied bandwidth	Bluetooth specification	–	–	1000	kHz
In-band spurious emission	2 MHz offset	–	-74	-55	dBm
	>3 MHz offset	–	-74	-55	dBm
Out-of-band spurious emission	30 MHz to 1 GHz, operating mode	–	-70	-55	dBm
	1 GHz to 12.75 GHz, operating mode[a]	–	-70	-50	dBm
	1.8 GHz to 1.9 GHz	–	–	-62	dBm
	5.15 GHz to 5.3 GHz	–	–	-47	dBm

a.Except transmit harmonics.

System Requirements

Analog Voltage Supply Requirements

The SiW3000 is designed for use with integrated low noise analog voltage regulators and is recommended for all applications. If necessary, the internal analog regulator can be bypassed. In situations where bypassing the internal analog regulator is required, the supply voltage to the analog circuit must satisfy the following requirements to preserve the RF performance characteristics.

Parameter	Description	Min	Max	Unit
VCC	Analog supply voltage to all VCC input pins	1.71	1.89	V
Minimum load current	External regulator current	80	–	mA
Minimum ripple rejection	at 400Hz	40	–	dB
Output noise	Integrated 10 Hz to 80 kHz noise	–	22	mV RMS

External Reference Requirements

It is possible to provide a number of reference frequencies that are typical on most cellular phones directly into ball B7 (XTAL_P/CLK) of the device. The following reference frequencies (in MHz) can be used:

3.84, 9.6, 12, 12.8, 13, 14.4, 15.36, 16, 16.8, 19.2, 19.68, 19.8, 26, 32, 38.4, and 48 MHz. For other frequencies, please contact RFMD.

Parameter	Description	Min	Max	Units
Phase noise	100 Hz offset	–	-100	dBc/Hz
	1 kHz offset	–	-120	dBc/Hz
	10 kHz offset	–	-140	dBc/Hz
Drive level	AC amplitude	0.5	V_{CC}	V_{P-P}
	DC level[a]	0.3	V_{CC}	V

a.If DC-coupled, the external reference signal voltage must stay within this range at all times.

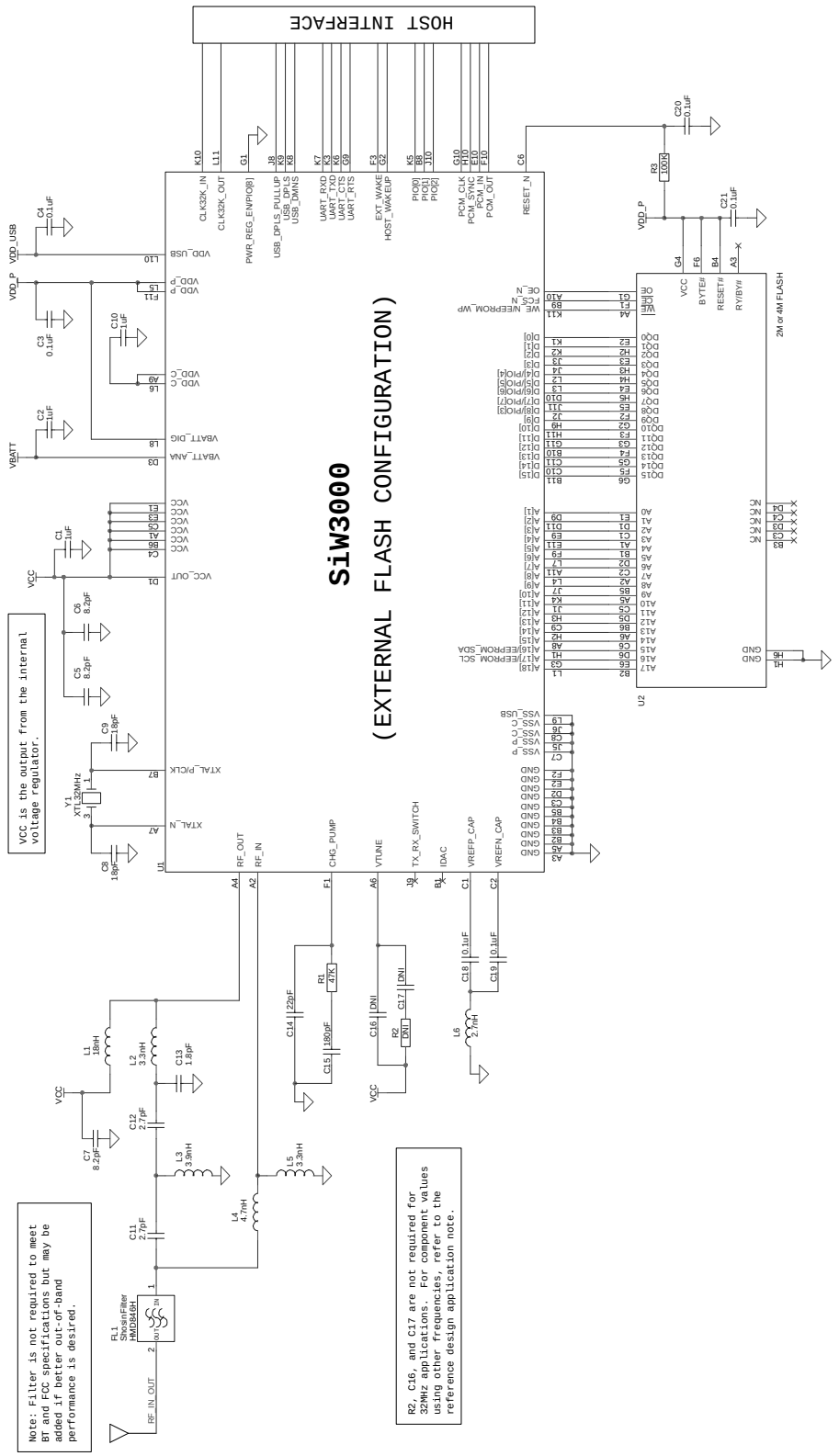
Reference Crystal Requirements

Many reference frequencies are supported by the device. If a crystal is used as the reference frequency source, the typical required parameters are listed below:

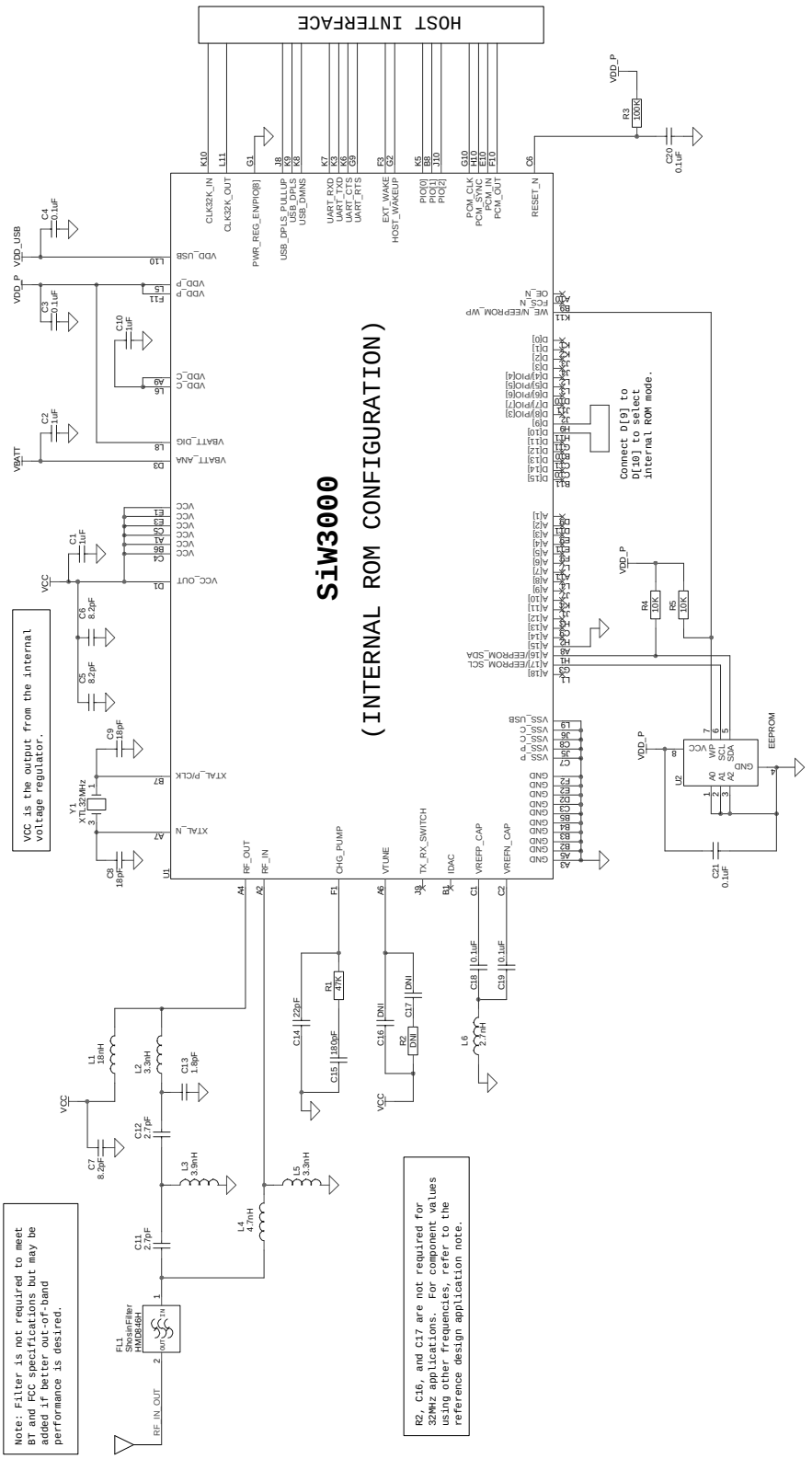
Parameter	Description	Min	Typ	Max	Unit
Drive level	–	–	–	0.3	mW
ESR	Effective serial resistance[a]	–	–	150	W
C_O	Holder capacitance[b]	–	3	5	pF
C_L	Load capacitance[b]	–	12	18	pF
C_M	Motional capacitance	–	6	–	fF

a.For 32-MHz crystal.
b.The actual values for C_O and C_L are dependent on the crystal manufacturer and can be compensated for by an internal crystal calibration capability.

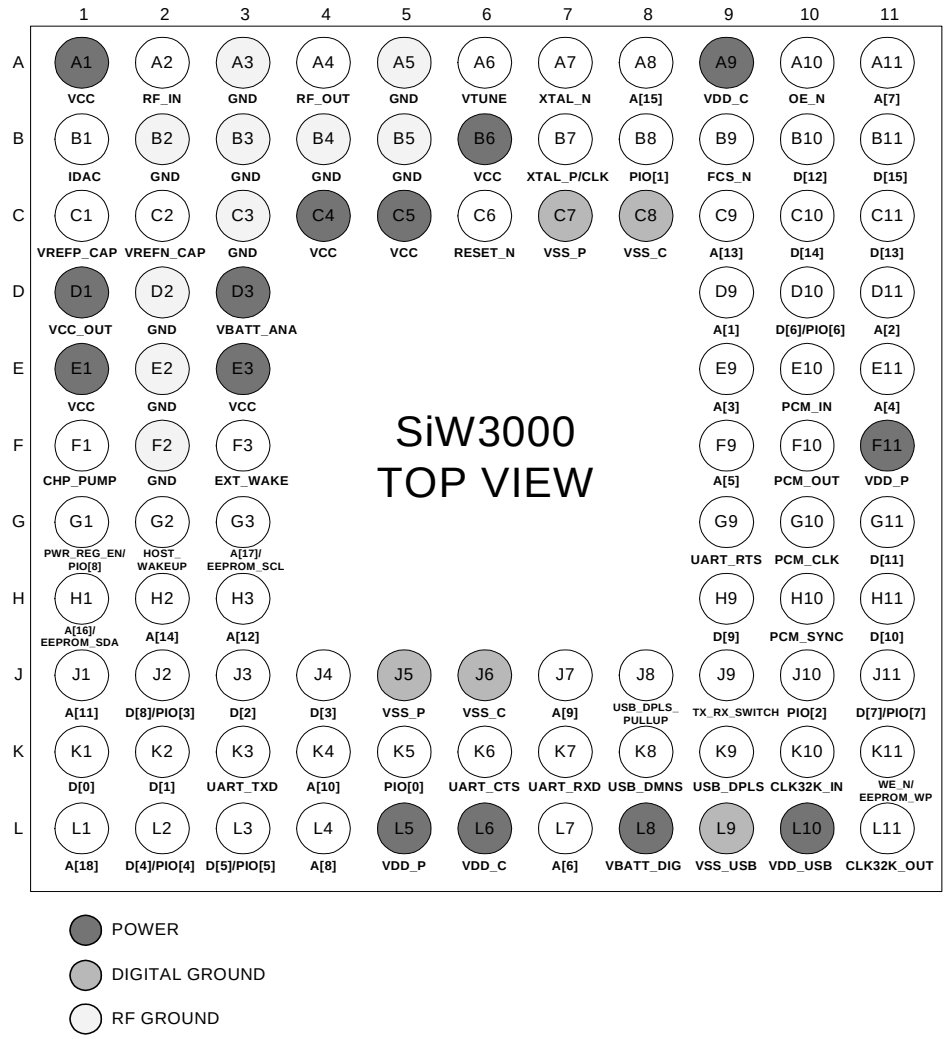
Application Circuit for External Flash-based Products



Application Circuit for Internal ROM-based Products



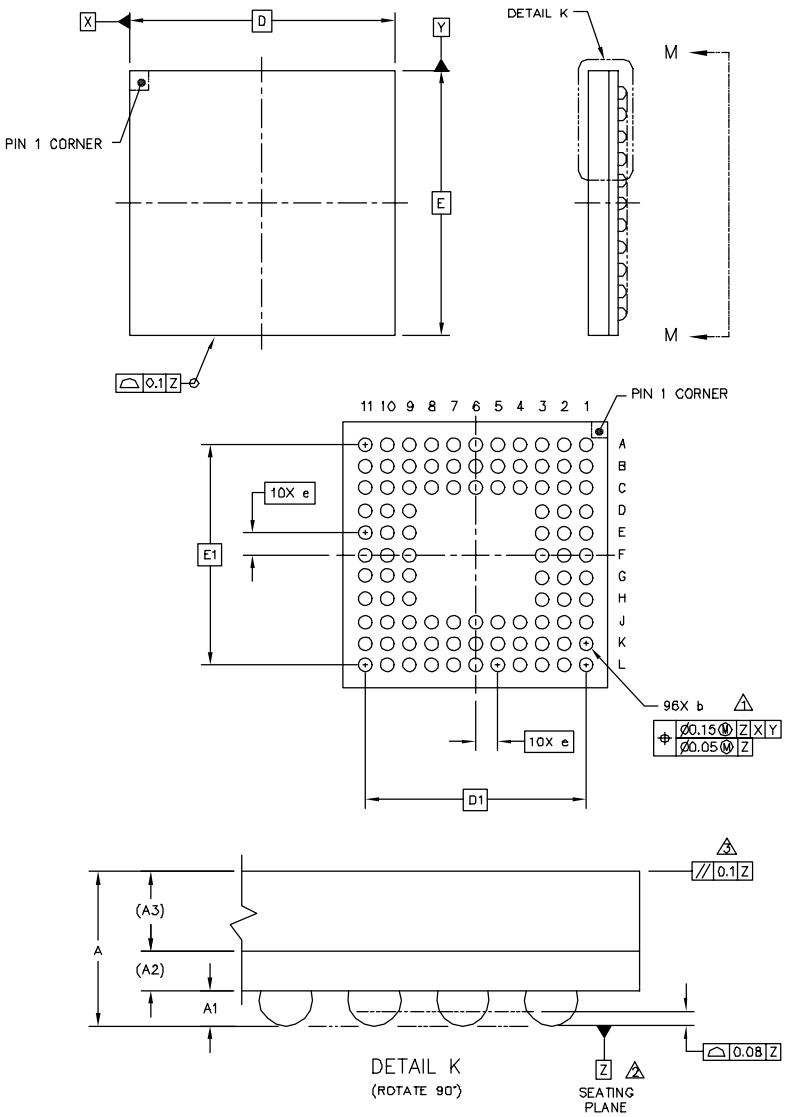
I/O Configuration (Top View)



Packaging and Product Marking

Package Drawing

96-Pin, 6 mm x 6 mm, VFBGA Drawing and Dimensions



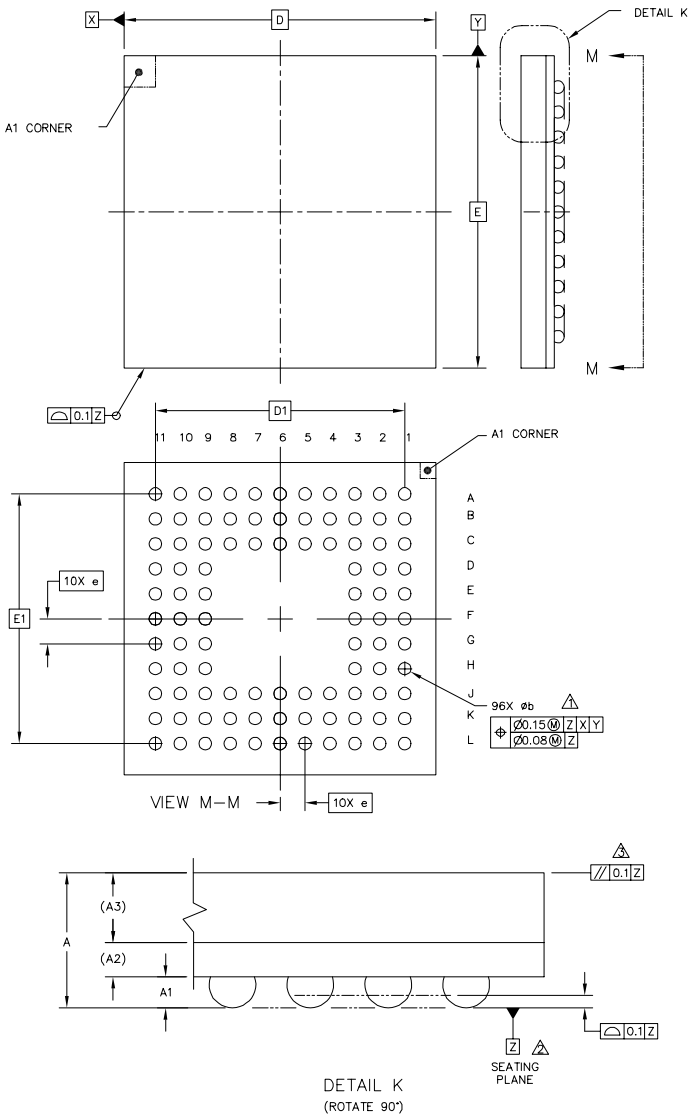
Symbol	Min	Max
A	0.8	1.0
A1	0.2	0.3
A2	0.22 REF	
A3	0.45 REF	
b	0.25	0.35
D	6 BSC	
E	6 BSC	
e	0.5 BSC	
D1	5 BSC	
E1	5 BSC	

Notes:

1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
2. Datum Z is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of mark on top surface of package.
4. All dimensions are in millimeters.

Package Drawing

96-Pin, 10 mm x 10 mm, LFBGA Drawing and Dimensions

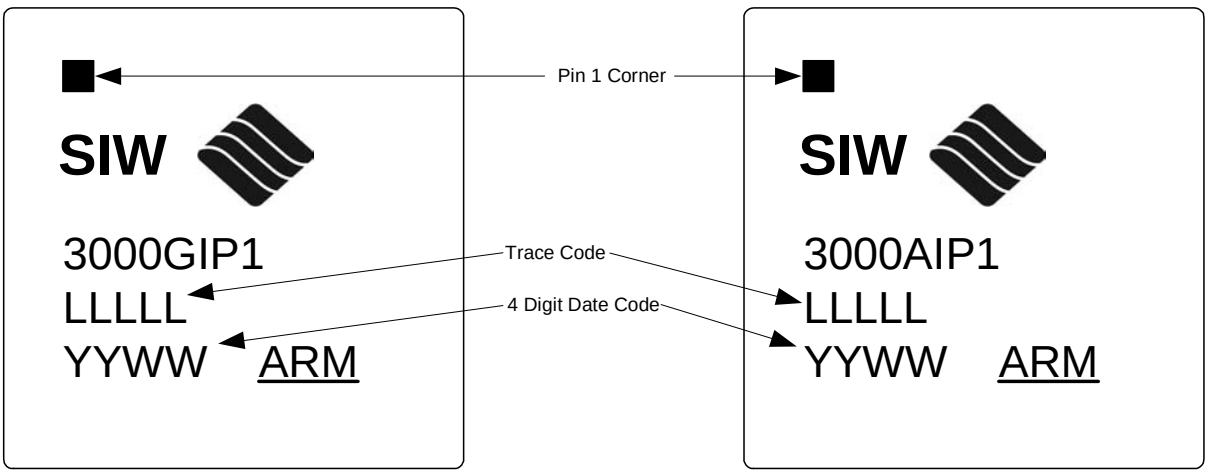


Symbol	Min	Max
A	-	1.4
A1	0.27	0.37
A2	0.26 REF	
A3	0.8 REF	
b	0.35	0.45
D	10 BSC	
E	10 BSC	
e	0.8 BSC	
D1	8 BSC	
E1	8 BSC	

Notes:

1. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
2. Datum Z is defined by the spherical crowns of the solder balls.
3. Parallelism measurement shall exclude any effect of mark on top surface of package.
4. All dimensions are in millimeters.
5. Dimensions and tolerances: ASME Y14.5M.
6. Reference document: JEDEC-MO-210.

Product Marking

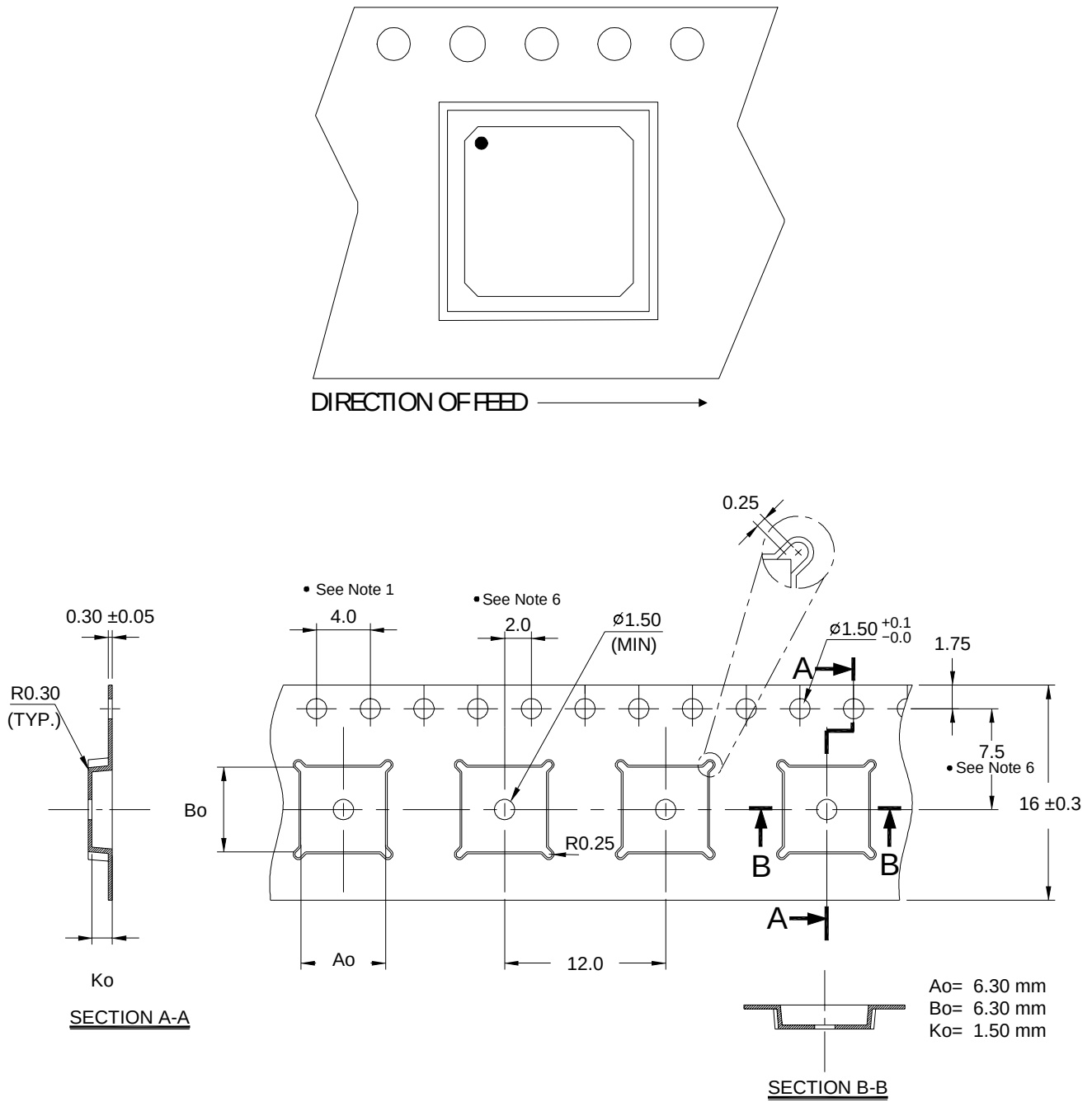


6-by-6-mm VFBGA **Note**: Drawing not to scale. 10-by-10-mm LFBGA

Tape and Reel Specification

Carrier Tape:	ADV ML0707-A
Reel Type:	Klik Reel (16 mm) 13" dia.
Peel Test:	20–80 grams
Cover Tape:	RS Standard (anti-static)
Leader:	500 mm (minimum 400 mm)
Trailer:	250 mm (minimum 160 mm)
Peel Speed:	300 mm/minute

Tape Detail (6 mm x 6 mm VFBGA)

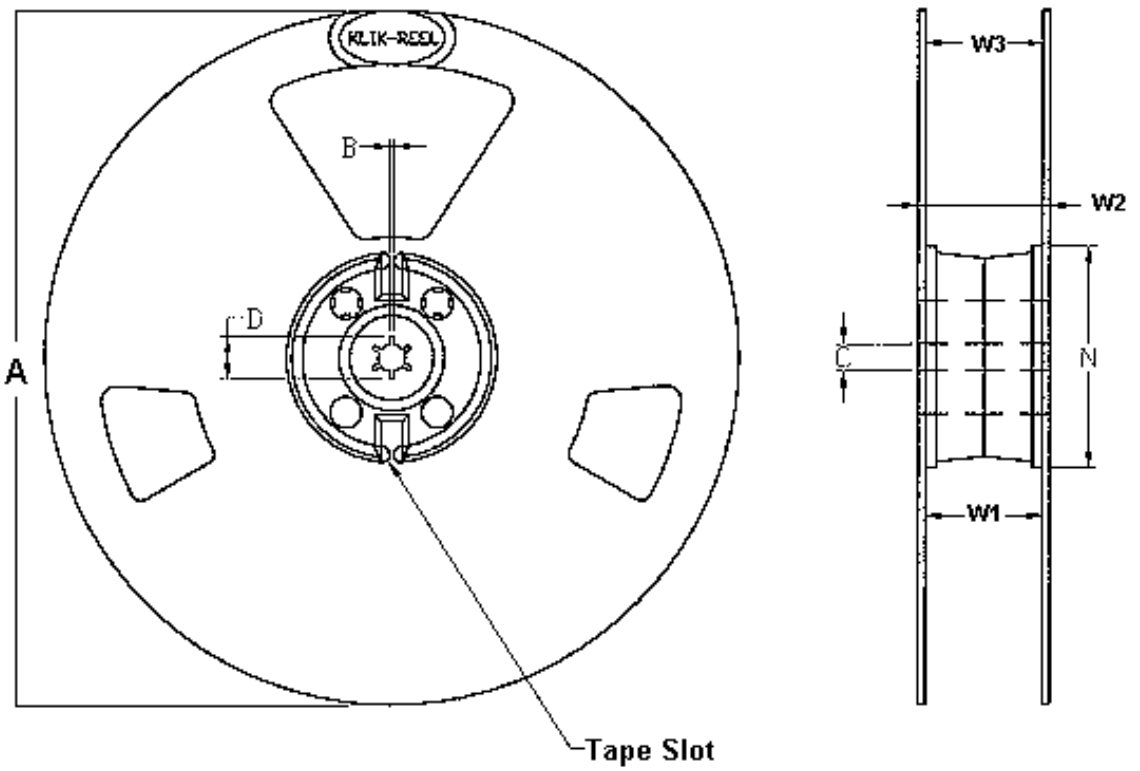


Note:

1. Tolerances ±0.10 unless otherwise specified.
2. 10 sprocket hole pitch cumulative tolerance ±0.2
3. Camber not to exceed 1mm in 100 mm.
4. Material: Black Advantek Polystyrene.
5. Ao and Bo measured on a plane 0.3 mm above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
8. All dimensions in millimeters.

Reel Dimensions: Klik Reel

Tape Width	A	B(min)	C	D (min)	N (min)	W1	W2 (max)	W3 (min)	W3 (max)
16	330	1.50	13.00+0.5	20.20	100	16.4+2.0 -0.00	22.40	15.90	19.40



Note: All dimensions in millimeters (mm) unless otherwise stated.

Ordering Information

Part Number	Operational Temperature Range[1]	Package	Ordering Quantity
SiW3000GIP1	Industrial	96-pin VFBGA 6-by-6-mm	25 pcs on cut tape
SIW3000GIP1SB	Industrial	96-pin VFBGA 6-by-6-mm	5 pcs on cut tape
SIW3000GIP1SR	Industrial	96-pin VFBGA 6-by-6-mm	100 pcs on short reel
SiW3000GIP1-T13	Industrial	96-pin VFBGA 6-by-6-mm	2500 on 13” reel
SiW3000GIG1	Industrial	96-pin VFBGA 6-by-6-mm Green	25 pcs on cut tape
SIW3000GIG1SB	Industrial	96-pin VFBGA 6-by-6-mm Green	5 pcs on cut tape
SIW3000GIG1SR	Industrial	96-pin VFBGA 6-by-6-mm Green	100 pcs on short reel
SiW3000GIG1-T13	Industrial	96-pin VFBGA 6-by-6-mm Green	2500 on 13” reel
SiW3000AIP1	Industrial	96-pin LFBGA 10-by-10-mm	25 pcs on cut tape
SIW3000AIP1SB	Industrial	96-pin LFBGA 10-by-10-mm	5 pcs on cut tape
SIW3000AIP1SR	Industrial	96-pin LFBGA 10-by-10-mm	100 pcs on short reel
SiW3000AIP1-T13	Industrial	96-pin LFBGA 10-by-10-mm	1500 on 13” reel

[1] Industrial temperature range: -40°C to +85°C