Not Recommended for New Designs

This product was manufactured for Maxim by an outside wafer foundry using a process that is no longer available. It is not recommended for new designs. The data sheet remains available for existing users.

A Maxim replacement or an industry second-source may be available. Please see the QuickView data sheet for this part or contact technical support for assistance.

For further information, [contact Maxim's Applications Tech Support].

19-0260; Rev 1; 3/95

MAXIM

Single/Dual/Quad, 10MHz Single-Supply Op Amps

General Description

The single MAX473, dual MAX474, and quad MAX475 are single-supply (2.7V to 5.25V), unity-gain-stable op amps with rail-to-rail output swing. Each op amp guarantees a 10MHz unity-gain bandwidth, 15V/µs slew rate, and 600Ω drive capability while typically consuming only 2mA supply current. In addition, the input range includes the negative supply rail and the output swings to within 50mV of each supply rail.

Single-supply operation makes these devices ideal for low-power and low-voltage portable applications. With their fast slew rate and settling time, they can replace higher-current op amps in large-signal applications. The MAX473/MAX474/MAX475 are available in DIP and SO packages in the industry-standard op-amp pin configurations. The MAX473 and MAX474 are also offered in the µMAX package, the smallest 8-pin SO.

Applications

- Portable Equipment
- Battery-Powered Instruments
- Signal Processing
- Discrete Filters
- Signal Conditioning
- Servo-Loops

Features

- ♦ **15V/µs Min Slew Rate**
- ♦ **+3V Single-Supply Operation**
- ♦ **Guaranteed 10MHz Unity-Gain Bandwidth**
- ♦ **2mA Supply Current per Amplifier**
- ♦ **Input Range Includes Negative Rail**
- ♦ **Outputs Short-Circuit Protected**
- ♦ **Rail-to-Rail Output Swing (to within ±50mV)**
- ♦ **µMAX Package (the smallest 8-pin SO)**

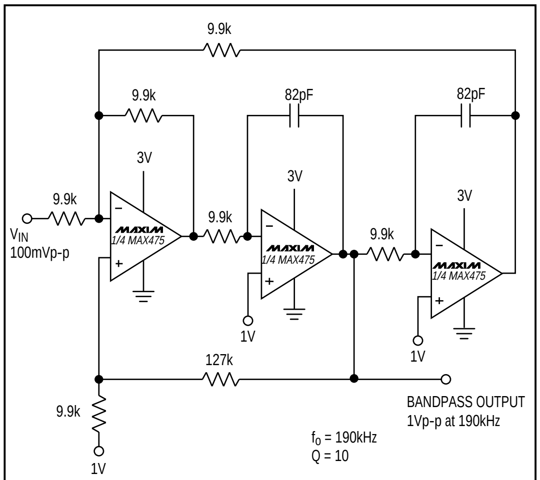
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX473CPA	0°C to +70°C	8 Plastic DIP
MAX473CSA	0°C to +70°C	8 SO
MAX473CUA	0°C to +70°C	8 µMAX
MAX473C/D	0°C to +70°C	Dice*
MAX473EPA	-40°C to +85°C	8 Plastic DIP
MAX473ESA	-40°C to +85°C	8 SO
MAX473MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

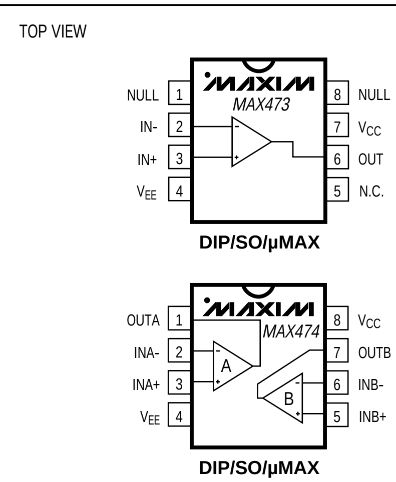
** Dice are specified at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



BANDPASS FILTER

Pin Configurations



Pin Configurations continued on last page.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} - V_{EE})..7V
Input Voltage (IN+, IN-, IN_+, IN_-) ....(V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration.....................................Continuous
Continuous Power Dissipation (T_A = +70°C)
  8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...727mW
  8-Pin SO (derate 5.88mW/°C above +70°C)................471mW
  8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
  8-Pin CERDIP (derate 8.00mW/°C above +70°C)........640mW
  14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)...800mW
  14-Pin SO (derate 8.33mW/°C above +70°C)..............667mW
  14-Pin CERDIP (derate 9.09mW/°C above +70°C)......727mW
Operating Temperature Ranges
  MAX47_C_ _ ....0°C to +70°C
  MAX47_E_ _..-40°C to +85°C
  MAX47_MJ_ ....-55°C to +125°C
Junction Temperatures
  MAX47_C_ _/E_ _... +150°C
  MAX47_MJ_ .... +175°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(+3V ≤ V_{CC} ≤ +5V, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX473			±0.70	±2.0	mV
		MAX474			±0.70	±2.0	
		MAX475			±0.80	±2.5	
Input Bias Current	I_B	Current flows out of terminals		0	80	150	nA
Input Offset Current	I_{OS}				±10	±30	nA
Common-Mode Voltage	V_{CM}	High		V_{CC} - 1.9	V_{CC} - 1.7		V
		Low			V_{EE} - 0.1	V_{EE}	
Common-Mode Rejection Ratio	CMRR	V_{EE} ≤ V_{CM} ≤ (V_{CC} - 1.9V)		80	90		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 6.0V		80	90		dB
Input Noise-Voltage Density	e_n	f = 10kHz			40		$nV/\sqrt{Hz}$
Large-Signal Gain (Note 1)	A_{VOL}	0.3V ≤ V_{OUT} ≤ (V_{CC} - 0.5V)	R_L = no load		110		dB
			R_L = 10kΩ	94	105		
			R_L = 600Ω	82	90		
		Sinking 5mA	V_{CC} = 5V		76		
			V_{CC} = 3V		100		
		Sourcing 5mA	V_{CC} = 5V		76		
			V_{CC} = 3V		90		
Output Voltage	V_{OH}	V_{IN}+ - V_{IN}- = +1V, R_L = no load		V_{CC} - 0.05			V
	V_{OL}	V_{IN}+ - V_{IN}- = -1V, R_L = no load				V_{EE} + 0.05	
Slew Rate	SR	V_{CC} = 5V, R_L = 10kΩ, C_L = 20pF, V_{IN}+ - V_{IN}- = +1V step		15	17		V/µs
Unity-Gain Bandwidth (Note 2)	GBW	3V ≤ V_{CC} ≤ 5V		10	12		MHz
		V_{CC} = 2.7V			10		

ELECTRICAL CHARACTERISTICS (continued)

(+3V ≤ V_{CC} ≤ +5V, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Settling Time	t_S	To 0.1%, C_L = 20pF			400		ns
Power-Up Time	t_{PU}	A_V = +1, V_{IN} = 1/2 V_{CC} step, see *Typical Operating Characteristics*			700		ns
Overshoot		C_L = 150pF			10		%
		C_L = 20pF			5		
Phase Margin		R_L = 10kΩ, C_L = 20pF	V_{CC} = 5V		63		degrees
			V_{CC} = 3V		58		
Gain Margin		R_L = 10kΩ, C_L = 20pF	V_{CC} = 5V		10		dB
			V_{CC} = 3V		12		
Supply Current	I_S	Per amplifier			2.0	3.0	mA
Operating Supply-Voltage Range		Single supply		2.7		5.25	V
		Dual supplies		±1.35		±2.625	

ELECTRICAL CHARACTERISTICS

(+3V ≤ V_{CC} ≤ +5V, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX473				±2.0	mV
		MAX474				±2.0	
		MAX475				±3.0	
Input Bias Current	I_B	Current flows out of terminals		0		175	nA
Input Offset Current	I_{OS}					±35	nA
Common-Mode Rejection Ratio	CMRR	V_{EE} ≤ V_{CM} ≤ (V_{CC} - 1.9V)		78			dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 6.0V		78			dB
Large-Signal Gain (Note 1)	A_{VOL}	0.4V ≤ V_{OUT} ≤ (V_{CC} - 0.6V)	R_L = 10kΩ	94			dB
			R_L = 600Ω	80			
Output Voltage	V_{OH}	V_{IN}+ - V_{IN}- = +1V, R_L = no load		V_{CC} - 0.07			V
	V_{OL}	V_{IN}+ - V_{IN}- = -1V, R_L = no load				V_{EE} + 0.07	
Slew Rate	SR	V_{CC} = 5V, R_L = 10kΩ, C_L = 20pF, V_{IN}+ - V_{IN}- = +1V step		12			V/µs
Supply Current	I_S	Per amplifier				3.3	mA
Operating Supply-Voltage Range		Single supply		2.7		5.25	V
		Dual supplies		±1.35		±2.625	

Single/Dual/Quad, 10MHz Single-Supply Op Amps

ELECTRICAL CHARACTERISTICS

($+3V \le V_{CC} \le +5V$, $V_{EE} = 0V$, $V_{CM} = 0.5V$, $V_{OUT} = 0.5V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX473				±2.3	mV
		MAX474				±2.3	
		MAX475				±3.3	
Input Bias Current	I_B	Current flows out of terminals		0		200	nA
Input Offset Current	I_{OS}					±50	nA
Common-Mode Rejection Ratio	CMRR	$V_{EE} \le V_{CM} \le (V_{CC} - 2.0V)$		72			dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 6.0V		72			dB
Large-Signal Gain (Note 1)	A_{VOL}	$0.4V \le V_{OUT} \le (V_{CC} - 0.6V)$	$R_L = 10k\Omega$	94			dB
			$R_L = 600\Omega$	72			
Output Voltage	V_{OH}	$V_{IN}+ - V_{IN}- = +1V$, R_L = no load		$V_{CC} - 0.08$			V
	V_{OL}	$V_{IN}+ - V_{IN}- = -1V$, R_L = no load				$V_{EE} + 0.08$	
Slew Rate	SR	$V_{CC} = 5V$, $R_L = 10k\Omega$, $C_L = 20pF$, $V_{IN}+ - V_{IN}- = +1V$ step		10			V/µs
Supply Current	I_S	Per amplifier				3.4	mA
Operating Supply-Voltage Range		Single supply		2.7		5.25	V
		Dual supplies		±1.35		±2.625	

ELECTRICAL CHARACTERISTICS

($+3V \le V_{CC} \le +5V$, $V_{EE} = 0V$, $V_{CM} = 0.5V$, $V_{OUT} = 0.5V$, $T_A = -55°C$ to $+125°C$, unless otherwise noted.)

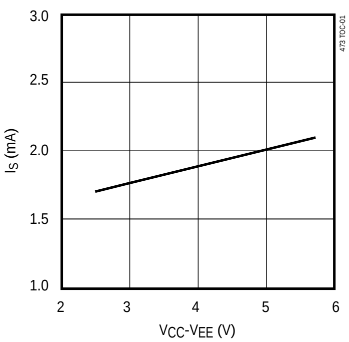
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX473				±2.8	mV
		MAX474				±2.8	
		MAX475				±4.0	
Input Bias Current	I_B	Current flows out of terminals		0		225	nA
Input Offset Current	I_{OS}					±60	nA
Common-Mode Rejection Ratio	CMRR	$V_{EE} \le V_{CM} \le (V_{CC} - 2.15V)$		70			dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 6.0V		70			dB
Large-Signal Gain (Note 1)	A_{VOL}	$0.5V \le V_{OUT} \le (V_{CC} - 0.6V)$	$R_L = 10k\Omega$	90			dB
			$R_L = 600\Omega$	70			
Output Voltage	V_{OH}	$V_{IN}+ - V_{IN}- = +1V$, R_L = no load		$V_{CC} - 0.1$			V
	V_{OL}	$V_{IN}+ - V_{IN}- = -1V$, R_L = no load				$V_{EE} + 0.1$	
Slew Rate	SR	$V_{CC} = 5V$, $R_L = 10k\Omega$, $C_L = 20pF$, $V_{IN}+ - V_{IN}- = +1V$ step		9			V/µs
Supply Current	I_S	Per amplifier				3.6	mA
Operating Supply-Voltage Range		Single supply		2.7		5.25	V
		Dual supplies		±1.35		±2.625	

Note 1: Gain decreases to zero as the output swings beyond the specified limits.
Note 2: Guaranteed by correlation to slew rate.

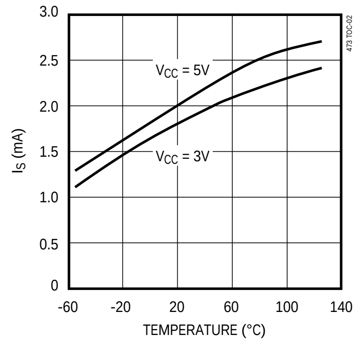
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

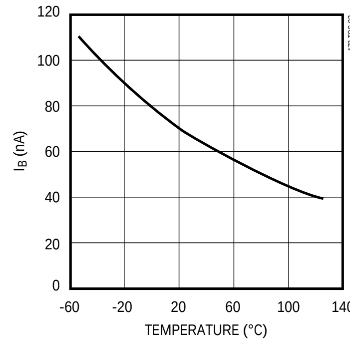
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE



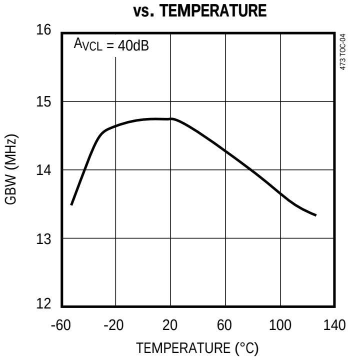
SUPPLY CURRENT vs. TEMPERATURE



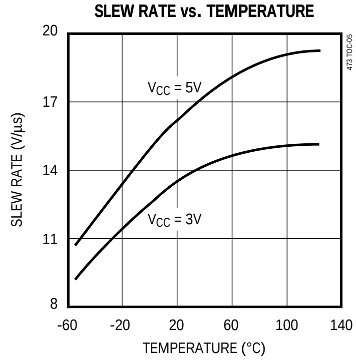
INPUT BIAS CURRENT vs. TEMPERATURE



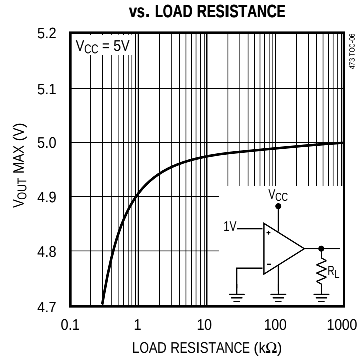
GAIN-BANDWIDTH PRODUCT vs. TEMPERATURE



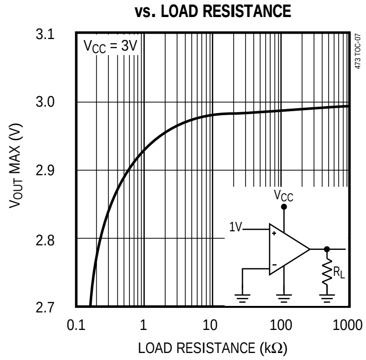
SLEW RATE vs. TEMPERATURE



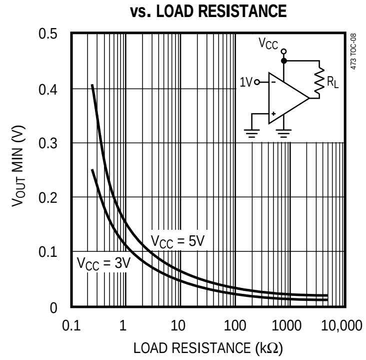
MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE



MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE



MINIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE

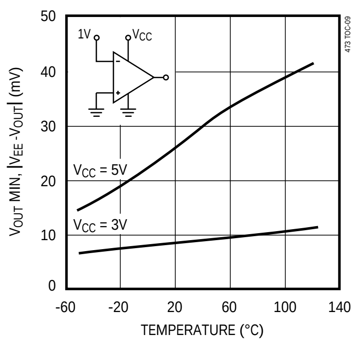


Single/Dual/Quad, 10MHz Single-Supply Op Amps

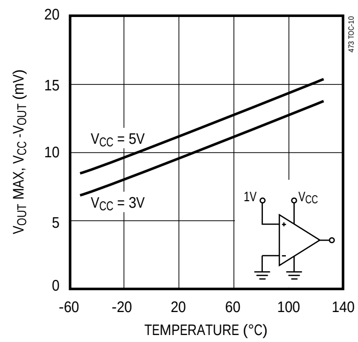
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

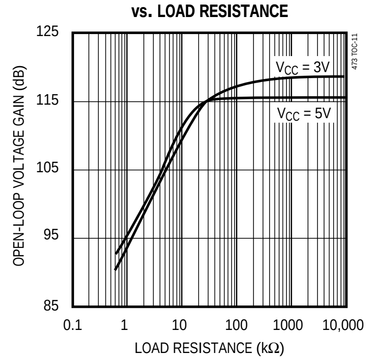
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE



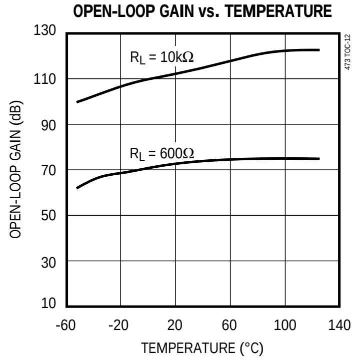
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



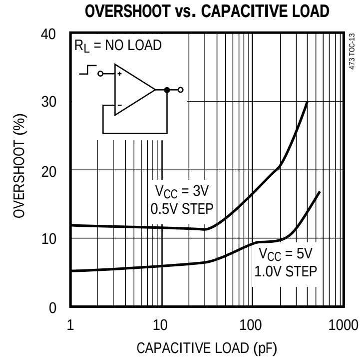
OPEN-LOOP VOLTAGE GAIN vs. LOAD RESISTANCE



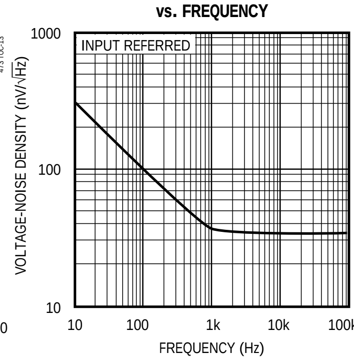
OPEN-LOOP GAIN vs. TEMPERATURE



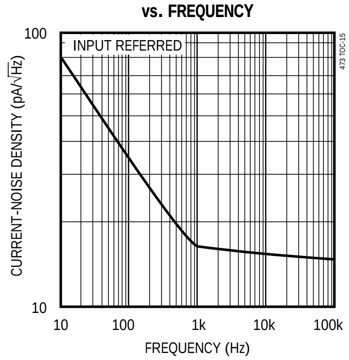
OVERSHOOT vs. CAPACITIVE LOAD



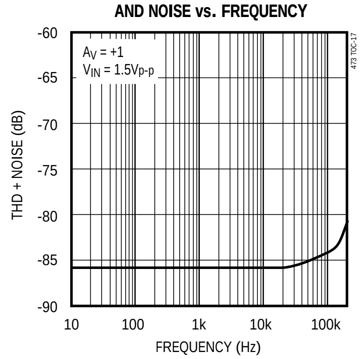
VOLTAGE-NOISE DENSITY vs. FREQUENCY



CURRENT-NOISE DENSITY vs. FREQUENCY

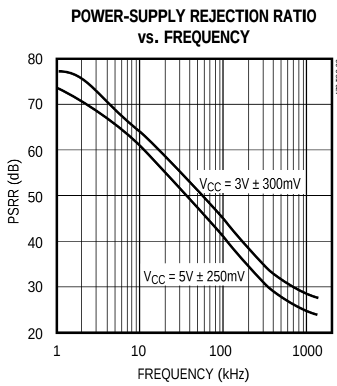


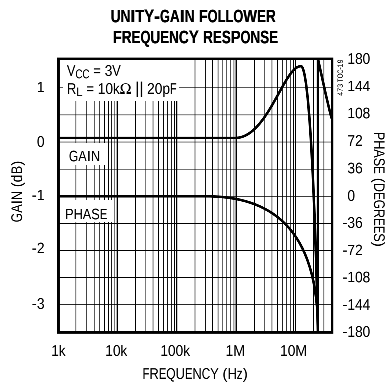
TOTAL HARMONIC DISTORTION AND NOISE vs. FREQUENCY

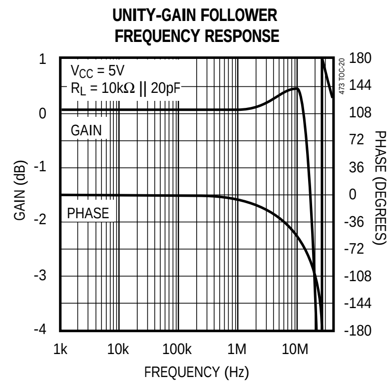


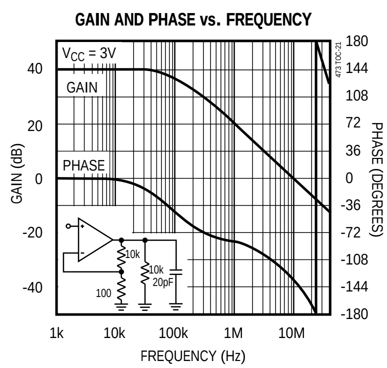
Typical Operating Characteristics (continued)

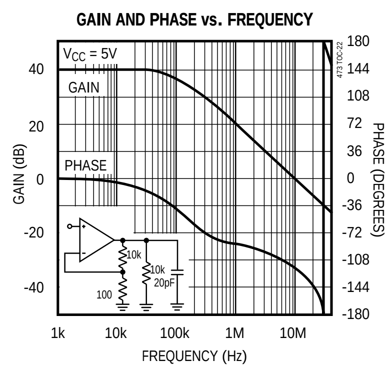
(V_{CC} = 5V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

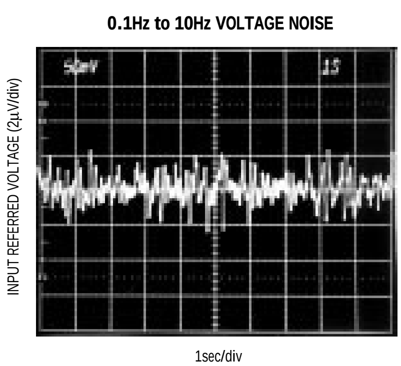


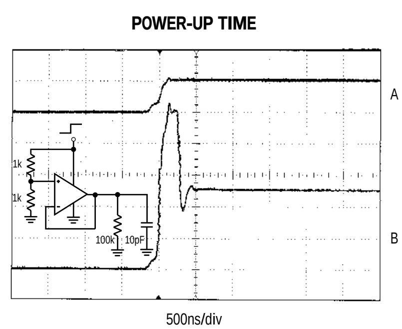










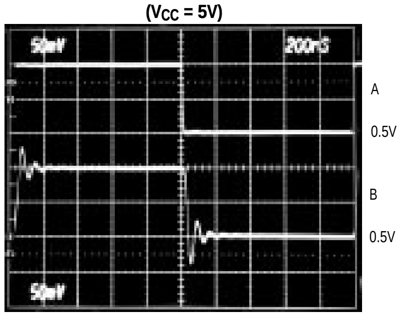


A : V_{CC}, 5V/div
B : V_{OUT}, 1V/div

Typical Operating Characteristics (continued)

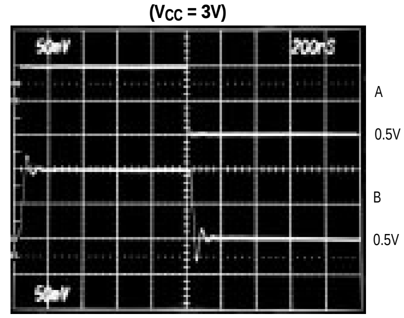
(V_{CC} = 5V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

SMALL-SIGNAL TRANSIENT RESPONSE (V_{CC} = 5V)



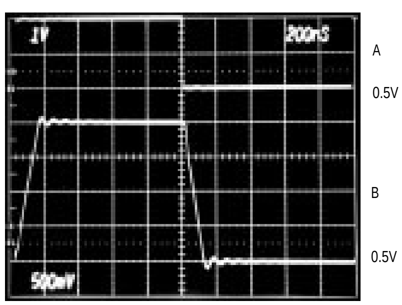
V_{CC} = 5V, A_V = +1, R_L = 10kΩ, C_L = 220pF
A : V_{IN}, 50mV/div
B : V_{OUT}, 50mV/div

SMALL-SIGNAL TRANSIENT RESPONSE (V_{CC} = 3V)



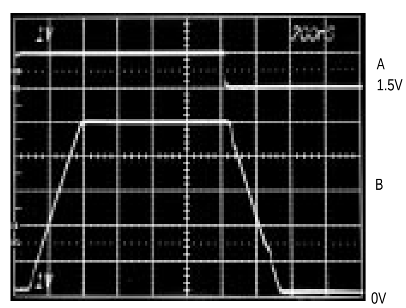
V_{CC} = 3V, A_V = +1, R_L = 10kΩ, C_L = 100pF
A : V_{IN}, 50mV/div
B : V_{OUT}, 50mV/div

LARGE-SIGNAL TRANSIENT RESPONSE



V_{CC} = 5V, A_V = +1, R_L = 10kΩ, C_L = 220pF
A : V_{IN}, 1V/div
B : V_{OUT}, 500mV/div

OVERDRIVING THE OUTPUT



V_{CC} = 5V, V_{IN-} = 2.0V, R_L = 10kΩ, C_L = 33pF
A : V_{IN}+, 1V/div
B : V_{OUT}, 1V/div

Pin Description

PIN			NAME	FUNCTION
MAX473	MAX474	MAX475		
1, 8	—	—	NULL	Offset Null Input. Connect to one end of 2kΩ potentiometer for offset voltage trimming. Connect wiper to V_{EE}. See Figure 1.
—	1	1	OUTA	Amplifier A Output
2	—	—	IN-	Inverting Input
—	2	2	INA-	Amplifier A Inverting Input
3	—	—	IN+	Noninverting Input
—	3	3	INA+	Amplifier A Noninverting Input
4	4	11	V_{EE}	Negative Power-Supply Pin. Connect to ground or a negative voltage.
5	—	—	N.C.	No Connect—not internally connected
—	5	5	INB+	Amplifier B Noninverting Input
6	—	—	OUT	Amplifier Output
—	6	6	INB-	Amplifier B Inverting Input
—	7	7	OUTB	Amplifier B Output
7	8	4	V_{CC}	Positive Power-Supply Pin. Connect to (+) terminal of power supply.
—	—	8	OUTC	Amplifier C Output
—	—	9	INC-	Amplifier C Inverting Input
—	—	10	INC+	Amplifier C Noninverting Input
—	—	12	IND+	Amplifier D Noninverting Input
—	—	13	IND-	Amplifier D Inverting Input
—	—	14	OUTD	Amplifier D Output

Applications Information

Power Supplies

The MAX473/MAX474/MAX475 operate from a single 2.7V to 5.25V power supply, or from dual supplies of ±1.35V to ±2.625V. For single-supply operation, bypass the power supply with 0.1µF. If operating from dual supplies, bypass each supply to ground. With 0.1µF bypass capacitance, channel separation (MAX474/MAX475) is typically better than 120dB with signal frequencies up to 300kHz. Increasing the bypass capacitance (e.g. 10µF || 0.1µF) maintains channel separation at higher frequencies.

Minimizing Offsets

The MAX473's maximum offset voltage is ±2mV (T_A = +25°C). If additional offset adjustment is required, connect a 2kΩ trim potentiometer between pins 1, 8, and 4 (Figure 1). Input offset voltage for the dual MAX474 and quad MAX475 cannot be externally trimmed.

The MAX473/MAX474/MAX475 are bipolar op amps with low input bias currents. The bias currents at both inputs flow out of the device. Matching the resistance at the op amp's inputs significantly reduces the offset error caused by the bias currents. Place a resistor (R3) from the noninverting input to ground when using the inverting configuration (Figure 2a); place R3 in series with the noninverting input when using the noninverting configuration (Figure 2b). Select R3 such that the parallel combination of R2 and R1 equals R3. Adding R3 will slightly increase the op amp's voltage noise.

Output Loading and Stability

The MAX473/MAX474/MAX475 op amps are unity-gain stable. Any op amp's stability depends on the configuration, closed-loop gain, and load capacitance. The unity-gain, noninverting buffer is the most sensitive gain configuration, and driving capacitive loads decreases stability.

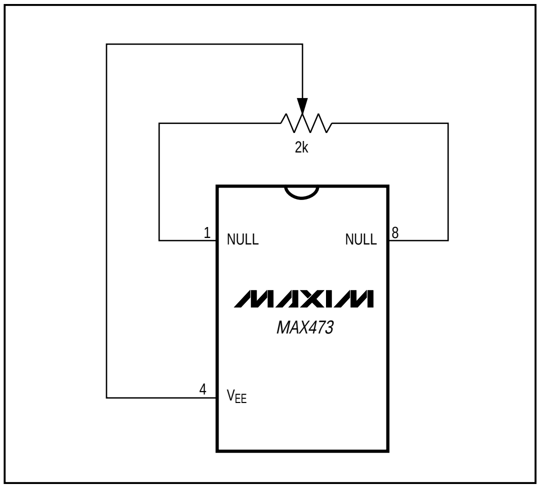


Figure 1. Offset Null Circuit

The MAX473/MAX474/MAX475 have excellent phase margin (the difference between 180° and the unity-gain phase angle). It is typically 63° with a load of 10kΩ in parallel with 20pF. Generally, higher phase margins indicate greater stability.

Capacitive loads form an RC network with the op amp's output resistance, causing additional phase shift that reduces the phase margin. Figure 3 shows the MAX473/MAX474/MAX475 output response when driving a 390pF load in parallel with 10kΩ.

When driving large capacitive loads, add an output isolation resistor, as shown in Figure 4. This resistor improves the phase margin by isolating the load capacitance from the amplifier output. Figure 5 shows the MAX473/MAX474/MAX475 driving a capacitive load of 1000pF using the circuit of Figure 4.

Feedback Resistors

The feedback resistors appear as a resistance network to the op amp's feedback input (Figure 2). This resistance, combined with the op amp's input and stray capacitance (total input capacitance), forms a pole that adds unwanted phase shift when either the total input capacitance or feedback resistance is too large. For example, using the noninverting configuration with a gain of 10, if the total capacitance at the negative input is 10pF and the effective resistance ($R1 \parallel R2$) is 9kΩ, this RC network introduces a pole at f_o = 1.8MHz. At input frequencies above f_o, the pole introduces additional phase shift, which reduces the overall bandwidth and adversely affects stability. Choose feedback resistors small enough so they do not adversely affect the op amp's operation at the frequencies of interest.

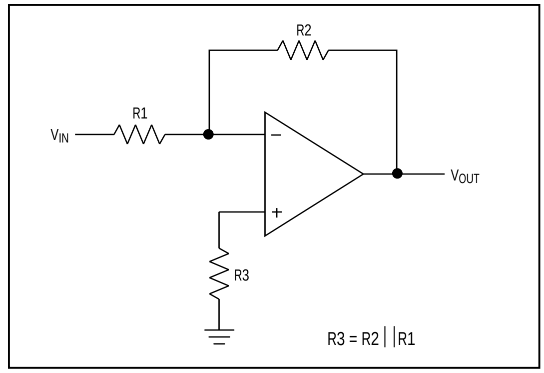


Figure 2a. Reducing Offset Error Due to Bias Current: Inverting Configuration

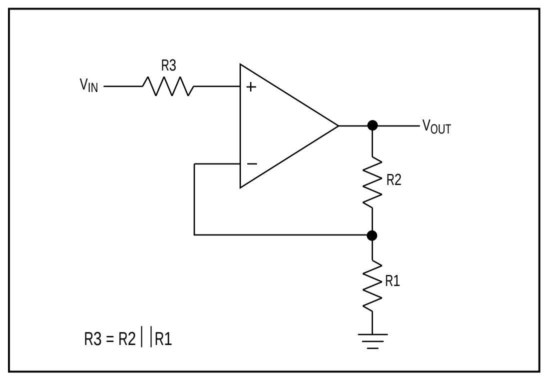
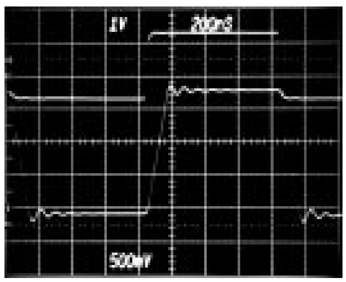


Figure 2b. Reducing Offset Error Due to Bias Current: Noninverting Configuration

Overdriving the Outputs

The output voltage swing for specified operation is from (V_{EE} + 0.3V) to (V_{CC} - 0.5V) (*see Electrical Characteristics*). Exercising the outputs beyond these limits drives the output transistors toward saturation, resulting in bandwidth degradation, response-time increase, and gain decrease (which affects linearity). Operation in this region causes a slight distortion in the output waveform, but does not adversely affect the op amp.



Driving 390pF in parallel with 10kΩ, V_{CC} = 5V, buffer configuration

Figure 3. MAX474 Driving 390pF

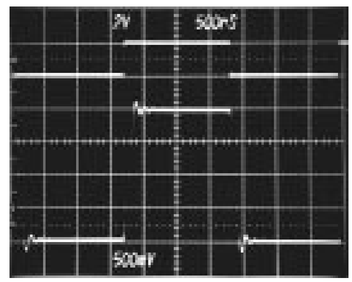


Figure 5. The MAX473 easily drives 1000pF using the Capacitive-Load Driving Circuit (Figure 4).

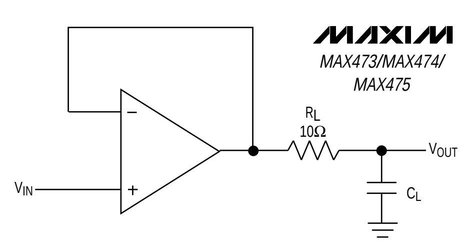


Figure 4. Capacitive-Load Driving Circuit

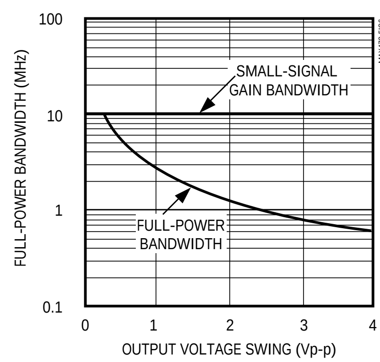


Figure 6. Full-Power Bandwidth vs. Peak-to-Peak AC Voltage

Full-Power Bandwidth

The MAX473/MAX474/MAX475's fast 15V/µs slew rate maximizes full-power bandwidth (FPBW). The FPBW is given by:

$$\text{FPBW (Hz)} = \frac{SR}{\pi\,[V_{OUT}\ \text{peak-to-peak(max)}]}$$

where the slew rate (SR) is 15V/µs min. Figure 6 shows the full-power bandwidth as a function of the peak-to-peak AC output voltage.

Layout

A good layout improves performance by decreasing the amount of stray capacitance at the amplifier's inputs and output. Since stray capacitance might be unavoidable, minimize trace lengths and resistor leads, and place external components as close to the pins as possible.

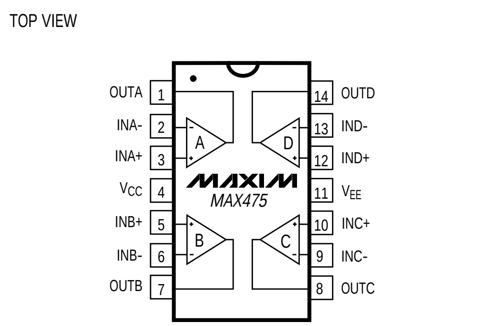
Single/Dual/Quad, 10MHz Single-Supply Op Amps

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX474CPA	0°C to +70°C	8 Plastic DIP
MAX474CSA	0°C to +70°C	8 SO
MAX474CUA	0°C to +70°C	8 µMAX
MAX474C/D	0°C to +70°C	Dice*
MAX474EPA	-40°C to +85°C	8 Plastic DIP
MAX474ESA	-40°C to +85°C	8 SO
MAX474MJA	-55°C to +125°C	8 CERDIP
MAX475CPD	0°C to +70°C	14 Plastic DIP
MAX475CSD	0°C to +70°C	14 SO
MAX475EPD	-40°C to +85°C	14 Plastic DIP
MAX475ESD	-40°C to +85°C	14 SO
MAX475MJD	-55°C to +125°C	14 CERDIP

Dice are specified at T_A = +25°C, DC parameters only.

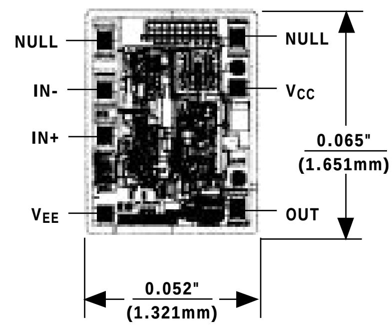
Pin Configurations (continued)



DIP/SO

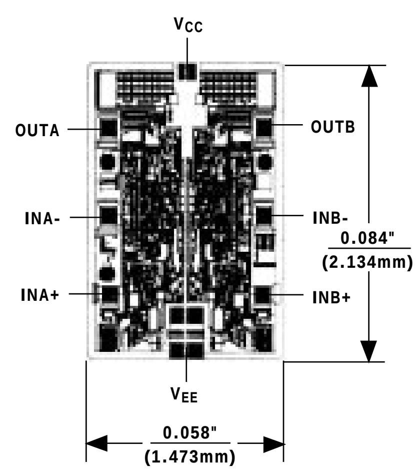
Chip Topographies

MAX473



TRANSISTOR COUNT: 185
SUBSTRATE CONNECTED TO V_{EE}

MAX474



TRANSISTOR COUNT: 355
SUBSTRATE CONNECTED TO V_{EE}

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