

Designer's™ Data Sheet

Surface Mount

Schottky Power Rectifier

POWERMITE® Power Surface Mount Package

The Schottky Powermite employs the Schottky Barrier principle with a barrier metal and epitaxial construction that produces optimal forward voltage drop–reverse current tradeoff. The advanced packaging techniques provide for a highly efficient micro miniature, space saving surface mount Rectifier. With its unique heatsink design, the Powermite has the same thermal performance as the SMA while being 50% smaller in footprint area, and delivering one of the lowest height profiles, < 1.1 mm in the industry. Because of its small size, it is ideal for use in portable and battery powered products such as cellular and cordless phones, chargers, notebook computers, printers, PDAs and PCMCIA cards. Typical applications are ac/dc and dc–dc converters, reverse battery protection, and “Oring” of multiple supply voltages and any other application where performance and size are critical.

Features:

- Low Profile — Maximum Height of 1.1 mm
- Small Footprint — Footprint Area of 8.45 mm²
- Low V_F Provides Higher Efficiency and Extends Battery Life
- Supplied in 12 mm Tape and Reel — 12,000 Units per Reel
- Low Thermal Resistance with Direct Thermal Path of Die on Exposed Cathode Heat Sink

Mechanical Characteristics:

- Powermite is JEDEC Registered as D0–216AA
- Case: Molded Epoxy
- Epoxy Meets UL94, VO at 1/8"
- Weight: 62 mg (approximately)
- Device Marking: BCV
- Lead and Mounting Surface Temperature for Soldering Purposes. 260°C Maximum for 10 Seconds

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	V
Average Rectified Forward Current (At Rated V_R , $T_C = 130^\circ\text{C}$)	I_O	1.0	A
Peak Repetitive Forward Current (At Rated V_R , Square Wave, 20 kHz, $T_C = 135^\circ\text{C}$)	I_{FRM}	2.0	A
Non–Repetitive Peak Surge Current (Non–Repetitive peak surge current, halfwave, single phase, 60 Hz)	I_{FSM}	50	A
Storage Temperature	T_{stg}	–65 to 150	°C
Operating Junction Temperature	T_J	–65 to 150	°C
Voltage Rate of Change (Rated V_R , $T_J = 25^\circ\text{C}$)	dv/dt	10,000	V/ μs

THERMAL CHARACTERISTICS

Thermal Resistance – Junction–to–Lead (Anode) (1)	R_{tjl}	35	°C/W
Thermal Resistance – Junction–to–Tab (Cathode) (1)	R_{tjtab}	23	
Thermal Resistance – Junction–to–Ambient (1)	R_{tja}	277	

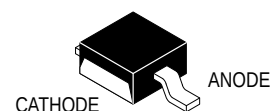
(1) Mounted with minimum recommended pad size, PC Board FR4, See Figures 9 and 10.

POWERMITE is a registered trademark of MicroSemi Corporation

Designer's Data for “Worst Case” Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate “worst case” design.

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**SCHOTTKY BARRIER
RECTIFIER
1.0 AMPERES
20 VOLTS**



**CASE 457–04
ISSUE C**

ELECTRICAL CHARACTERISTICS

Maximum Instantaneous Forward Voltage (2), See Figure 2 ($I_F = 0.1$ A) ($I_F = 1.0$ A) ($I_F = 2.0$ A)	V_F	$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	V
		0.455	0.360	
		0.530	0.455	
Maximum Instantaneous Reverse Current, See Figure 4 ($V_R = 20$ V) ($V_R = 10$ V) ($V_R = 5.0$ V)	I_R	$T_J = 25^\circ\text{C}$	$T_J = 100^\circ\text{C}$	μA
		10	1600	
		1.0	500	
		0.5	300	

(2) Pulse Test: Pulse Width ≤ 250 μs , Duty Cycle $\leq 2\%$.

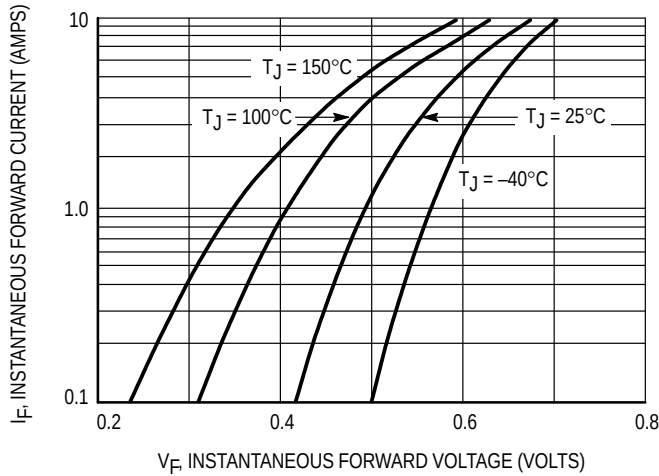


Figure 1. Typical Forward Voltage

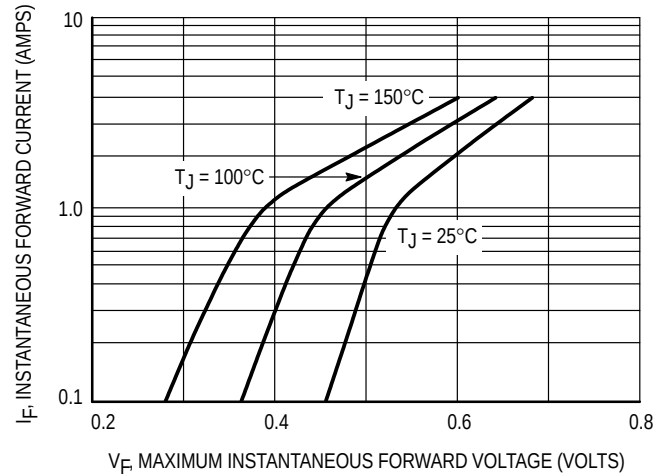


Figure 2. Maximum Forward Voltage

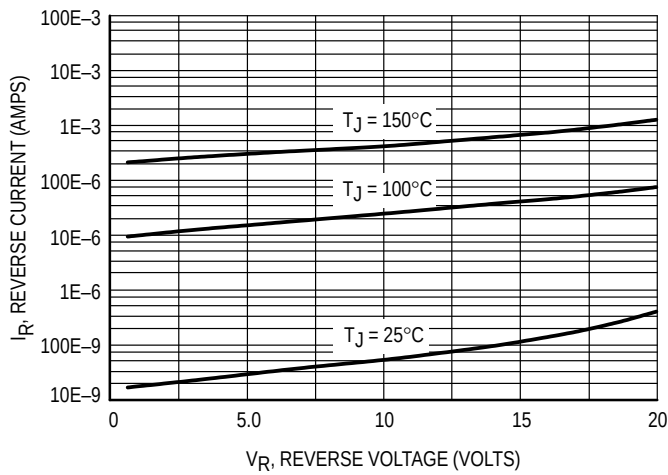


Figure 3. Typical Reverse Current

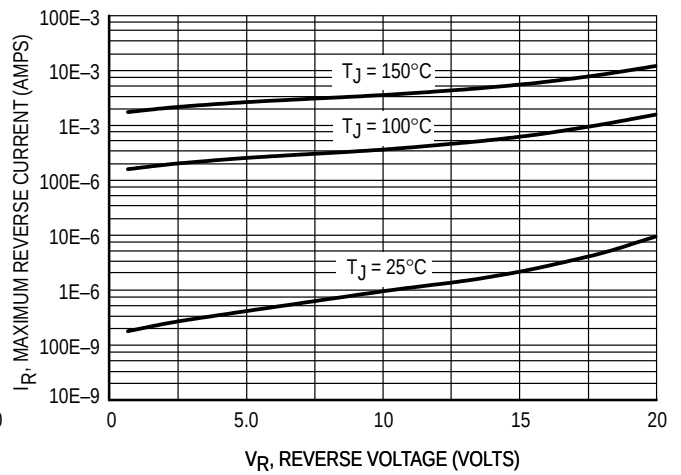


Figure 4. Maximum Reverse Current

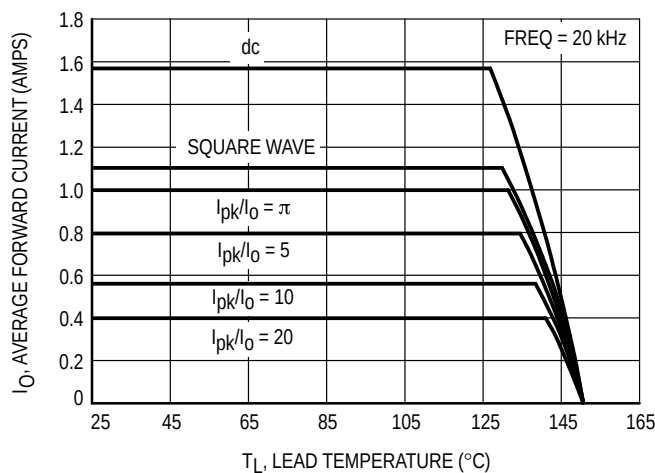


Figure 5. Current Derating

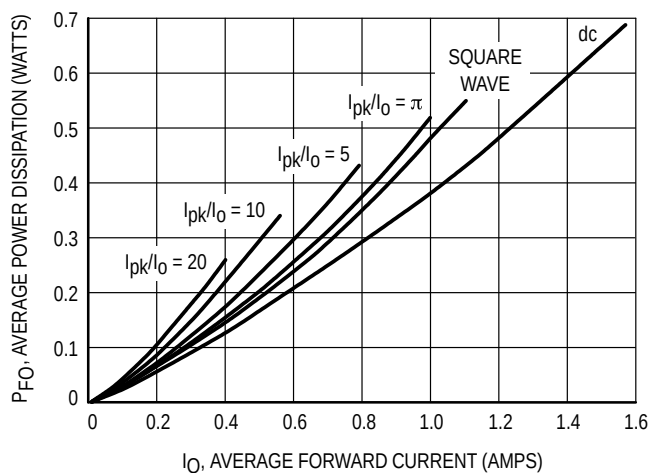


Figure 6. Forward Power Dissipation

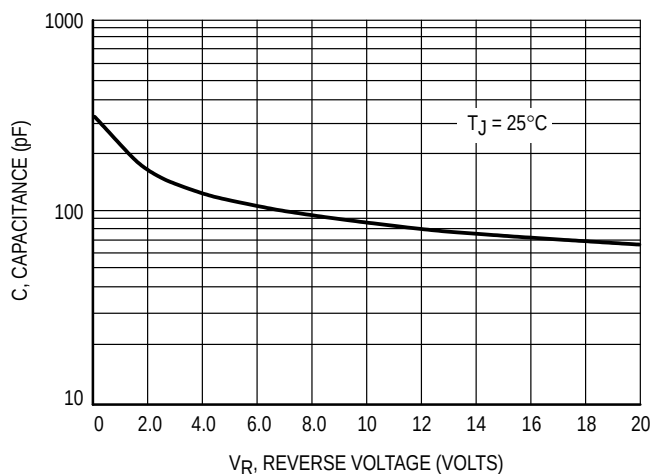


Figure 7. Capacitance

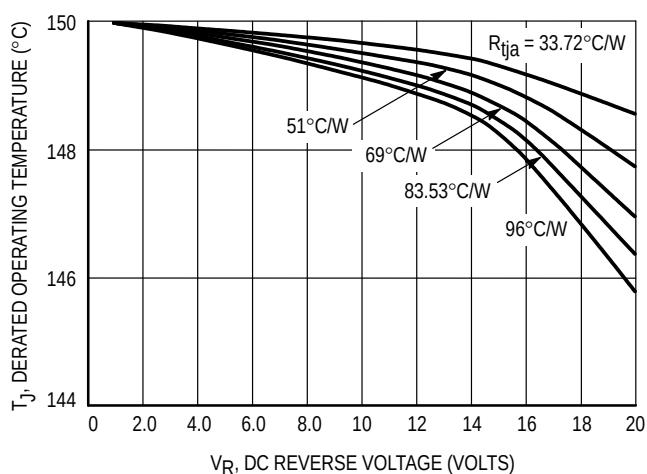


Figure 8. Typical Operating Temperature Derating*

* Reverse power dissipation and the possibility of thermal runaway must be considered when operating this device under any reverse voltage conditions. Calculations of T_J therefore must include forward and reverse power effects. The allowable operating T_J may be calculated from the equation:

$$T_J = T_{Jmax} - r(t)(P_f + P_r) \text{ where}$$

$r(t)$ = thermal impedance under given conditions,
 P_f = forward power dissipation, and
 P_r = reverse power dissipation

This graph displays the derated allowable T_J due to reverse bias under DC conditions only and is calculated as $T_J = T_{Jmax} - r(t)P_r$, where $r(t) = R_{thja}$. For other power applications further calculations must be performed.

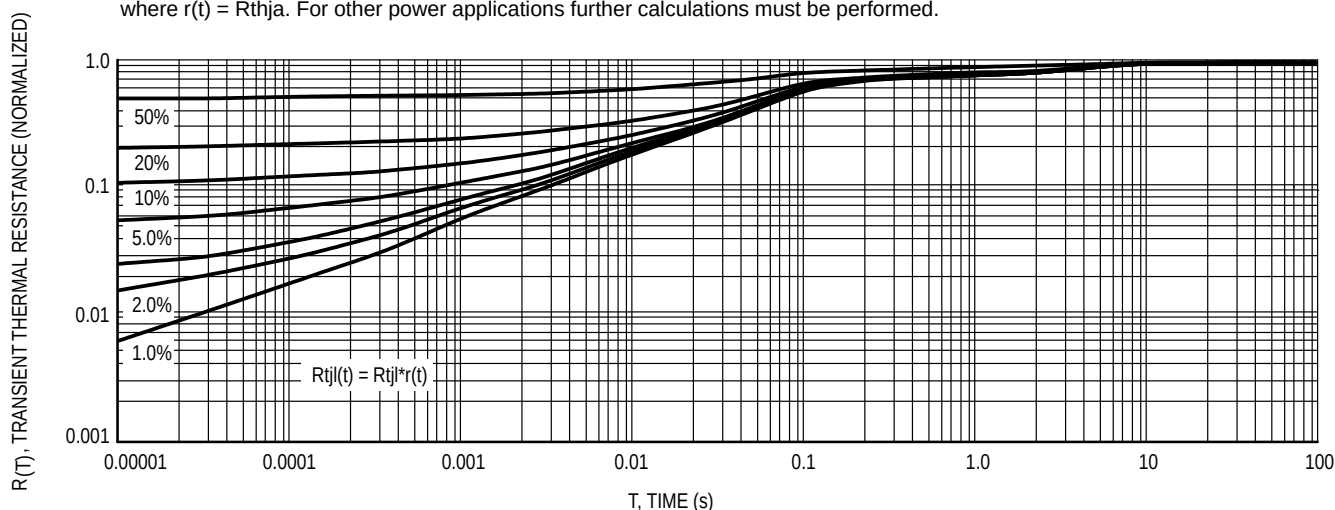


Figure 9. Thermal Response Junction to Lead

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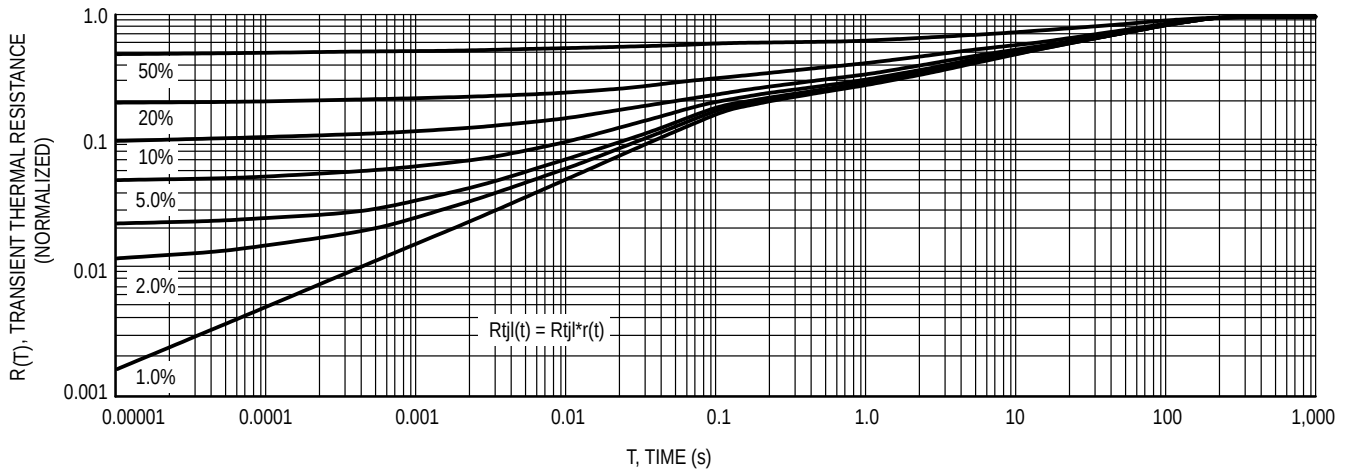
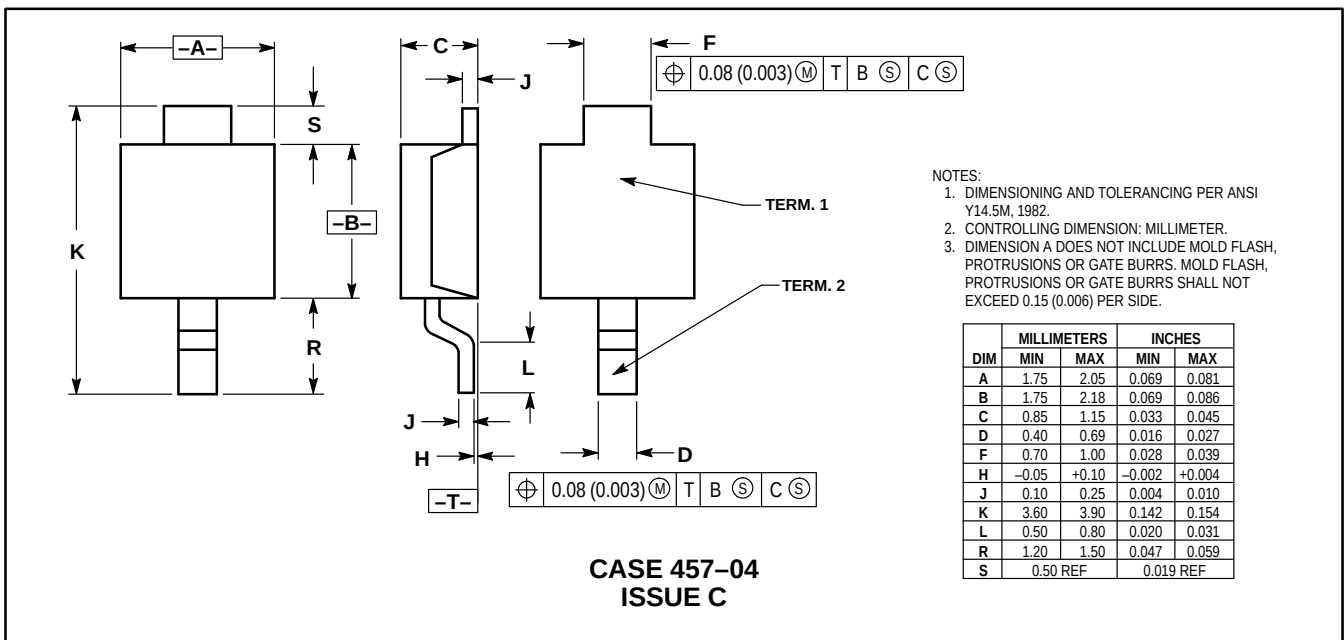


Figure 10. Thermal Response Junction to Ambient

PACKAGE DIMENSIONS



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