256 x 8-BIT CMOS EEPROMS with I²C-bus interface

PCx8582x-2 Family

FEATURES

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Low power CMOS; maximum active current 2 mA, maximum standby current 10 µA
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, PCF8572 and PCF8581
- Write operations

  byte write mode

  8-byte page write mode (minimizes total write time per byte)
- Read operations

  sequential read and random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- High reliability by using a redundant storage code
- Endurance 100 k; T_{amb} = +85 °C

GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories. By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCx8582x-2 devices can be connected to the I²C-bus.
Chip select is accomplished by the three address inputs.

Timing of the Erase/Write cycle is achieved internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

An option exists for using an external clock for timing the length of an Erase/Write cycle.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive suppy voltage		2.5	–	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	60	µA
		V_{DD} = 6 V	–	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	0.5	mA
		V_{DD} = 6 V	–	–	2.0	mA
I_{DDO}	supply current STANDBY					
		V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA

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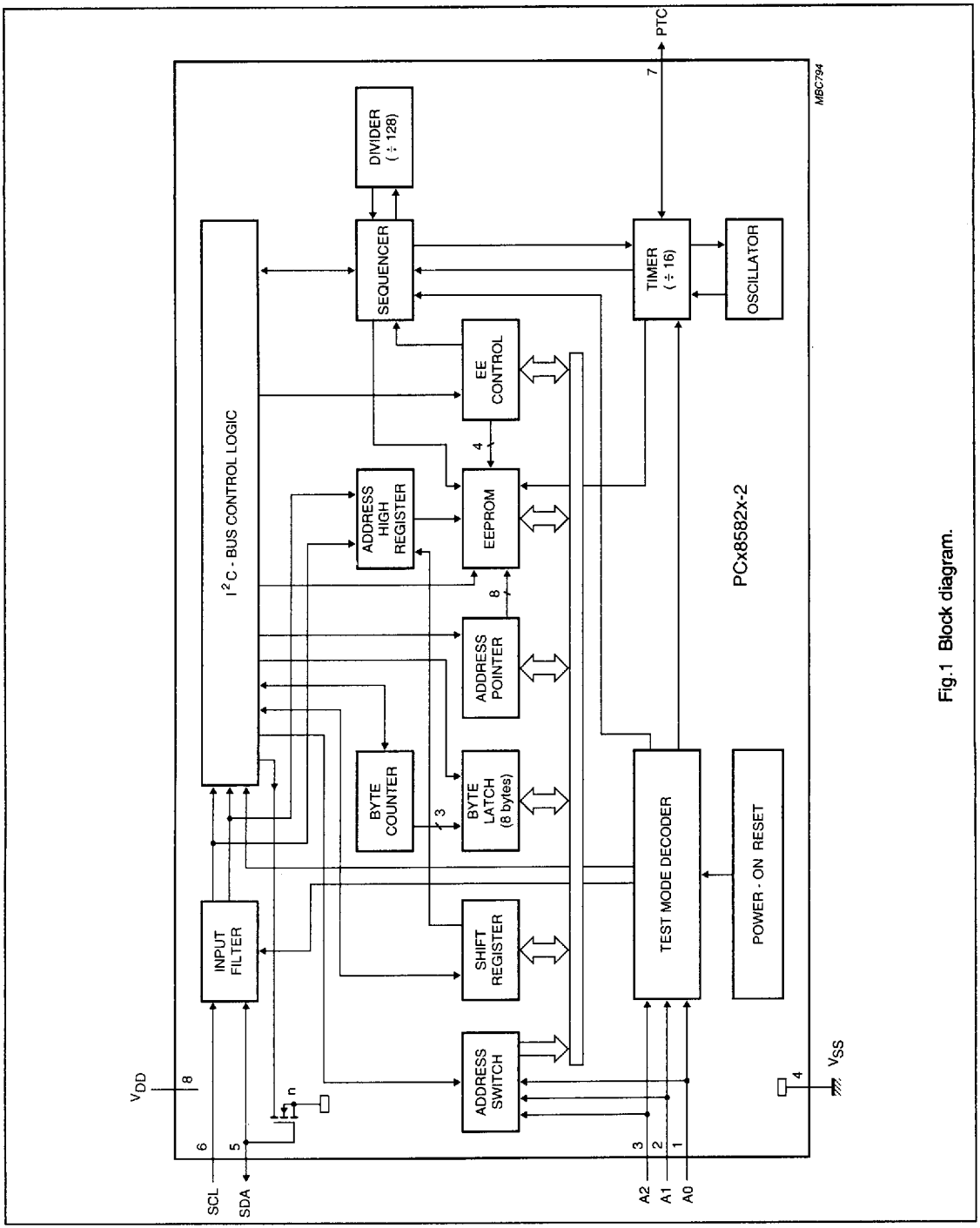

Fig.1 Block diagram.

256 x 8-BIT CMOS EEPROMS with I²C-bus interface

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ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCx8582x-2P	8	DIL	plastic	SOT97
PCx8582x-2T	8	SO8	plastic	SOT96A

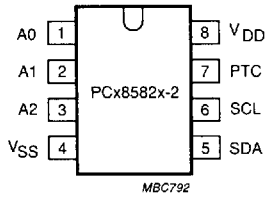


Fig.2 Pin configuration (SOT96A and SOT97).

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
A2	3	address input
V_{SS}	4	negative supply voltage
SDA	5	serial data
SCL	6	serial clock
PTC	7	programming time control
V_{DD}	8	positive supply voltage

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage		−0.3	+7.0	V
V_I	voltage on any input	$\|Z_I\| > 500\ \Omega$	V_{SS}−0.8	V_{DD} + 0.8	V
I_I	current on any input pin		−	1	mA
I_O	output current		−	10	mA
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range				
	PCF8582C-2; PCF8582E-2		−40	+85	°C
	PCD8582D-2		−25	+70	°C
	PCA8582F-2		−40	+125	°C

CHARACTERISTICS

PCF8582C-2; V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C
PCD8582D-2; V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C
PCF8582E-2; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C
PCA8582F-2; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +125 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage					
	PCF8582C-2		2.5	–	6.0	V
	PCD8582D-2		3.0	–	6.0	V
	PCF8582E-2; PCA8582F-2		4.5	–	5.5	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
	PCF8582C-2; PCD8582D-2	V_{DD} = 3 V	–	–	60	µA
		V_{DD} = 6 V	–	–	200	µA
	PCF8582E-2	$V_{DD\ max}$	–	–	200	µA
	PCF8582F-2	$V_{DD\ max}$	–	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
	PCF8582C-2; PCD8582D-2	V_{DD} = 3 V	–	–	0.5	mA
		V_{DD} = 6 V	–	–	2.0	mA
	PCF8582E-2	$V_{DD\ max}$	–	–	2.0	mA
	PCF8582F-2	$V_{DD\ max}$	–	–	2.0	mA
I_{DDO}	supply current STANDBY					
	PCF8582C-2; PCD8582D-2	V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA
	PCF8582E-2	$V_{DD\ max}$	–	–	10	µA
	PCF8582F-2	$V_{DD\ max}$	–	–	10	µA
PTC input						
V_{IH}	HIGH level input voltage		0.9 V_{DD}	–	V_{DD}+0.8	V
V_{IL}	LOW level input voltage		–0.8	–	0.1 V_{DD}	V
SCL input						
V_{IH}	HIGH level input voltage		0.7 V_{DD}	–	V_{DD}+0.8	V
V_{IL}	LOW level input voltage		–0.8	–	0.3 V_{DD}	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	–	±1	µA
f_{SCL}	clock frequency		0	–	100	kHz
C_i	input capacitance	$V_I = V_{SS}$	–	–	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA input/output						
V_{IL}	LOW level input voltage		–0.8	–	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	–	V_{DD}+0.8	V
V_{OL}	LOW level output voltage	I_{OH} = 3 mA; $V_{DD\ min}$	–	–	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	–	–	1	µA
C_i	input capacitance	$V_I = V_{SS}$	–	–	7	pF
Data retention time						
t_S	data retention time	T_{amb} = +55 °C	10	–	–	yrs

WRITE CYCLE LIMITS

Selection of the chip address is achieved by connecting the A0, A1 and A2 inputs to either V_{DD} or V_{SS}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{E/W}$	ERASE/WRITE cycle time					
	internal oscillator		–	7	–	ms
	external clock		4	–	10	ms
$N_{E/W}$	ERASE/WRITE cycles per byte					
	PCF8582C-2	T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	–	–	100 000	
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	–	–	500 000	
	PCD8582D-2	T_{amb} = –25 to +70 °C; $t_{E/W}$ = 4 to 10 ms	–	–	10 000	
		T_{amb} = –25 to +40 °C; $t_{E/W}$ = 5 ms	–	–	100 000	
	PCF8582E-2	T_{amb} = –40 to +85 °C; $t_{E/W}$ = 4 to 10 ms	–	–	10 000	
		T_{amb} = +22 °C; $t_{E/W}$ = 5 ms	–	–	100 000	
	PCA8582F-2	T_{amb} = 125 °C; $t_{E/W}$ = 4 to 10 ms	–	–	50 000	
		T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	–	–	100 000	
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	–	–	500 000	

I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).
Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.

Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes,
transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.
The PCx8582x-2 operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig.3). For the PCx8582x-2 this is fixed as 1010.

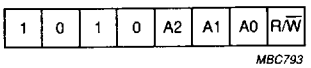


Fig.3 Slave address.

The next three significant bits address a particular device. A system could have up to eight PCx8582x-2 devices on the bus. The eight addresses are defined by the state of the A0, A1 and A2 inputs.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.
Address inputs must be connected either to V_{DD} or V_{SS}.

WRITE OPERATIONS

Byte/word write

For a write operation the PCx8582x-2 requires a second address field. This address field is a word address providing access to any one of the 256 words of memory. Upon receipt of the word address the PCx8582x-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 10 ms per byte.
During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCx8582x-2 is capable of a eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCx8582x-2 will respond with an acknowledge.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

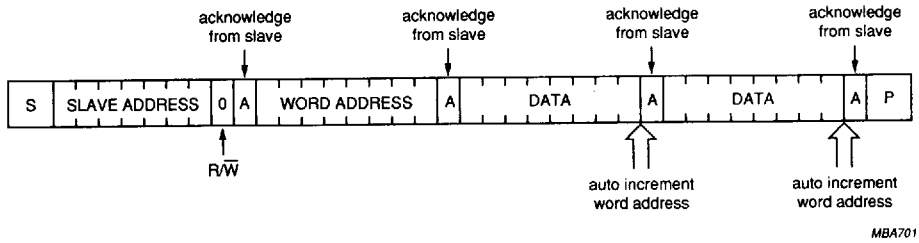


Fig.4 Auto increment memory word address; two byte write.

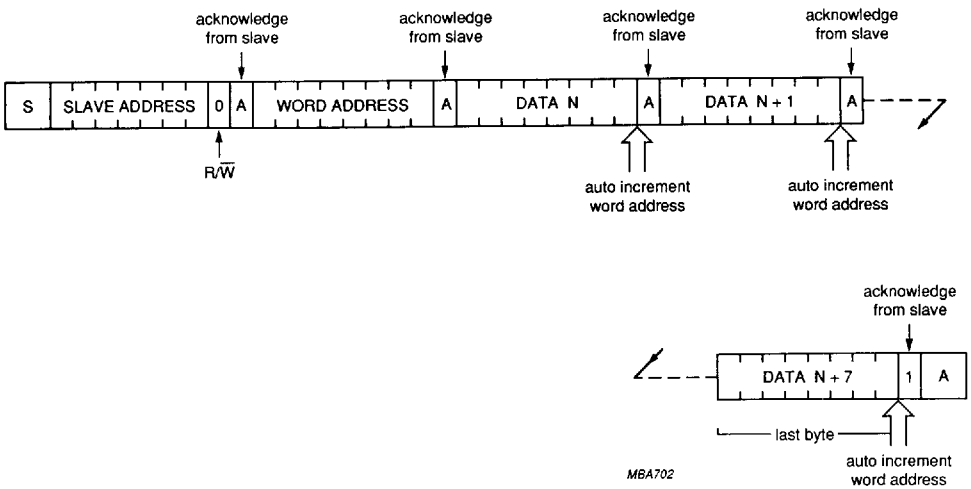


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

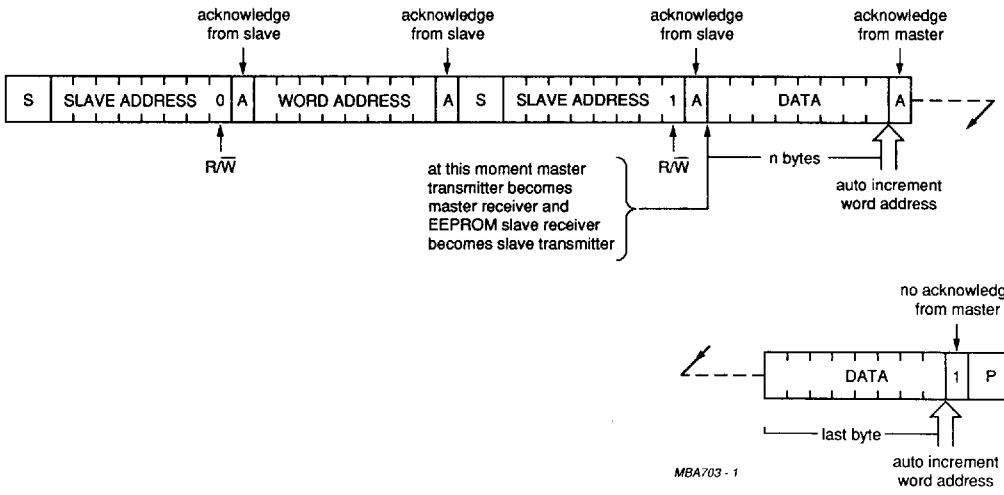


Fig.6 Master reads PCx8582x-2 slave after setting word address (WRITE word address; READ data).

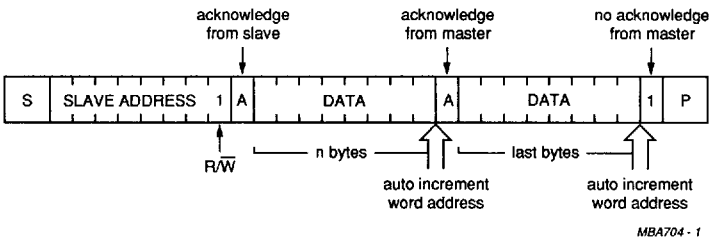


Fig.7 Master reads PCx8582x-2 immediately after first byte (READ mode).

I²C-BUS TIMING

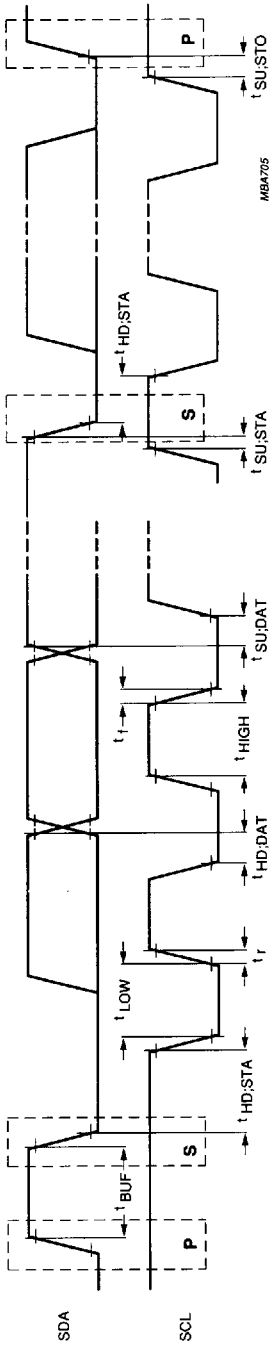


Fig.8 Timing requirements for the I²C-bus.

I²C-BUS CHARACTERISTICS

All of the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing from V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{SCL}	clock frequency		0	–	100	kHz
t_{BUF}	time the bus must be free before new transmission can start		4.7	–	–	µs
$t_{HD;STA}$	start condition hold time after which first clock pulse is generated		4	–	–	µs
t_{LOW}	LOW level clock period		4.7	–	–	µs
t_{HIGH}	HIGH level clock period		4	–	–	µs
$t_{SU;STA}$	set up time for start condition	repeated start	4.7	–	–	µs
$t_{HD;DAT}$	data hold time for bus compatible masters		5	–	–	µs
$t_{HD;DAT}$	data hold time for bus devices	note 2	0	–	–	ns
$t_{SU;DAT}$	data set up time		250	–	–	ns
t_r	SDA and SCL rise time		–	–	1	µs
t_f	SDA and SCL fall time		–	–	300	ns
$t_{SU;STO}$	set up time for stop condition		4.7	–	–	µs

Note to the characteristics

1. The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be provided internally by a transmitter.

EXTERNAL CLOCK TIMING

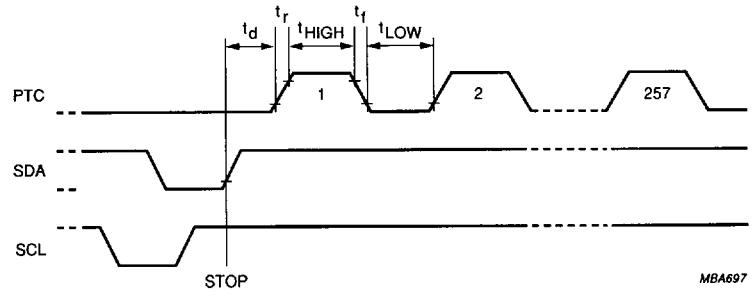


Fig.9 One byte ERASE/WRITE cycle.

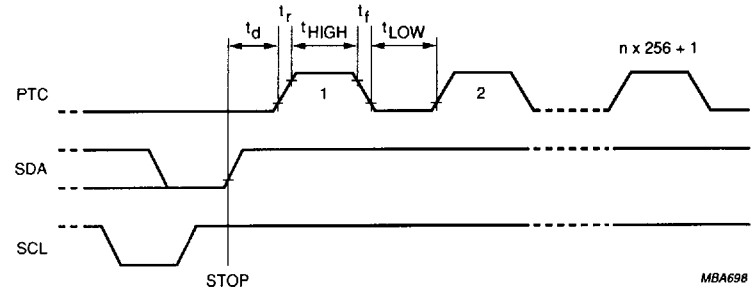


Fig.10 n byte ERASE/WRITE cycle (n = 2 to 7).

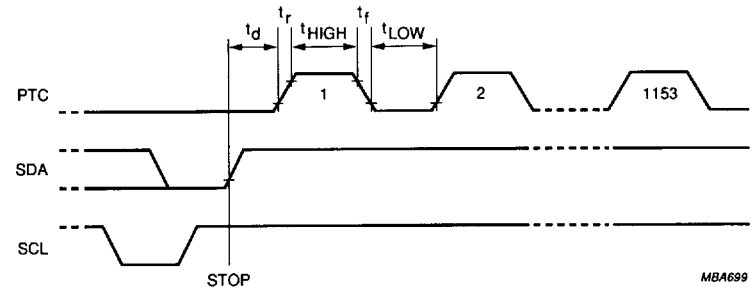
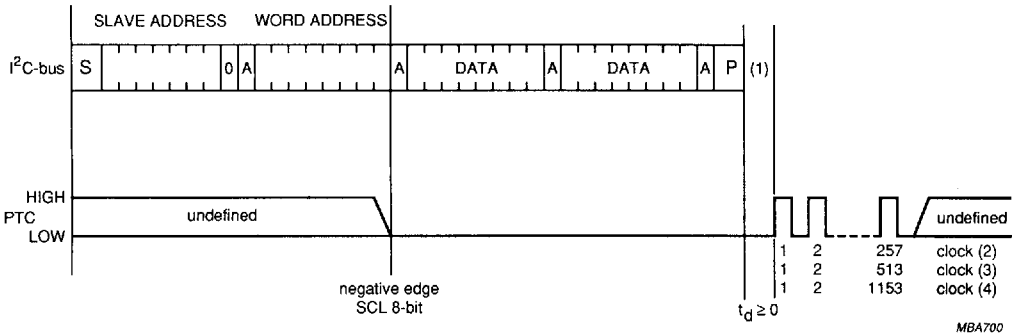


Fig.11 Page mode.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eighth bit of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8-byte) programming.

Fig.12 External clock.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.