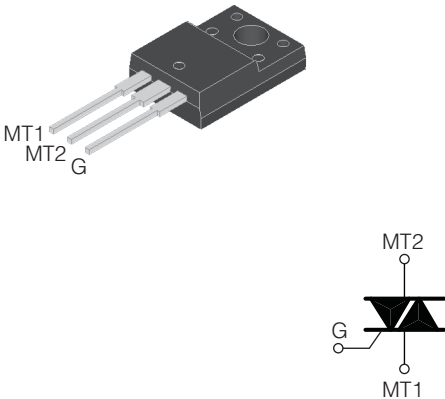


LOGIC LEVEL TRIAC

TO220-F (FULLY ISOLATED CASE) 	<table> <tr> <td>On-State Current 16 Amp</td><td>Gate Trigger Current < 10 mA</td></tr> <tr> <td colspan="2">Off-State Voltage 200 V ÷ 800 V</td></tr> <tr> <td colspan="2"> This series of TRIACs uses a high performance PNP technology. These parts are intended for general purpose AC switching applications with highly inductive loads. </td></tr> </table>	On-State Current 16 Amp	Gate Trigger Current < 10 mA	Off-State Voltage 200 V ÷ 800 V		This series of TRIACs uses a high performance PNP technology. These parts are intended for general purpose AC switching applications with highly inductive loads.	
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Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 95\text{ }^{\circ}\text{C}$	16	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 60 Hz ($t = 16.7\text{ ms}$)	176	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 50 Hz ($t = 20\text{ ms}$)	160	A
I^2t	Fusing Current	$t_p = 10\text{ ms}$, Half Cycle	128	A^2s
I_{GM}	Peak Gate Current	$20\text{ }\mu\text{s max.}$ $T_j = 125\text{ }^{\circ}\text{C}$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125\text{ }^{\circ}\text{C}$	1	W
di/dt	Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ ns}$ $f = 120\text{ Hz}$, $T_j = 125\text{ }^{\circ}\text{C}$	50	$\text{A}/\mu\text{s}$
T_j	Operating Temperature		$(-40 + 125)$	$^{\circ}\text{C}$
T_{stg}	Storage Temperature		$(-40 + 150)$	$^{\circ}\text{C}$
T_{sld}	Soldering Temperature	10s max	260	$^{\circ}\text{C}$
V_{iso}	R.M.S. isolation voltage 50/60 Hz sinusoidal waveform		2.500	Vac

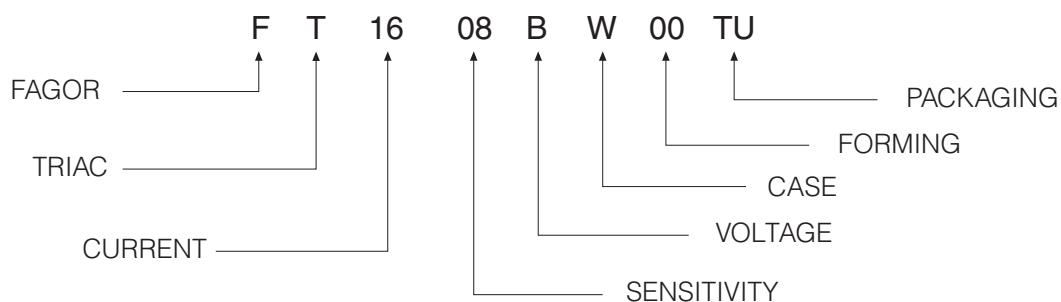
SYMBOL	PARAMETER	VOLTAGE					Unit
		B	D	M	S	N	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	200	400	600	700	800	V

LOGIC LEVEL TRIAC
Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY		Unit
					08	09	
$I_{GT}^{(1)}$	Gate Trigger Current	$V_D = 12 V_{DC}$, $R_L = 33\Omega$, $T_j = 25^\circ C$	Q1÷Q3 Q4	MAX MAX	10	10 10	mA mA
V_{GT}	Gate Trigger Voltage	$V_D = 12 V_{DC}$, $R_L = 33\Omega$, $T_j = 25^\circ C$	Q1÷Q3 Q1÷Q4	MAX MAX	1.3	1.3	V V
V_{GD}	Gate Non Trigger Voltage	$V_D = V_{DRM}$, $R_L = 3.3 K\Omega$, $T_j = 125^\circ C$	Q1÷Q3 Q1÷Q4	MIN MIN	0.2	0.2	V V
$I_H^{(2)}$	Holding Current	$I_T = 100$ mA, Gate open, $T_j = 25^\circ C$		MAX	15	20	mA
I_L	Latching Current	$I_G = 1.2 I_{GT}$, $T_j = 25^\circ C$	Q1,Q3 Q1,Q3,Q4 Q2	MAX MAX MAX	25	20 25	mA mA mA
$dV/dt^{(2)}$	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}$, Gate open $T_j = 125^\circ C$		MIN	40	50	V/ μs
$(dI/dt)^{(2)}$	Critical Rate of Current Rise	$(dv/dt)_c = 0.1$ V/ μs $T_j = 125^\circ C$ $(dv/dt)_c = 10$ V/ μs $T_j = 125^\circ C$ without snubber $T_j = 125^\circ C$		MIN MIN MIN	8.5 3.0	2.5 1.5	A/ms A/ms
$V_{TM}^{(2)}$	On-state Voltage	$I_T = 22.5$ Amp, $t_p = 380 \mu s$, $T_j = 25^\circ C$		MAX	1.55		V
$V_{t(o)}^{(2)}$	Threshold Voltage	$T_j = 125^\circ C$		MAX	0.77		V
$r_d^{(2)}$	Dynamic resistance	$T_j = 125^\circ C$		MAX	30		m Ω
I_{DRM}/I_{RRM}	Off-State Leakage Current	$V_D = V_{DRM}$, $T_j = 125^\circ C$ $V_R = V_{RRM}$, $T_j = 25^\circ C$		MAX MAX	2 5		mA μA
$R_{th(j-c)}$	Thermal Resistance Junction-Case	for AC 360° conduction angle			2.7		°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Ambient	$S = 1$ cm ²			50		°C/W

(1) Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

PART NUMBER INFORMATION


LOGIC LEVEL TRIAC

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle)

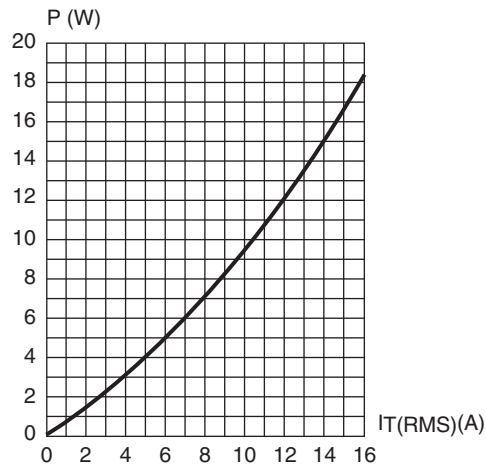


Fig. 2: RMS on-state current versus case temperature (full cycle).

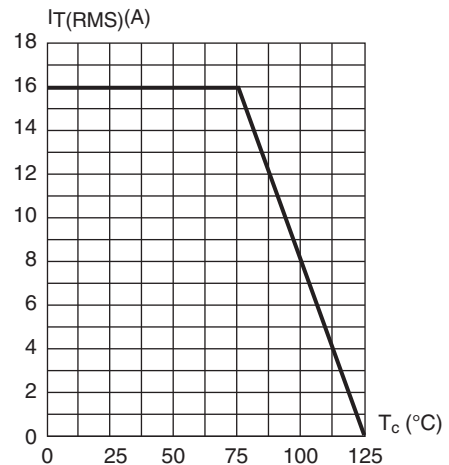


Fig. 3: Relative variation of thermal impedance versus pulse duration.

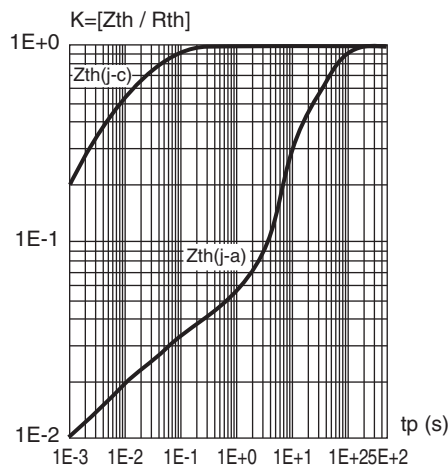


Fig. 5: Surge peak on-state current versus number of cycles

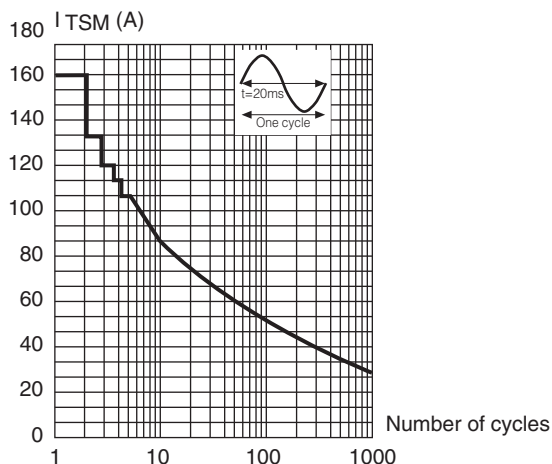


Fig. 4: On-state characteristics (maximum values)

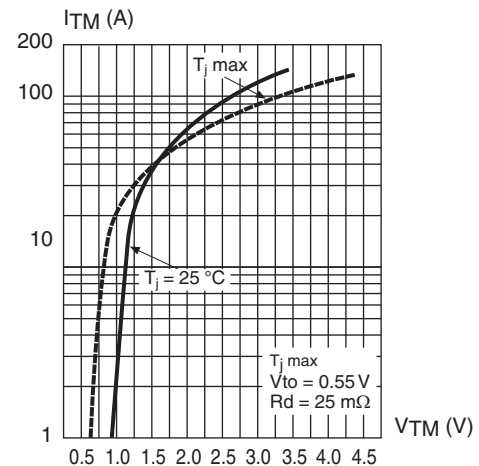
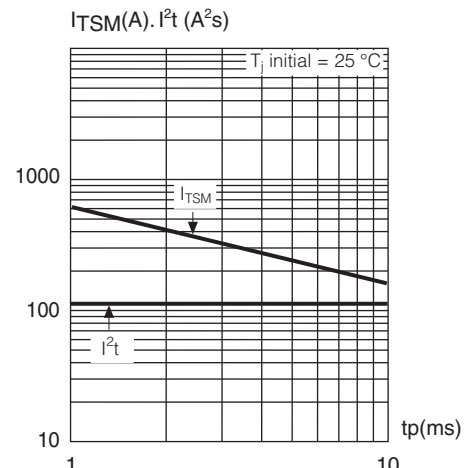


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: $t_p < 10$ ms, and corresponding value of $I^2 t$.



LOGIC LEVEL TRIAC

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

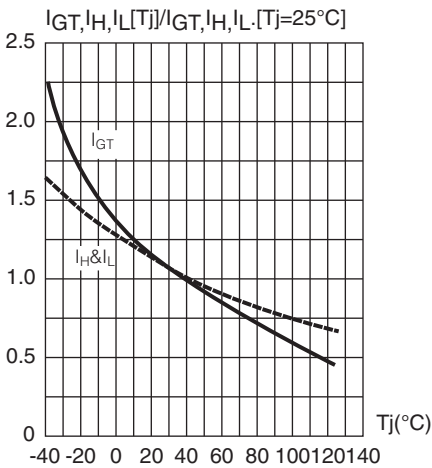


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

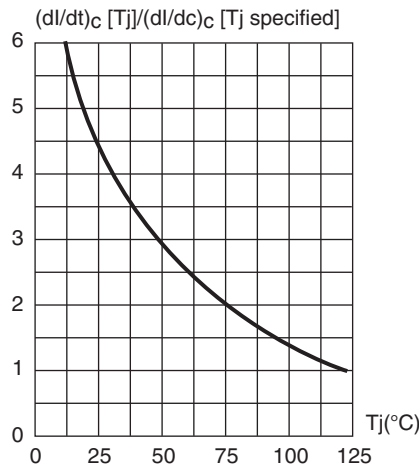
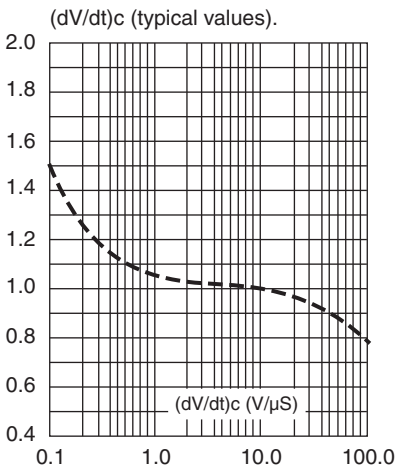
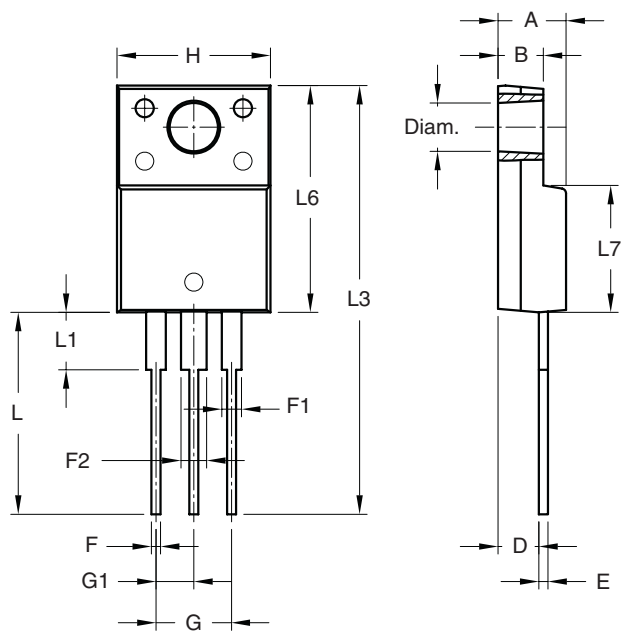


Fig. 9: Relative variation of critical rate of decrease of main current versus



PACKAGE MECHANICAL DATA

TO220-F



REF.	DIMENSIONS		
	Milimeters		
	Min.	Nominal	Max.
A	3.55	4.50	4.90
B	2.34	3.00	3.70
D	2.03	2.70	2.96
E	0.35	0.60	0.70
F	0.25	0.60	1.01
F1	0.70	1.30	1.78
F2	0.70	1.70	1.78
G	4.88	5.00	5.28
G1	2.34	2.50	2.74
H	9.65	10.15	10.67
L	12.70	13.35	14.73
L1	2.93	3.75	6.35
L3	26.90	28.35	31.20
L6	14.22	15.00	16.50
L7	8.30	8.40	9.59
Diam.	3.00	3.20	3.28