

# Am2909A/Am2911A

Microprogram Sequencers

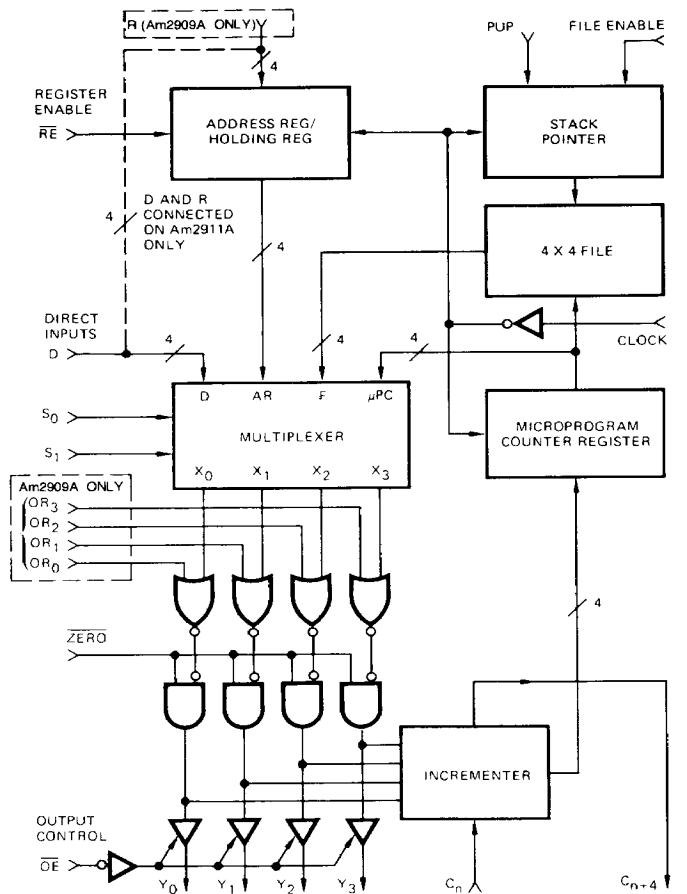
Am2909A/Am2911A

Advanced Micro Devices

## DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to form longer word width
- Branch input for N-way branches
- 4 x 4 file with stack pointer and push/pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909A only)
- Am2909A in 28-pin package & Am2911A in 20-pin package

## MICROPROGRAM SEQUENCER BLOCK DIAGRAM



BD002172

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|------------------------|------|-----------|
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## GENERAL DESCRIPTION

The Am2909A is a 4-bit wide sequencer intended for sequencing through a series of microinstructions contained in memory. Two Am2909As may be interconnected to generate an 8-bit address (256 words), and three may be used to generate a 12-bit address (4K words).

The Am2909A can select an address from any of four sources: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a 4-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack

includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeros; the outputs are three-state.

The Am2911A is an identical circuit to the Am2909A, except the four OR inputs and the R inputs are removed and the D inputs connect to the ADDRESS REG/HOLDING REG. The Am2911A is in a 20-pin, 0.3" centers package.

## RELATED AMD PRODUCTS

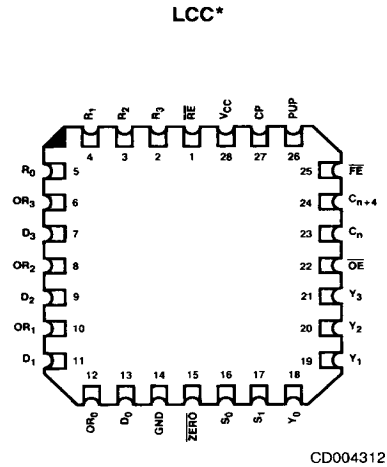
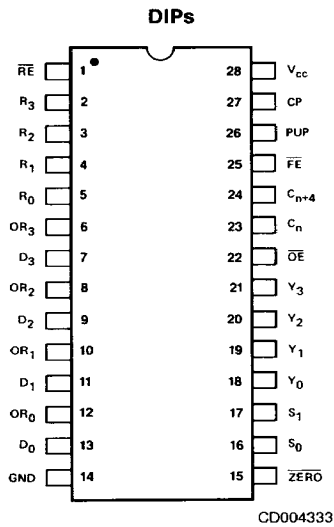
| Part No.  | Description                |
|-----------|----------------------------|
| Am2918    | Pipeline Register          |
| Am2922    | Condition Code MUX         |
| Am29803A  | 16-Way Branch Control Unit |
| Am29811A  | Next Address Control       |
| Am25LS163 | 4-Bit Counter              |
| Am27S35   | Registered PROM            |

For applications information, see Chapter 11 of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

## CONNECTION DIAGRAMS

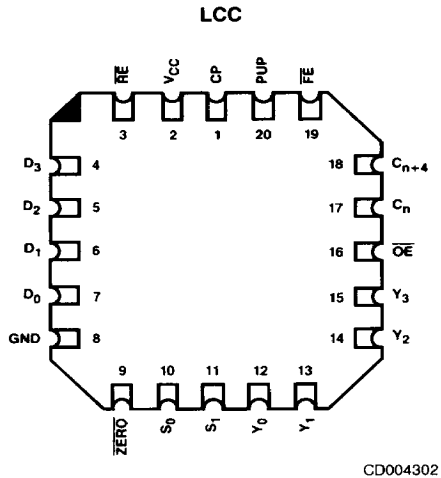
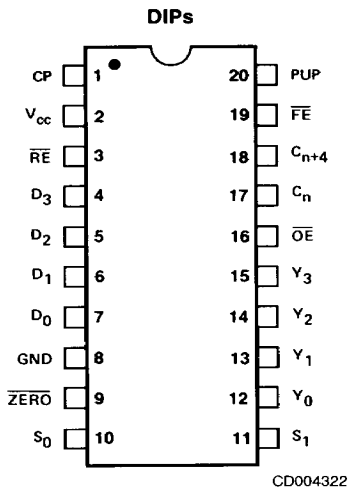
### Top View

#### Am2909A



\*Am2909A is also available in a 28-Pin Ceramic Flatpack; pinout is identical to the LCC.

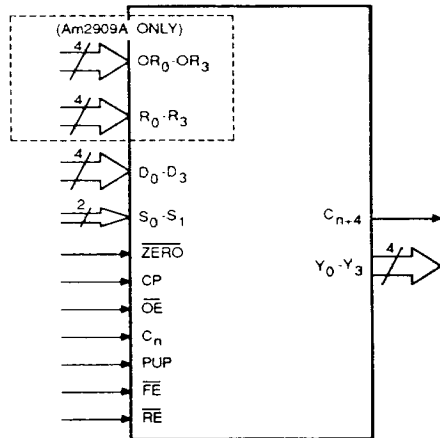
#### Am2911A



Note: Pin 1 is marked for orientation.

# LOGIC SYMBOL

## Am2909A/Am2911A



$V_{CC}$  = Power Supply  
 $GND$  = Ground

LS003110

## Am2909A ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- Device Number**
- Speed Option** (if applicable)
- Package Type**
- Temperature Range**
- Optional Processing**

AM2909A

D

C

B

**e. OPTIONAL PROCESSING**

Blank = Standard processing  
B = Burn-in

**d. TEMPERATURE RANGE**

C = Commercial (0 to +70°C)  
M = Military\* (-55 to +125°C)

**c. PACKAGE TYPE**

P = 28-Pin Plastic DIP (PD 028)  
D = 28-Pin Ceramic DIP (CD 028)  
X = Dice

**b. SPEED OPTION**

Not Applicable

**a. DEVICE NUMBER/DESCRIPTION**

Am2909A  
Microprogram Sequencer

| Valid Combinations |                        |
|--------------------|------------------------|
| AM2909A            | PC, DC, DCB,<br>XC, XM |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

\*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

## Am2909A MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**

AM2909A

/B

X

A

**e. LEAD FINISH**

A = Hot Solder Dip

**d. PACKAGE TYPE**

X = 28-Pin Ceramic DIP (CD 028)

Y = 28-Pin Ceramic Flatpack (CFM028)

3 = 28-Pin Ceramic Leadless Chip Carrier (CLT028)

**c. DEVICE CLASS**

/B = Class B

**b. SPEED OPTION**

Not Applicable

**a. DEVICE NUMBER/DESCRIPTION**

Am2909A

Microprogram Sequencer

| Valid Combinations |                  |
|--------------------|------------------|
| AM2909A            | /BXA, /BYA, /B3A |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups

1, 2, 3, 7, 8, 9, 10, 11.

## Am2911A ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**

AM2911A

D

C

B

**e. OPTIONAL PROCESSING**

Blank = Standard processing  
B = Burn-in

**d. TEMPERATURE RANGE**

C = Commercial (0 to +70°C)  
M = Military\* (-55 to +125°C)

**c. PACKAGE TYPE**

P = 20-Pin Plastic DIP (PD 020)  
D = 20-Pin Ceramic DIP (CD 020)  
X = Dice

**b. SPEED OPTION**

Not Applicable

**a. DEVICE NUMBER/DESCRIPTION**

Am2911A  
Microprogram Sequencer

| Valid Combinations |                        |
|--------------------|------------------------|
| AM2911A            | PC, DC, DCB,<br>XC, XM |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

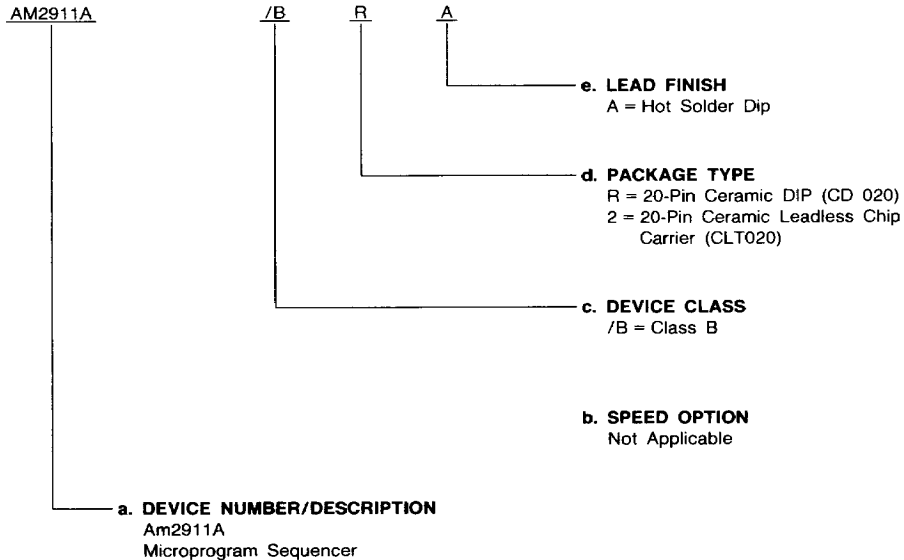
\*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

## Am2911A MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number**
- b. Speed Option** (if applicable)
- c. Device Class**
- d. Package Type**
- e. Lead Finish**



| Valid Combinations |            |
|--------------------|------------|
| AM2911A            | /BRA, /B2A |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups  
1, 2, 3, 7, 8, 9, 10, 11.



## PIN DESCRIPTION

### Am2909A/Am2911A

**C<sub>n</sub> Carry In (Input)**

Carry input to the incrementer.

**C<sub>n</sub> + 4 Carry Out (Output)**

Carry out from the incrementer.

**CP Clock Pulse (Input)**

Clock input to the AR and  $\mu$ PC register and push/pop stack.

**D<sub>0-3</sub> Direct Input (Input)**

Direct input to the multiplexer.

**FE File Enable (Input; Active LOW)**

Used along with PUP to control the push/pop stack.

**OE Output Enable (Input; Three State, Active LOW)**

Three-state control of Y<sub>i</sub> outputs.

**PUP Push/Pop (Input)**

Used along with FE to control the push/pop stack.

**RE Register Load Enable (Input; Active LOW)**

Enable input for internal address register.

**S<sub>0</sub>, S<sub>1</sub> Source (Input)**

Control inputs to the multiplexer that select the source of the next microinstruction address.

**Y<sub>0-3</sub> Address (Output; Three State)**

Address outputs.

**ZERO Zero (Input; Active LOW)**

Forces the four Y outputs to binary zero (except when  $\overline{OE}$  is HIGH).

**Am2909A Only****OR<sub>0-3</sub> Logic OR (Input)**

Logic-OR inputs on each address output line.

**R<sub>0-3</sub> Register Input (Input)**

Inputs to the internal address register.

## FUNCTIONAL DESCRIPTION

### Architecture of the Am2909A/Am2911A

The Am2909A/Am2911A are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256 words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 1.

The device contains a 4-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S<sub>0</sub> and S<sub>1</sub> inputs.

The address register consists of four D-type, edge-triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a 4-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911A, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909A/Am2911A contains a microprogram counter ( $\mu$ PC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C<sub>n</sub>) and carry-out (C<sub>n</sub> + 4) such that cascading to larger word lengths is straightforward. The  $\mu$ PC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word, plus one (Y + 1 -  $\mu$ PC); thus sequential microinstructions can be executed. If this least significant C<sub>n</sub> is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y -  $\mu$ PC). Thus, the same microinstruction can be executed any number of times by using the least significant C<sub>n</sub> as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the push operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage — the next microinstruction address following the subroutine jump which initiated the push.

If the file enable input is LOW and the push/pop control is LOW, a pop operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops, or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is four words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs except OE. In the Am2909A, each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The Am2909A/Am2911A feature three-state Y outputs. These can be particularly useful in designs requiring external equipment to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

## Operation of the Am2909A/Am2911A

Figure 2 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 1 also shows the truth table for the output control and

for the control of the push/pop stack. Figure 2 shows in detail the effect of  $S_0$ ,  $S_1$ ,  $\overline{FE}$  and PUP on the Am2909A. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain  $R_a$  through  $R_d$ .

### Address Selection

| $S_1$ | $S_0$ | Source for Y Outputs     | Symbol   |
|-------|-------|--------------------------|----------|
| L     | L     | Microprogram Counter     | $\mu PC$ |
| L     | H     | Address/Holding Register | AR       |
| H     | L     | Push-Pop stack           | STK0     |
| H     | H     | Direct inputs            | $D_i$    |

### Output Control

| $OR_i^*$ | ZERO | $\overline{OE}$ | $Y_i$                        |
|----------|------|-----------------|------------------------------|
| X        | X    | H               | Z                            |
| X        | L    | L               | L                            |
| H        | H    | L               | H                            |
| L        | H    | L               | Source selected by $S_0 S_1$ |

Z = High Impedance

\*Am2909A only.

### Synchronous Stack Control

| $\overline{FE}$ | PUP | Push/Pop Stack Change                                   |
|-----------------|-----|---------------------------------------------------------|
| H               | X   | No change                                               |
| L               | H   | Increment stack pointer, then push current PC onto STK0 |
| L               | L   | Pop stack (decrement stack pointer)                     |

H = High

L = Low

X = Don't Care

Figure 1. Multiplexer Select Codes

| Cycle    | $S_1, S_0, \overline{FE}, PUP$ | $\mu PC$     | REG    | STK0           | STK1           | STK2           | STK3           | $Y_{OUT}$  | Comment                                   | Principle Use    |
|----------|--------------------------------|--------------|--------|----------------|----------------|----------------|----------------|------------|-------------------------------------------|------------------|
| N<br>N+1 | L L L L<br>—                   | J<br>J+1     | K<br>K | $R_a$<br>$R_b$ | $R_b$<br>$R_c$ | $R_c$<br>$R_d$ | $R_d$<br>$R_a$ | J<br>—     | Pop Stack                                 | End Loop         |
| N<br>N+1 | L L L H<br>—                   | J<br>J+1     | K<br>K | $R_a$<br>J     | $R_b$<br>$R_a$ | $R_c$<br>$R_b$ | $R_d$<br>$R_c$ | J<br>—     | Push $\mu PC$                             | Set-up Loop      |
| N<br>N+1 | L L H X<br>—                   | J<br>J+1     | K<br>K | $R_a$<br>$R_a$ | $R_b$<br>$R_b$ | $R_c$<br>$R_c$ | $R_d$<br>$R_d$ | J<br>—     | Continue                                  | Continue         |
| N<br>N+1 | L H L L<br>—                   | J<br>K+1     | K<br>K | $R_a$<br>$R_b$ | $R_b$<br>$R_c$ | $R_c$<br>$R_d$ | $R_d$<br>$R_a$ | K<br>—     | Pop Stack;<br>Use AR for Address          | End Loop         |
| N<br>N+1 | L H L H<br>—                   | J<br>K+1     | K<br>K | $R_a$<br>J     | $R_b$<br>$R_a$ | $R_c$<br>$R_b$ | $R_d$<br>$R_c$ | K<br>—     | Push $\mu PC$ ;<br>Jump to Address in AR  | JSR AR           |
| N<br>N+1 | L H H X<br>—                   | J<br>K+1     | K<br>K | $R_a$<br>$R_a$ | $R_b$<br>$R_b$ | $R_c$<br>$R_c$ | $R_d$<br>$R_d$ | K<br>—     | Jump to Address in AR                     | JMP AR           |
| N<br>N+1 | H L L L<br>—                   | J<br>$R_a+1$ | K<br>K | $R_a$<br>$R_b$ | $R_b$<br>$R_c$ | $R_c$<br>$R_d$ | $R_d$<br>$R_a$ | $R_a$<br>— | Jump to Address in STK0;<br>Pop Stack     | RTS              |
| N<br>N+1 | H L L H<br>—                   | J<br>$R_a+1$ | K<br>K | $R_a$<br>J     | $R_b$<br>$R_a$ | $R_c$<br>$R_b$ | $R_d$<br>$R_c$ | $R_a$<br>— | Jump to Address in STK0;<br>Push $\mu PC$ |                  |
| N<br>N+1 | H L H X<br>—                   | J<br>$R_a+1$ | K<br>K | $R_a$<br>$R_a$ | $R_b$<br>$R_b$ | $R_c$<br>$R_c$ | $R_d$<br>$R_d$ | $R_a$<br>— | Jump to Address in STK0                   | Stack Ref (Loop) |
| N<br>N+1 | H H L L<br>—                   | J<br>D+1     | K<br>K | $R_a$<br>$R_b$ | $R_b$<br>$R_c$ | $R_c$<br>$R_d$ | $R_d$<br>$R_a$ | D<br>—     | Pop Stack;<br>Jump to Address on D        | End Loop         |
| N<br>N+1 | H H L H<br>—                   | J<br>D+1     | K<br>K | $R_a$<br>J     | $R_b$<br>$R_a$ | $R_c$<br>$R_b$ | $R_d$<br>$R_c$ | D<br>—     | Jump to Address on D;<br>Push $\mu PC$    | JSR D            |
| N<br>N+1 | H H H X<br>—                   | J<br>D+1     | K<br>K | $R_a$<br>$R_a$ | $R_b$<br>$R_b$ | $R_c$<br>$R_c$ | $R_d$<br>$R_d$ | D<br>—     | Jump to Address on D                      | JMP D            |

X = Don't care, 0 = LOW, 1 = HIGH, Assume  $C_n$  = HIGH

Note: STK0 is the location addressed by the stack pointer.

Figure 2. Output and Internal Next-Cycle Register States for Am2909A/Am2911A

Figure 3 illustrates the execution of a subroutine using the Am2909A. The configuration of Figure 6 is assumed. The instruction being executed at any given time is the one contained in the microword register ( $\mu$ WR). The contents of the  $\mu$ WR also control (indirectly, perhaps) the four signals  $S_0$ ,  $S_1$ ,  $FE$ , and  $PUP$ . The starting address of the subroutine is applied to the D inputs of the Am2909A at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to subroutine at A". At the time  $T_2$ , this instruction is in the  $\mu$ WR,

and the Am2909A inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the  $\mu$ WR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the  $\mu$ WR. On the next clock transition, I(A) is loaded into the  $\mu$ WR for execution, and the return address J + 3 is pushed onto the stack. The return instruction is executed at  $T_5$ . Figure 4 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

### Control Memory

| Execute Cycle | Microprogram |                       |
|---------------|--------------|-----------------------|
|               | Address      | Sequencer Instruction |
| $T_0$         | J - 1        | -                     |
| $T_1$         | J            | -                     |
| $T_2$         | J + 1        | -                     |
| $T_6$         | J + 2        | JSR A                 |
| $T_7$         | J + 3        | -                     |
|               | J + 4        | -                     |
|               | -            | -                     |
|               | -            | -                     |
|               | -            | -                     |
|               | -            | -                     |
| $T_3$         | A            | I(A)                  |
| $T_4$         | A + 1        | -                     |
| $T_5$         | A + 2        | RTS                   |
|               | -            | -                     |
|               | -            | -                     |
|               | -            | -                     |
|               | -            | -                     |
|               | -            | -                     |

| Execute Cycle                                     |                                          | $T_0$                     | $T_1$                     | $T_2$                     | $T_3$                    | $T_4$                    | $T_5$                    | $T_6$                | $T_7$                | $T_8$ | $T_9$ |
|---------------------------------------------------|------------------------------------------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|----------------------|----------------------|-------|-------|
| Clock Signals                                     |                                          |                           |                           |                           |                          |                          |                          |                      |                      |       |       |
| Am2909A Inputs (from $\mu$ WR)                    | $S_1, S_0$<br>$FE$<br>$PUP$<br>$D$       | 0<br>H<br>X<br>X          | 0<br>H<br>X<br>X          | 3<br>L<br>H<br>A          | 0<br>H<br>X<br>X         | 0<br>H<br>X<br>X         | 2<br>L<br>X<br>X         | 0<br>H<br>X<br>X     | 0<br>H<br>X<br>X     |       |       |
| Internal Registers                                | $\mu$ PC<br>STK0<br>STK1<br>STK2<br>STK3 | J + 1<br>-<br>-<br>-<br>- | J + 2<br>-<br>-<br>-<br>- | J + 3<br>-<br>-<br>-<br>- | A + 1<br>J + 3<br>-<br>- | A + 2<br>J + 3<br>-<br>- | A + 3<br>J + 3<br>-<br>- | J + 4<br>-<br>-<br>- | J + 5<br>-<br>-<br>- |       |       |
| Am2909A Output                                    | Y                                        | J + 1                     | J + 2                     | A                         | A + 1                    | A + 2                    | J + 3                    | J + 4                | J + 5                |       |       |
| ROM Output                                        | (Y)                                      | I(J + 1)                  | JSR A                     | I(A)                      | I(A + 1)                 | RTS                      | I(J + 3)                 | I(J + 4)             | I(J + 5)             |       |       |
| Contents of $\mu$ WR (Instruction being executed) | $\mu$ WR                                 | I(J)                      | I(J + 1)                  | JSR A                     | I(A)                     | I(A + 1)                 | RTS                      | I(J + 3)             | I(J + 4)             |       |       |

$C_N = \text{HIGH}$

Figure 3. Subroutine Execution

### Control Memory

| Execute Cycle | Microprogram |                       |
|---------------|--------------|-----------------------|
|               | Address      | Sequencer Instruction |
| $T_0$         | J - 1        | -                     |
| $T_1$         | J            | -                     |
| $T_2$         | J + 1        | -                     |
| $T_9$         | J + 2        | JSR A                 |
|               | J + 3        | -                     |
|               | -            | -                     |
|               | -            | -                     |
|               | -            | -                     |
| $T_3$         | A            | -                     |
| $T_4$         | A + 1        | -                     |
| $T_5$         | A + 2        | JSR B                 |
| $T_7$         | A + 3        | -                     |
| $T_8$         | A + 4        | RTS                   |
|               | -            | -                     |
|               | -            | -                     |
| $T_6$         | B            | RTS                   |
|               | -            | -                     |
|               | -            | -                     |

| Execute Cycle                                     |                                          | $T_0$                     | $T_1$                     | $T_2$                     | $T_3$                    | $T_4$                    | $T_5$                    | $T_6$                   | $T_7$               | $T_8$               | $T_9$            |
|---------------------------------------------------|------------------------------------------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|--------------------------|-------------------------|---------------------|---------------------|------------------|
| Clock Signals                                     |                                          |                           |                           |                           |                          |                          |                          |                         |                     |                     |                  |
| Am2909A Inputs (from $\mu$ WR)                    | $S_1, S_0$<br>$FE$<br>$PUP$<br>$D$       | 0<br>H<br>X<br>X          | 0<br>H<br>X<br>X          | 3<br>L<br>H<br>A          | 0<br>H<br>X<br>X         | 0<br>H<br>X<br>X         | 3<br>L<br>H<br>B         | 2<br>L<br>L<br>X        | 0<br>H<br>X<br>X    | 2<br>L<br>L<br>X    | 0<br>H<br>X<br>X |
| Internal Registers                                | $\mu$ PC<br>STK0<br>STK1<br>STK2<br>STK3 | J + 1<br>-<br>-<br>-<br>- | J + 2<br>-<br>-<br>-<br>- | J + 3<br>-<br>-<br>-<br>- | A + 1<br>J + 3<br>-<br>- | A + 2<br>J + 3<br>-<br>- | A + 3<br>J + 3<br>-<br>- | B + 1<br>A + 3<br>J + 3 | A + 4<br>J + 3<br>- | A + 5<br>J + 3<br>- | J + 4<br>-<br>-  |
| Am2909A Output                                    | Y                                        | J + 1                     | J + 2                     | A                         | A + 1                    | A + 2                    | B                        | A + 3                   | A + 4               | J + 3               | J + 4            |
| ROM Output                                        | (Y)                                      | I(J + 1)                  | JSR A                     | I(A)                      | I(A + 1)                 | JSR B                    | RTS                      | I(A + 3)                | RTS                 | I(J + 3)            | I(J + 4)         |
| Contents of $\mu$ WR (Instruction being executed) | $\mu$ WR                                 | I(J)                      | I(J + 1)                  | JSR A                     | I(A)                     | I(A + 1)                 | JSR B                    | RTS                     | I(A + 3)            | RTS                 | I(J + 3)         |

$C_N = \text{HIGH}$

Figure 4. Two Nested Subroutines (Routine B is Only One Instruction)

## Using the Am2909A and Am2911A

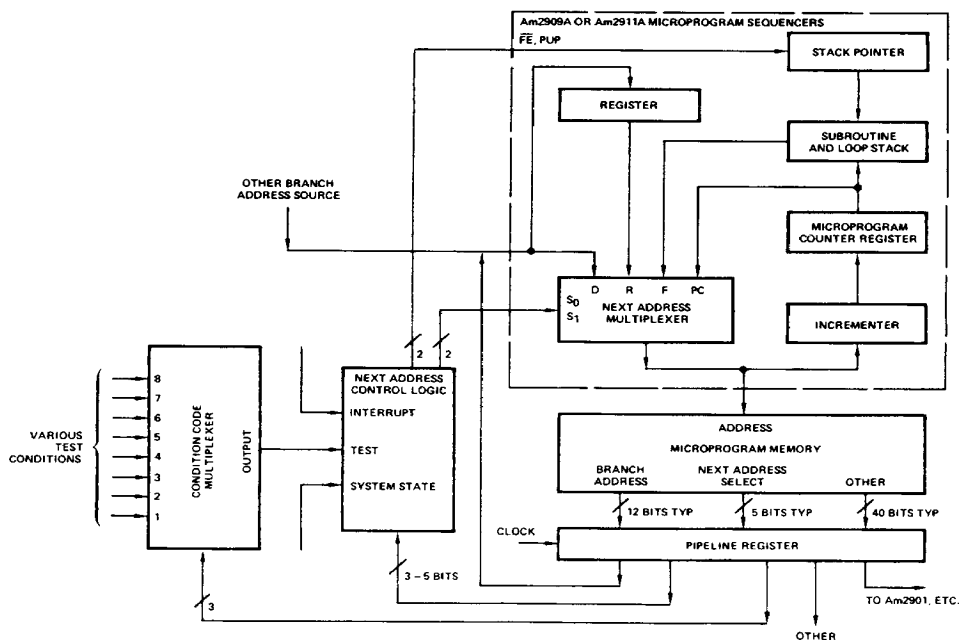
The Am2909A and Am2911A are 4-bit slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the Am2909A and Am2911A apart from the Am2910, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The Am2909A or Am2911A should be selected instead of the Am2910 under the following conditions:

- Address less than 8 bits and not likely to be expanded
- Address longer than 12 bits

- More complex instruction set needed than is available on Am2910

## Architecture of the Control Unit

The recommended architecture using the Am2909A or Am2911A is shown in Figure 5. Note that the path from the pipeline register output through the next address logic, multiplexer, and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return-from-subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the Am2909A or Am2911A. The block labeled "next address logic" may consist of simple gates, a PROM or a PLA, but it should be all combinational.



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**Figure 5. Recommended Computer Control Unit Architecture Using the Am2911A or Am2909A**

also controls a loop counter and several branch address sources. The instructions which are implemented by the Am29811A are shown in Figure 7, along with the Am29811A outputs for each instruction. Generating any instruction set consists simply of writing a truth table and designing combinational logic to implement it. For more detailed information refer to "The Microprogramming Handbook".

Figure 6 shows the CCU of Figure 5 with the Am29811A in place. The Am29811A, in addition to controlling the Am2911A,



**Figure 6. A Typical Computer Control Unit Using the Am2911A and Am29811A**

## Expansion of the Am2909A or Am2911A

Figure 8 shows the interconnection of three Am2911As to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between  $\mu$ PC incrementors. This carry path is not in the critical speed path if the Am2911A Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a micro-address register is placed at the Am2911A output, then the carry may lie in the critical speed path, since the last carry-in must be stable for a setup time prior to the clock.

## Selecting Between the Am2909A and Am2911A

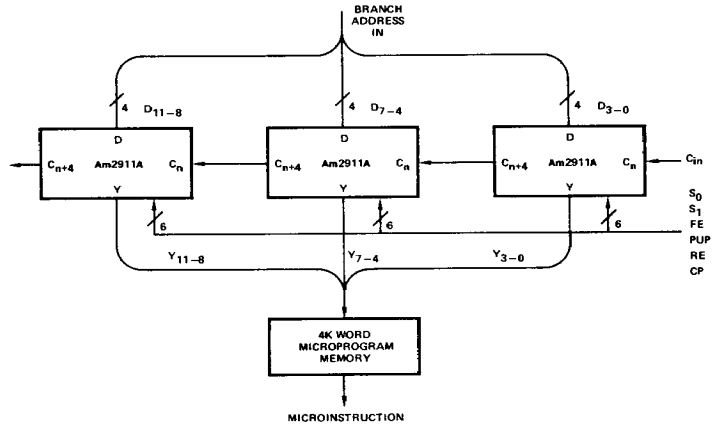
The difference between the Am2909A and the Am2911A involves two signals: the data inputs to the holding register

and the "OR" inputs. In the Am2909A, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the Am2911A, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 9. Using the Am2909A, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the Am2911A, it is more common to connect the Am2911A's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 9 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

| Mnemonic | Pin No.              | Inputs         |                |                |                |      | Outputs           |                |      |     |         |    |       |      |
|----------|----------------------|----------------|----------------|----------------|----------------|------|-------------------|----------------|------|-----|---------|----|-------|------|
|          |                      |                |                |                |                |      | Next ADDR. Source |                | File |     | Counter |    | MAP E | PL E |
|          |                      | I <sub>3</sub> | I <sub>2</sub> | I <sub>1</sub> | I <sub>0</sub> | TEST | S <sub>1</sub>    | S <sub>0</sub> | FE   | PUP | LOAD    | EN |       |      |
|          |                      | 14             | 13             | 12             | 11             | 10   | 4                 | 5              | 3    | 2   | 6       | 7  | 1     | 9    |
| JZ       | JUMP ZERO            | L              | L              | L              | L              | H    | H                 | H              | H    | H   | L       | L  | H     | L    |
| CJS      | CON JSB PL           | L              | L              | L              | H              | L    | L                 | L              | H    | H   | H       | H  | H     | L    |
| JMAP     | JUMP MAP             | L              | L              | H              | L              | L    | H                 | H              | H    | H   | H       | H  | L     | H    |
| CJP      | COND JUMP PL         | L              | L              | H              | H              | H    | L                 | L              | H    | H   | H       | H  | H     | L    |
| PUSH     | PUSH/COND LD CNTR    | L              | H              | L              | L              | L    | L                 | L              | L    | H   | H       | H  | H     | L    |
| JSRP     | COND JSB R/PL        | L              | H              | L              | H              | L    | L                 | H              | L    | H   | H       | H  | H     | L    |
| CVJ      | COND JUMP VECTOR     | L              | H              | H              | L              | L    | L                 | L              | H    | H   | H       | H  | H     | H    |
| JRP      | COND JUMP R/PL       | L              | H              | H              | H              | L    | L                 | H              | H    | H   | H       | H  | H     | L    |
| RFCT     | REPEAT LOOP, CTR # 0 | H              | L              | L              | L              | H    | L                 | L              | L    | L   | H       | H  | H     | L    |
| RPCT     | REPEAT PL, CTR # 0   | H              | L              | L              | H              | L    | H                 | H              | H    | H   | H       | L  | H     | L    |
| CRTN     | COND RTN             | H              | L              | H              | L              | L    | L                 | L              | H    | L   | H       | H  | H     | L    |
| CJPP     | COND JUMP PL & POP   | H              | L              | H              | H              | L    | L                 | H              | L    | L   | H       | H  | H     | L    |
| LDCT     | LD CNTR & CONTINUE   | H              | H              | L              | L              | L    | L                 | L              | H    | H   | L       | H  | H     | L    |
| LOOP     | TEST END LOOP        | H              | H              | L              | H              | L    | H                 | L              | L    | L   | H       | H  | H     | L    |
| CONT     | CONTINUE             | H              | H              | H              | L              | L    | L                 | L              | H    | H   | H       | H  | H     | L    |
| JP       | JUMP PL              | H              | H              | H              | H              | L    | H                 | H              | H    | H   | H       | H  | H     | L    |

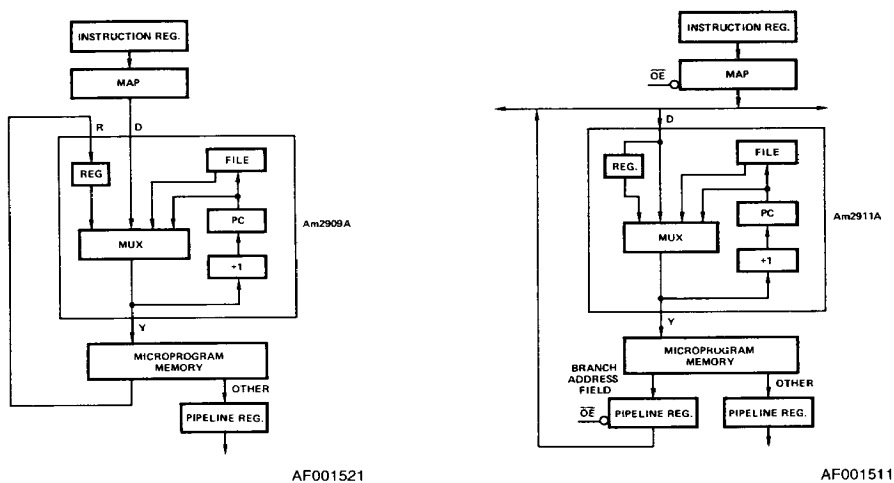
L = LOW  
H = HIGH

Figure 7. Am29811A Truth Table



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Figure 8. 12-Bit Sequencer



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AF001511

Figure 9. Branch Address Structures

## How to Perform Some Common Functions with the Am2909A or Am2911A

|                      |       |                |                |                |                 |     |
|----------------------|-------|----------------|----------------|----------------|-----------------|-----|
| MUX/Y <sub>OUT</sub> | STACK | C <sub>n</sub> | S <sub>1</sub> | S <sub>0</sub> | $\overline{FE}$ | PUP |
| PC                   | HOLD  | H              | L              | L              | H               | X   |

## 2. BRANCH

|                      |       |                |                |                |                 |     |
|----------------------|-------|----------------|----------------|----------------|-----------------|-----|
| MUX/Y <sub>OUT</sub> | STACK | C <sub>n</sub> | S <sub>1</sub> | S <sub>0</sub> | $\overline{FE}$ | PUP |
| D                    | HOLD  | H              | H              | H              | H               | X   |

### 3. JUMP-TO-SUBROUTINE

|                      |       |                |                |                |                 |     |
|----------------------|-------|----------------|----------------|----------------|-----------------|-----|
| MUX/Y <sub>OUT</sub> | STACK | C <sub>n</sub> | S <sub>1</sub> | S <sub>0</sub> | $\overline{FE}$ | PUP |
| D                    | PUSH  | H              | H              | H              | L               | H   |

#### 4. RETURN-FROM-SUBROUTINE

|                      |       |                |                |                |                 |     |
|----------------------|-------|----------------|----------------|----------------|-----------------|-----|
| MUX/Y <sub>OUT</sub> | STACK | C <sub>n</sub> | S <sub>1</sub> | S <sub>0</sub> | $\overline{FE}$ | PUP |
| STACK                | POP   | H              | H              | L              | L               | L   |

AF001610

Diagram illustrating the Am2903A block structure. The block is labeled "Am2903A". It has four inputs on the left labeled  $T_3$ ,  $T_2$ ,  $T_1$ , and  $T_0$ , grouped under the label "FOUR TEST CONDITIONS". It has four inputs on the top labeled  $i_3$ ,  $i_2$ ,  $i_1$ , and  $i_0$ . It has four outputs on the right labeled  $OR_3$ ,  $OR_2$ ,  $OR_1$ , and  $OR_0$ , grouped under the label "TO Am2909 A OR INPUTS".

**Figure 11-1. Am29803A Truth Table**

|                    | Branch On                                                         | I <sub>3</sub> | I <sub>2</sub> | I <sub>1</sub> | I <sub>0</sub> | OR <sub>3</sub> | OR <sub>2</sub> | OR <sub>1</sub> | OR <sub>0</sub> |
|--------------------|-------------------------------------------------------------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|
| NONE               | NONE                                                              | L              | L              | L              | L              | L               | L               | L               | L               |
| Two-way Branches   | T <sub>0</sub>                                                    | L              | L              | L              | H              | L               | L               | L               | T <sub>0</sub>  |
|                    | T <sub>1</sub>                                                    | L              | L              | H              | L              | L               | L               | L               | T <sub>1</sub>  |
|                    | T <sub>2</sub>                                                    | L              | H              | L              | L              | L               | L               | L               | T <sub>2</sub>  |
|                    | T <sub>3</sub>                                                    | H              | L              | L              | L              | L               | L               | L               | T <sub>3</sub>  |
| Four-Way Branches  | T <sub>1</sub> & T <sub>0</sub>                                   | L              | L              | H              | H              | L               | L               | T <sub>1</sub>  | T <sub>0</sub>  |
|                    | T <sub>2</sub> & T <sub>0</sub>                                   | L              | H              | L              | H              | L               | L               | T <sub>2</sub>  | T <sub>0</sub>  |
|                    | T <sub>3</sub> & T <sub>0</sub>                                   | H              | L              | L              | H              | L               | L               | T <sub>3</sub>  | T <sub>0</sub>  |
|                    | T <sub>2</sub> & T <sub>1</sub>                                   | L              | H              | H              | L              | L               | L               | T <sub>2</sub>  | T <sub>1</sub>  |
|                    | T <sub>3</sub> & T <sub>1</sub>                                   | H              | L              | H              | L              | L               | L               | T <sub>3</sub>  | T <sub>1</sub>  |
|                    | T <sub>3</sub> & T <sub>2</sub>                                   | H              | H              | L              | L              | L               | L               | T <sub>3</sub>  | T <sub>2</sub>  |
| Eight-Way Branches | T <sub>2</sub> , T <sub>1</sub> , T <sub>0</sub>                  | L              | H              | H              | H              | L               | T <sub>2</sub>  | T <sub>1</sub>  | T <sub>0</sub>  |
|                    | T <sub>3</sub> , T <sub>1</sub> , T <sub>0</sub>                  | H              | L              | H              | H              | L               | T <sub>3</sub>  | T <sub>1</sub>  | T <sub>0</sub>  |
|                    | T <sub>3</sub> , T <sub>2</sub> , T <sub>0</sub>                  | H              | H              | L              | H              | L               | T <sub>3</sub>  | T <sub>2</sub>  | T <sub>0</sub>  |
|                    | T <sub>3</sub> , T <sub>2</sub> , T <sub>1</sub>                  | H              | H              | H              | L              | L               | T <sub>3</sub>  | T <sub>2</sub>  | T <sub>1</sub>  |
| Sixteen-Way Branch | T <sub>3</sub> , T <sub>2</sub> , T <sub>1</sub> , T <sub>0</sub> | H              | H              | H              | H              | T <sub>3</sub>  | T <sub>2</sub>  | T <sub>1</sub>  | T <sub>0</sub>  |

### Figure11-2. Am29803A Function Table



## ABSOLUTE MAXIMUM RATINGS

|                                        |                                |
|----------------------------------------|--------------------------------|
| Storage Temperature .....              | -65 to +150°C                  |
| (Ambient) Temperature Under Bias ..... | -55 to +125°C                  |
| Supply Voltage to Ground Potential     |                                |
| Continuous .....                       | -0.5 V to +7.0 V               |
| DC Voltage Applied to Outputs For      |                                |
| High Output State .....                | -0.5 V to +V <sub>CC</sub> max |
| DC Input Voltage .....                 | -0.5 V to +7.0 V               |
| DC Output Current, Into Outputs .....  | 30 mA                          |
| DC Input Current .....                 | -30 mA to +5.0 mA              |

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

|                                             |                    |
|---------------------------------------------|--------------------|
| Commercial (C) Devices                      |                    |
| Ambient Temperature (T <sub>A</sub> ) ..... | 0 to +70°C         |
| Supply Voltage (V <sub>CC</sub> ) .....     | +4.75 V to +5.25 V |
| Military (M) Devices                        |                    |
| Case Temperature (T <sub>C</sub> ) .....    | -55 to +125°C      |
| Supply Voltage .....                        | +4.5 V to +5.5 V   |

Operating ranges define those limits between which the functionality of the device is guaranteed.

### Thermal Resistance (Typical)

#### Am2909A

| Symbol        | PD 028 | CD 028 | CLT028 | CFM028 | Unit |
|---------------|--------|--------|--------|--------|------|
| $\theta_{JA}$ | 62     | 55     | 76     | 82     | °C/W |
| $\theta_{JC}$ | NA     | 5      | 7      | 8      | °C/W |

#### Am2911A

| Symbol        | PD 020 | CD 020 | CLT020 | Unit |
|---------------|--------|--------|--------|------|
| $\theta_{JA}$ | 76     | 74     | 84     | °C/W |
| $\theta_{JC}$ | NA     | 11     | 16     | °C/W |

\*Military product tested at T<sub>C</sub> = +25°C, +125°C, and -55°C.

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

| Parameter Symbol | Parameter Description                 | Test Conditions (Note 1)                                                       |                                |                                | Min.                    | Max.  | Unit |
|------------------|---------------------------------------|--------------------------------------------------------------------------------|--------------------------------|--------------------------------|-------------------------|-------|------|
| V <sub>OH</sub>  | Output HIGH Voltage                   | V <sub>CC</sub> = MIN,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | MIL                            | I <sub>OH</sub> = -1.0 mA      | 2.4                     |       | V    |
|                  |                                       |                                                                                | COM'L                          | I <sub>OH</sub> = -2.6 mA      | 2.4                     |       |      |
| V <sub>OL</sub>  | Output LOW Voltage                    | V <sub>CC</sub> = MIN,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OL</sub> = 16 mA        |                                |                         | 0.5   | V    |
| V <sub>IH</sub>  | Input HIGH Level                      | Guaranteed Input Logical-HIGH Voltage for All Inputs                           |                                |                                | 2.0                     |       | V    |
| V <sub>IL</sub>  | Input LOW-Level                       | Guaranteed Input Logical LOW Voltage for All Inputs                            |                                |                                |                         | 0.8   | V    |
| V <sub>I</sub>   | Input Clamp Voltage                   | V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA                               |                                |                                |                         | -1.5  | V    |
| I <sub>IL</sub>  | Input LOW Current                     | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = 0.4 V                             | C <sub>n</sub>                 |                                |                         | -1.08 | mA   |
|                  |                                       |                                                                                | Push/Pop, $\overline{OE}$      |                                |                         | -0.72 |      |
|                  |                                       |                                                                                | Others (Note 4)                |                                |                         | -0.36 |      |
| I <sub>IH</sub>  | Input HIGH Current                    | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = 2.7 V                             | C <sub>n</sub>                 |                                |                         | 40    | μA   |
|                  |                                       |                                                                                | Push/Pop, $\overline{OE}$      |                                |                         | 40    |      |
|                  |                                       |                                                                                | Others (Note 4)                |                                |                         | 20    |      |
| I <sub>I</sub>   | Input HIGH Current                    | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = 5.5 V                             | C <sub>n</sub> , Push/Pop      |                                |                         | 0.2   | mA   |
|                  |                                       |                                                                                | Others (Note 4)                |                                |                         | 0.1   |      |
| I <sub>OS</sub>  | Output Short Circuit Current (Note 2) | V <sub>CC</sub> = Max.+0.5 V<br>V <sub>OUT</sub> = 0.5V                        | Y <sub>0</sub> -Y <sub>3</sub> |                                | -30                     | -100  | mA   |
|                  |                                       |                                                                                | C <sub>n</sub> + 4             |                                | -30                     | -85   |      |
| I <sub>CC</sub>  | Power Supply Current                  | V <sub>CC</sub> = Max.<br>(Note 3)                                             | COM'L Only                     | T <sub>A</sub> = 0 to +70°C    |                         | 130   | mA   |
|                  |                                       |                                                                                | MIL Only                       | T <sub>C</sub> = -55 to +125°C |                         | 140   |      |
|                  |                                       |                                                                                |                                |                                | T <sub>C</sub> = +125°C |       |      |
| I <sub>OZL</sub> | Output OFF Current                    | V <sub>CC</sub> = Max,<br>$\overline{OE}$ = 2.7                                | Y <sub>0</sub> - 3             | V <sub>OUT</sub> = 0.4 V       |                         | -20   | μA   |
| I <sub>OZH</sub> |                                       |                                                                                |                                | V <sub>OUT</sub> = 2.7 V       |                         | 20    |      |

- Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.  
 2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.  
 3. Apply GND to C<sub>n</sub>, R<sub>0</sub>, R<sub>1</sub>, R<sub>2</sub>, R<sub>3</sub>, OR<sub>0</sub>, OR<sub>1</sub>, OR<sub>2</sub>, OR<sub>3</sub>, D<sub>0</sub>, D<sub>1</sub>, D<sub>2</sub>, and D<sub>3</sub>. Other inputs high. All outputs open. Measured after a LOW-to-HIGH clock transition.  
 4. For the Am2911A, D<sub>i</sub> and R<sub>i</sub> are internally connected. Loading is doubled (to same values as Push/Pop).

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Tables A, B, and C below define the timing characteristics of the Am2909A/Am2911A over the operating voltage and temperature range. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs, and setup and hold-time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5 V with  $V_{IL} = 0$  V and  $V_{IH} = 3.0$  V. For three-state disable tests,  $C_L = 5.0$  pF and measurement is to 0.5 V change on output voltage level. All outputs have maximum DC loading.

#### A. Cycle Time and Clock Characteristics

| Time                    | COMMERCIAL | MILITARY |
|-------------------------|------------|----------|
| Minimum Clock LOW Time  | 20         | 20       |
| Minimum Clock HIGH Time | 20         | 20       |

#### C. Minimum Setup and Hold Times (all in ns) (Note 1)

| From Input                      | Notes | COMMERCIAL |           | MILITARY   |           |
|---------------------------------|-------|------------|-----------|------------|-----------|
|                                 |       | Setup Time | Hold Time | Setup Time | Hold Time |
| RE                              |       | 19         | 4         | 19         | 5         |
| R <sub>i</sub> **               | 2     | 10         | 4         | 12         | 5         |
| PUP                             |       | 25         | 4         | 27         | 5         |
| FE                              |       | 25         | 4         | 27         | 5         |
| C <sub>n</sub>                  |       | 18         | 4         | 18         | 5         |
| D <sub>i</sub>                  |       | 25         | 0         | 25         | 0         |
| OR <sub>i</sub> **              |       | 25         | 0         | 25         | 0         |
| S <sub>0</sub> , S <sub>1</sub> |       | 25         | 0         | 29         | 0         |
| ZERO                            |       | 25         | 0         | 29         | 0         |

Notes: 1. All times relative to clock LOW-to-HIGH transition.

2. On Am2911A, R<sub>i</sub> and D<sub>i</sub> are internally connected together and labeled D<sub>i</sub>. Use R<sub>i</sub> set-up and hold times when D inputs are used to load register.

\*\*Am2909A only.

#### B. Maximum Combinational Propagation Delays (all in ns, C<sub>L</sub> = 50 pF (except output disable tests))

| From Input                                 | COMMERCIAL |                    | MILITARY |                    |
|--------------------------------------------|------------|--------------------|----------|--------------------|
|                                            | Y          | C <sub>n</sub> + 4 | Y        | C <sub>n</sub> + 4 |
| D <sub>i</sub>                             | 17         | 22                 | 20       | 25                 |
| S <sub>0</sub> , S <sub>1</sub>            | 29         | 34                 | 29       | 34                 |
| OR <sub>i</sub> **                         | 17         | 22                 | 20       | 25                 |
| C <sub>n</sub>                             | —          | 14                 | —        | 16                 |
| ZERO                                       | 29         | 34                 | 30       | 35                 |
| OE LOW (enable)                            | 25         | —                  | 25       | —                  |
| OE HIGH (disable)*                         | 25         | —                  | 25       | —                  |
| Clock ↑ S <sub>1</sub> S <sub>0</sub> = LH | 39         | 44                 | 45       | 50                 |
| Clock ↑ S <sub>1</sub> S <sub>0</sub> = LL | 39         | 44                 | 45       | 50                 |
| Clock ↑ S <sub>1</sub> S <sub>0</sub> = HL | 44         | 49                 | 53       | 58                 |

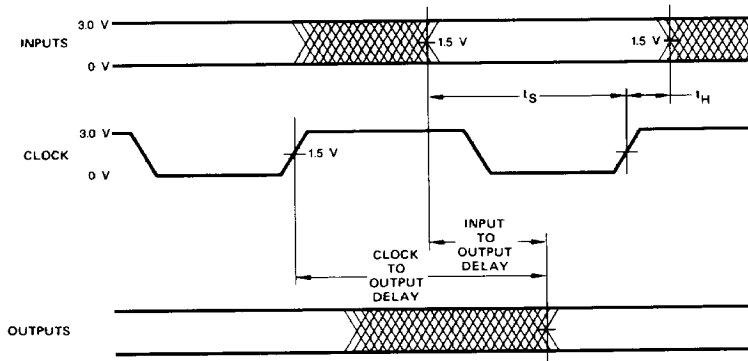
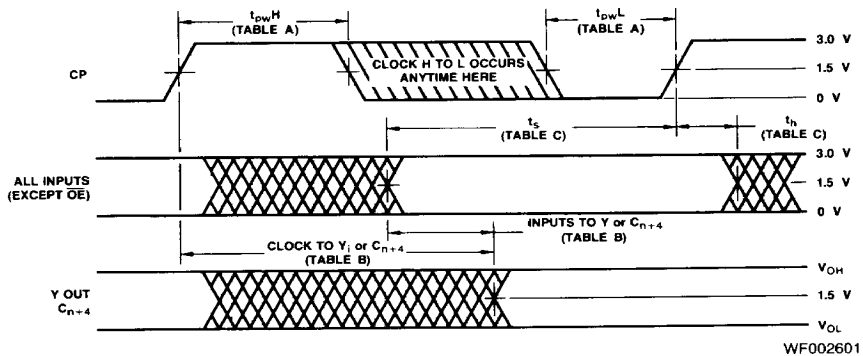
\*C<sub>L</sub> = 5 pF

## SWITCHING WAVEFORMS

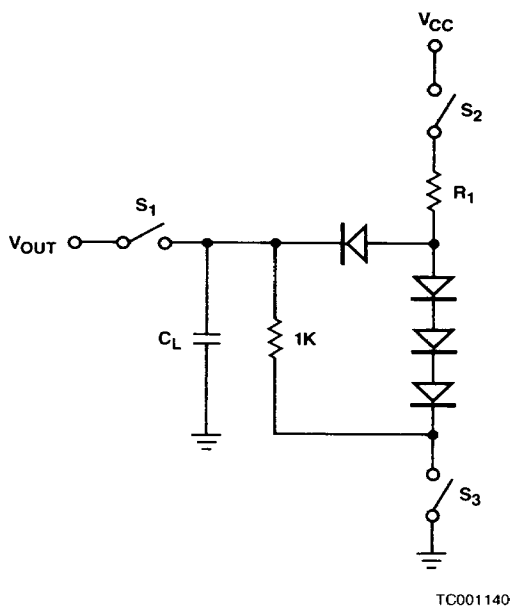
### Key to Switching Waveforms

| WAVEFORM | INPUTS                           | OUTPUTS                                   |
|----------|----------------------------------|-------------------------------------------|
|          | MUST BE STEADY                   | WILL BE STEADY                            |
|          | MAY CHANGE FROM H TO L           | WILL BE CHANGING FROM H TO L              |
|          | MAY CHANGE FROM L TO H           | WILL BE CHANGING FROM L TO H              |
|          | DON'T CARE, ANY CHANGE PERMITTED | CHANGING, STATE UNKNOWN                   |
|          | DOES NOT APPLY                   | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

KS000010



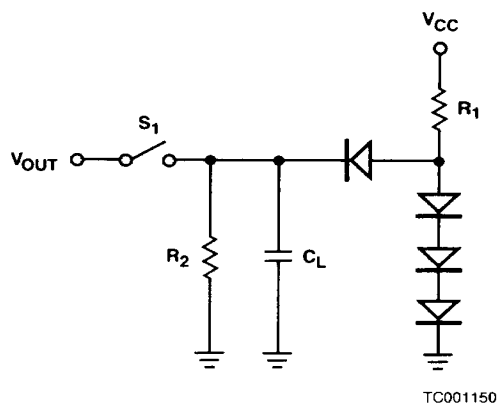
## SWITCHING TEST CIRCUITS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

### A. Three-State Outputs

- Notes: 1.  $C_L = 50$  pF includes scope probe, wiring and stray capacitances without device in test fixture.  
 2.  $S_1, S_2, S_3$  are closed during function tests all and AC tests except output enable tests.  
 3.  $S_1$  and  $S_3$  are closed while  $S_2$  is open for  $t_{pZH}$  test.  
 $S_1$  and  $S_2$  are closed while  $S_3$  is open for  $t_{pZL}$  test.  
 4.  $C_L = 5.0$  pF for output disable tests.



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

### B. Normal Outputs

## TEST OUTPUT LOADS

| Device  | Pin # | Pin Label          | Test Circuit | $R_1$ | $R_2$ |
|---------|-------|--------------------|--------------|-------|-------|
| Am2909A | 18-21 | Y <sub>0-3</sub>   | A            | 220   | 1K    |
| Am2911A | 12-15 |                    |              |       |       |
| Am2909A | 24    | C <sub>n + 4</sub> | B            | 220   | 2.4K  |
| AM2911A | 18    |                    |              |       |       |

## TEST PHILOSOPHY AND METHODS

The following nine points describe AMD's philosophy for high volume, high speed automatic testing.

1. Ensure that the part is adequately decoupled at the test head. Large changes in  $V_{CC}$  current as the device switches may cause erroneous function failures due to  $V_{CC}$  changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining point input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach  $V_{IL}$  or  $V_{IH}$  until the noise has settled. AMD recommends using  $V_{IL} \leq 0$  V and  $V_{IH} \geq 3.0$  V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Capacitive Loading for AC Testing

Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two

capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench setup and the knowledge that certain DC measurements ( $I_{OH}$ ,  $I_{OL}$  for example) have already been taken and are within spec. In some cases, special DC tests are performed in order to facilitate this correlation.

### 7. Threshold Testing

The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high speed circuits. These oscillations are not indicative of a reject device, but instead of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at  $V_{IL}$  Max. and  $V_{IH}$  Min.

### 8. AC Testing

Occasionally, parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer by using precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

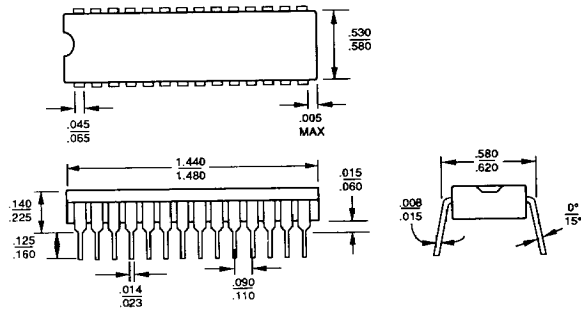
In some cases, certain AC tests are redundant, since they can be shown to be predicted by some other tests which have already been performed. In these cases, the redundant tests are not performed.

### 9. Output Short-Circuit Current Testing

When performing  $I_{OS}$  tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage ( $V_{OUTPUT}$ ) that is slightly above ground. The  $V_{CC}$  is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the  $V_{OUT} = 0$ ,  $V_{CC} = \text{Max.}$  case.

# PHYSICAL DIMENSIONS

PD 028

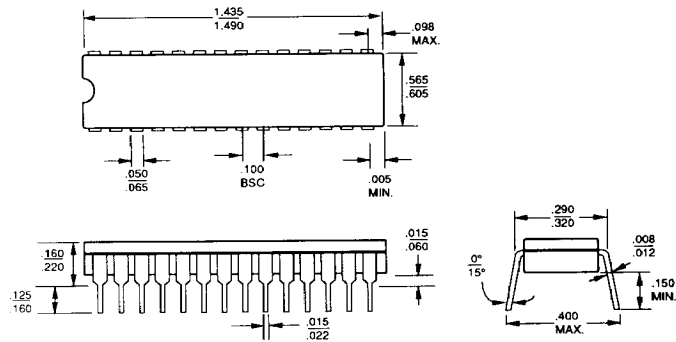


068428

\*For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.

# PHYSICAL DIMENSIONS (Cont'd.)

CD 028

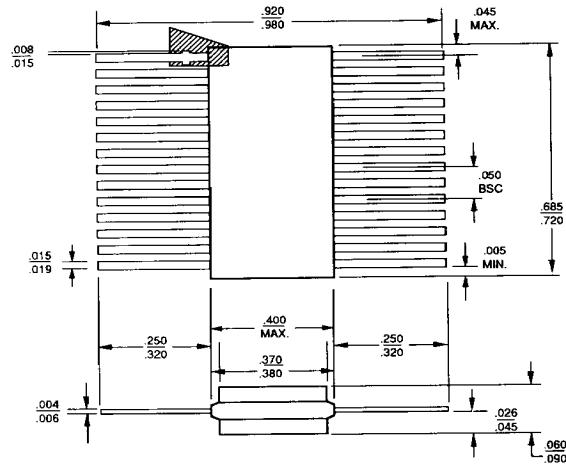


06837C

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# PHYSICAL DIMENSIONS (Cont'd.)

CFM028



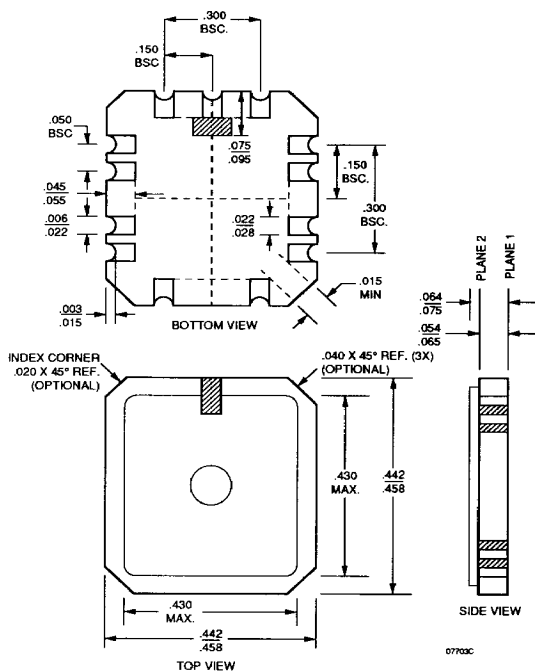
D97028

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# PHYSICAL DIMENSIONS (Cont'd.)

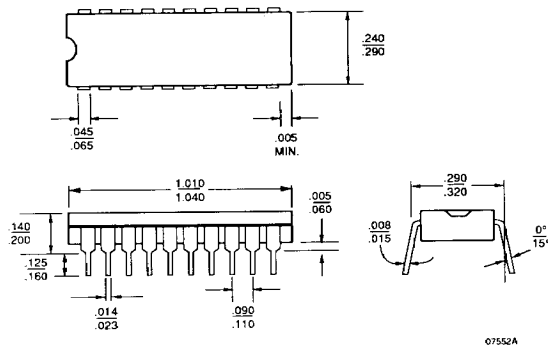
CLT028



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# PHYSICAL DIMENSIONS (Cont'd.)

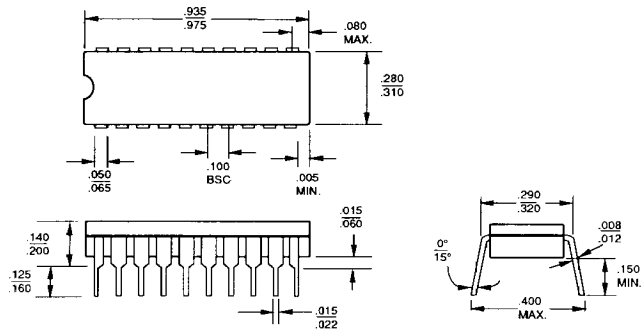
PD 020



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# PHYSICAL DIMENSIONS (Cont'd.)

CD 020

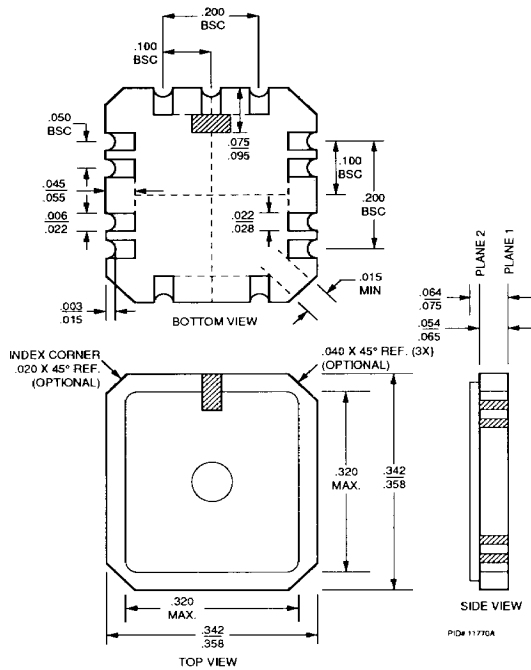


PID# 07553B

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# PHYSICAL DIMENSIONS (Cont'd.)

## CLT020



1/89  
AN 28  
CD

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