AN8130K

High-speed Low Power Consumption 10-bit A/D Converter

■ Overview

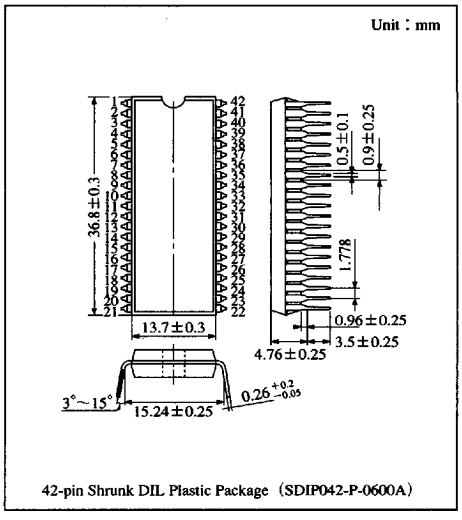
The AN8130K is a 10-bit A/D converter for image processing which has realized low power consumption by using the Bi-CMOS process.

■ Features

- 10-bit resolution
- High speed ; maximum conversion rate 20 MSPS
- Low power consumption ; 750mW
- Built-in sampling & holding circuit
- 2-step parallel type

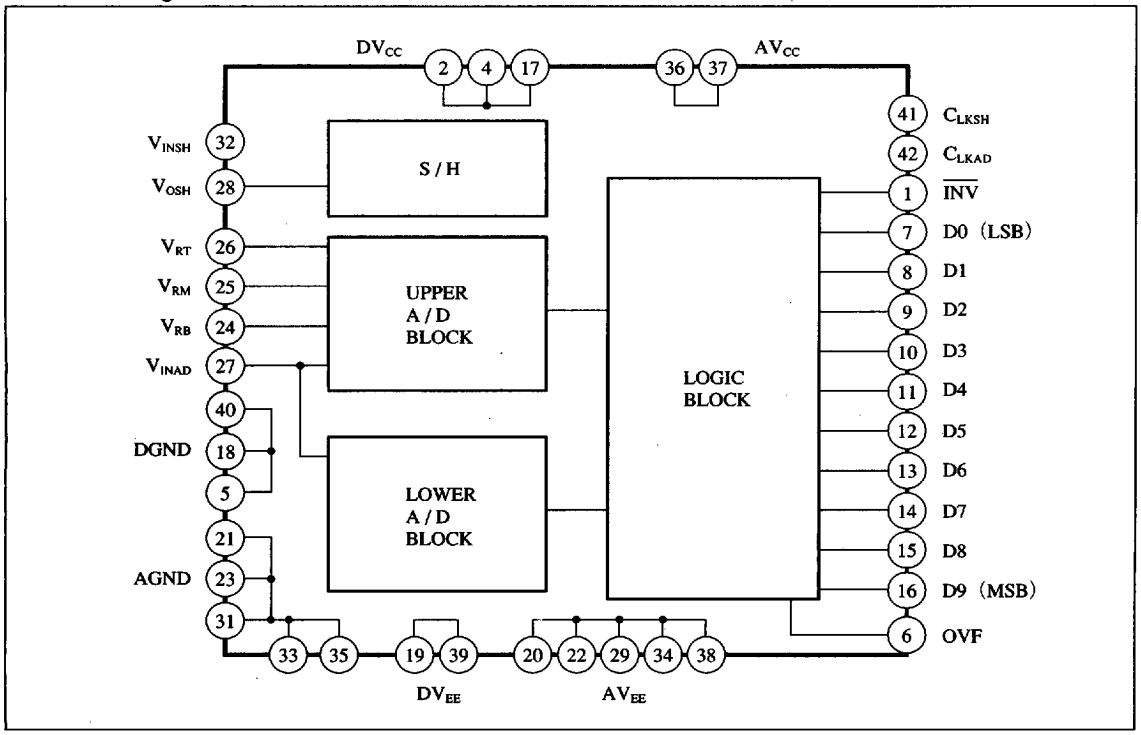
■ Application Field

- Digital video broadcasting such as D-STB
- Image equipment such as hi-vision device
- OA equipment such as image scanner
- Measuring equipment such as digital oscilloscope



42-pin Shrunk DIL Plastic Package (SDIP042-P-0600A)

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Pin name	Pin No.	Symbol	Pin name
1	INV	Digital output invert pin	22	AV_{EE}	Analogue negative power supply
2	DV_{CC}	Digital positive power supply	23	AGND	Analogue ground
3	NC	No connection pin	24	V_{RB}	Reference voltage low level
4	DV_{CC}	Digital positive power supply	25	V_{RM}	Reference voltage middle point level
5	DGND	Digital ground	26	V_{RT}	Reference voltage high level
6	OVF	Overflow pin	27	V_{INAD}	Analogue input (A/D)
7	D0	Digital output (LSB)	28	V_{OSH}	Analogue output (S/H)
8	D1	Digital output	29	AV_{EE}	Analogue negative power supply
9	D2	Digital output	30	NC	No connection pin
10	D3	Digital output	31	AGND	Analogue ground
11	D4	Digital output	32	V_{INSH}	Analogue input (S/H)
12	D5	Digital output	33	AGND	Analogue ground
13	D6	Digital output	34	AV_{EE}	Analogue negative power supply
14	D7	Digital output	35	AGND	Analogue ground
15	D8	Digital output	36	AV_{CC}	Analogue positive power supply
16	D9	Digital output (MSB)	37	AV_{CC}	Analogue positive power supply
17	DV_{CC}	Digital positive power supply	38	AV_{EE}	Analogue negative power supply
18	DGND	Digital ground	39	DV_{EE}	Digital negative power supply
19	DV_{EE}	Digital negative power supply	40	DGND	Digital ground
20	AV_{EE}	Analogue negative power supply	41	CLKSH	Clock input (S/H)
21	AGND	Analogue ground	42	CLKAD	Clock input (A/D)

■ Major Characteristics (V_{CC}=5.0V, V_{EE}=−5.0V, Ta=25℃)

Parameter	Condition	Rating	Unit
Resolution		10	Bit
Input dynamic range		2	V_{P-P}
Linearity error	$V_{IN}=2V_{P-P}$	±1.0	LSB
Differential linearity error		±0.5	LSB
Maximum conversion rate		20	MSPS
Quantization noise (S/N)	f_{CLK}=20MHz, f_I=1MHz	52	dB
	f_{CLK}=20MHz, f_I=8MHz	47	dB
Differential gain (DG)	IRE standard 15kHz Sawtooth 40% subcarrier	0.5	%
Differential phase (DP)	f_{CLK}=20MHz, Nolock	0.5	deg
Input band (BW)	$V_{IN}=2V_{P-P}$	10	MHz

■ Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{EE}	−6.0 to +0.5	V
	V_{CC}	−0.5 to +6.0	V
Analog input voltage	V_{IN}	V_{EE} to V_{CC}	V
Digital input voltage	V_{CLKSH}/V_{CLKAD}	−0.5 to V_{CC}+0.5	V
Reference voltage	IOVF, ID0 to ID9	−15	mA
Digital output current	V_{RB}/V_{RT}	V_{EE} to +0.5	V
Power dissipation	P_D	1100	mW
Operating ambient temperature	T_{opr}	−20 to +70	℃
Storage temperature	T_{stg}	−55 to +150	℃

■ Recommended Operating Conditions (Ta=25℃)

Parameter	Symbol	min	typ	max	Unit
Positive supply voltage	V_{CC}	4.75	5.0	5.25	V
Negative supply voltage	V_{EE}	−5.25	−5.0	−4.75	V
Reference voltage	V_{RT}	—	0	—	V
	V_{RB}	—	−2	—	V
Analog input voltage	V_{IN}	V_{RB}	—	V_{RT}	V
Digital input voltage	V_{IH}	2.0	—	3.5	V
	V_{IL}	0	—	0.8	V
Digital output current	I_{OH}	—	−0.4	—	mA
	I_{OL}	—	1.6	—	mA
S/H clock input pulse width*	t_H	15	20	—	ns
A/D clock input pulse width*	t_H	35	40	—	ns

* At f_{CLK}=16MHz

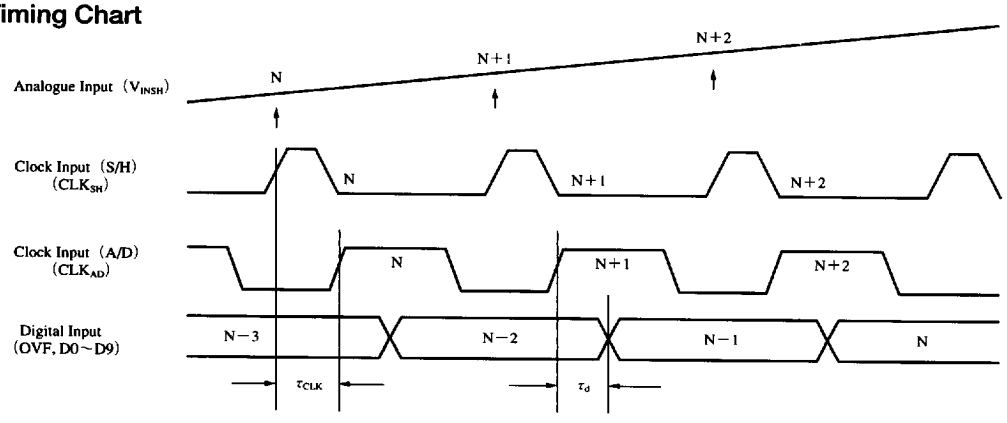
■ Electrical Characteristics (V_{CC}=5.0V, V_{EE}=−5.0V, Ta=25℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Supply current	DI_{CC}		—	5	10	mA
	AI_{CC}		—	14	28	mA
	I_{EE}		−164	−131	—	mA
Reference resistance current	I_{RT}	V_{RT}=0V	2.4	3	3.6	mA
	I_{RB}	V_{RB}=−2.0V	−3.6	−3	−2.4	mA
Input bias current	I_{IN}	V_{INSH}=−1.0V	—	10	100	μA
Clock input current	I_{IH}	V_{CLKAD}=V_{CLKSH}=2.7V	—	1	8	μA
	I_{IL}	V_{CLKAD}=V_{CLKSH}=0.4V	—	1	8	μA
Digital output voltage	V_{OH}	I_{OH}=−400μA	2.7	3.4	—	V
	V_{OL}	I_{OL}=1.6mA	—	—	0.4	V
Linearity error	E_L	V_{IN}=$2V_{P-P}$	—	±1.0	—	LSB
Differential linearity error	E_D	V_{IN}=$2V_{P-P}$	—	±0.5	±1.0	LSB
Maximum conversion rate	F_{CMAX}	V_{IN}=$2V_{P-P}$	20	—	—	MSPS
Quantization noise	S/N	f_{CLK}=16MHz, f_{IN}=1MHz	—	53	—	dB
		f_{CLK}=16MHz, f_{IN}=8MHz	—	49	—	dB
		f_{CLK}=20MHz, f_{IN}=1MHz	—	52	—	dB
		f_{CLK}=20MHz, f_{IN}=8MHz	—	47	—	dB
Differential gain	DG	IREstandard 15kHz Sawtooth 40% subcarrier f_{CLK}=20MHz, Nolock	—	0.5	1	%
Differential phase	DP		—	0.5	1	deg

■ Electrical Characteristics (cont.) (V_{CC}=5.0V, V_{EE}=−5.0V, Ta=25℃)

Parameter	Symbol	Condition	min	typ	max	Unit
Digital output delay	τ_d		—	33	—	ns
Clock delay	τ_{CLK}	f_{CLK}=16MHz	−5	0	5	ns
Input capacitance	C_{IN}		—	10	—	pF
Input offset	V_{OFS}		—	0	—	V

■ Timing Chart



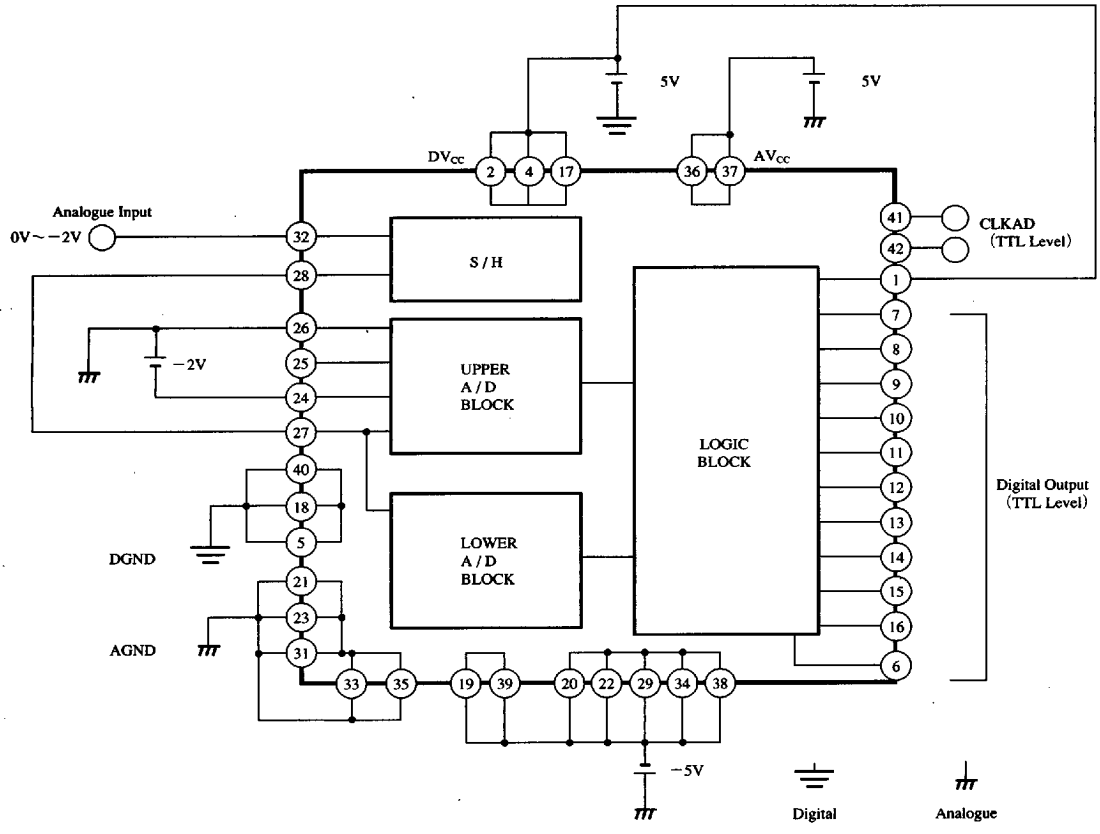
■ Pin Descriptions

Pin name	Description
Analogue power supply pins (AV_{CC}, AV_{EE})	They are power supply pins for analygue circuit block. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF as near as possible to the chip between each of these pins and AGND.
Digital power supply pin (DV_{CC})	It is a power supply pin for digital circuit block. Connect tantalum capacitor of several μF and ceramic capacitor of 0.1 μF as near as possible to the chip between this pin and DGND.
Ground pins (AGND, DGND)	Connect the analogue ground and digital ground with the possible lowest impedance at one point as near as possible to the chip. Inserting the ferrite beads between the above two grounds and connecting the analogue ground to the power supply ground may reduce the noise.
Reference voltage (V_{RB}, V_{RM}, V_{RT})	It is used to set the reference voltage for the comperator. Normally, the VRT is given 0 V and the VRB is given −2 V. Connect the tatulum capacitor of several μF and ceramic capacitor of 0.1 μF in parallel between each pin and analogue ground. VRM is pvovided for linearity compensation, which gives the middle point potential between VRT and VRB. However, it is normally opened.
$\overline{INV}$	Setting the INV pin to "L" level inverts all the outputs (D0-D9) but not the overflow pin. This pin is set to "L" level and operates a synchronously with clock.
Overflow output	When overflow occurs, it becomes "H" level. This output is not affected by the INV pin.
VINSH	It is an input pin of analogue signal for sample hold circuit. Input capacitance is about 10 pF. However, in order to obtain the good frequency characteristics, drive it by using the buffer with the possible large driving capacity. The resistance of approx. 150Ω should be inserted between this pin and AGND pin to make the frequency characteristics flat.
VINAD	It is an input pin of analogue signal for AD conversion circuit. Normally, the sample holding output VOSH is directly connected with this pin. However, when the ringing is large, connect the inductor of 0.3 μH and resistor of approx. 150Ω in series with this pin.
Clock input (CLKAD, CLKSH)	These are clocks of AD circuit and S/H circuit. For their details, refer to the timing chart. Input the signals with small jitter at TTL level. Care should be taken to suppress the ringing, particularly overshoot. When the CMOS level is used, arrangement should be made so that the high level could be under 3.5 V by using the resistive divider.
Digital outputs (D0~D9)	They are output pins at TTL level. In order to prevent the digital noise to the analogue circuit, suppress the ringing as far as possible. It is effective to insert the ferrite beads or resistance of approx. 220Ω between each of these pins and input pin of logic IC which receives it.

Output Code

Step	Input signal	Digital output
	2.000VFS 1.953mV STEP	M L OVF 9876543210
	$\overline{INV}$ = "H"	
000	−0.000000	00000000000
001	−0.001953	00000000001
.	.	.
.	.	.
.	.	.
511	−0.998047	00111111111
512	−1.000000	01000000000
513	−1.001953	01000000001
.	.	.
.	.	.
.	.	.
1023	−1.998047	01111111111
1024	−2.000000	11111111111

Application Circuit



■Technical Information

Bi-CMOS 10-Bit A/D Converter for Image Processing, the AN8130K

1. Overview

The AN8130K is a high accuracy low consumption 10-bit 20MSPS A/D converter. It is best suitable for the high quality TV such as hi-vision device.

2. Construction

The common high speed A/D converters use the conversion method which is called "total parallel connection." For the 10-bit A/D converter using this method, since 1023 comparators $(2^{10}-1)$ is required, chip area and consumption power should be large.

For the AN8130K, as shown in Fig. 1, the conversion method of serial and parallel connection type is employed to suppress the cunsumption power For this conversion method, the signal conversion from analogue to digital is performed by two steps, upper and lower. The AN8130K employs the conversion method, which is called "overlap interpolation method" [1) 2)] for the lower step to realize the high accuracy conversion.

The above two step conversion requires S/H circuit, which holds the analogue signals during the step shift. This S/H circuit is built in the AN8130K for easy operation

3. Features

The AN8130K employs the low consumption power 1.2 μ m Bi-CMOS process. In order to provide high speed high accuracy conversion, the following circuit features are incorporated.

- ●Overlap interpolation function
- ●Built-in S/H circuit

These functions are described below.

3.1 Overlap interpolation Function

As shown in Fig. 1, the AN8130K uses the serial and parallel connection method of upper 6-bits and lower 5-bits. First of all, the rough conversion is performed for upper 63 comparators. When input voltage Vi is between reference voltages V_{CN} and V_{CN-1}, current switches N−1, N, N+1 are turned on to convert the output current of differential amplifiers N−1, N and N+1 into voltage with resistances A, B and C. This voltage is deprived from the amplification of the difference voltage between input voltage Vi and the reference of differential amplifiers N−1, N, N+1. The lower conversion is performed on the base of this difference voltage.

Fig. 2 (b) shows the principle of lower conversion. In this figure, resistances A, B and C and the differential buffer are omitted so that operation can be easily grasped. The non reversal output of the differential amplifier N−1 and that of the differential amplifier are divided into 8 parts by resistances. Likewise, the reversal output of the differential amplifier N−1 and that of the differential amplifier N are also divided into 8 parts by resistances. All the lower comparators are connected to each node of resistances in the same way as comparators d4 and d5. For the difference between the input voltage and the reference voltage, each node voltage of resistances is changed as shown in Fig. 2 (a). For example, when input voltage Vi is between cross points 4 and 5, the inferior output is determined from the output of lower comparators d4 and d5.

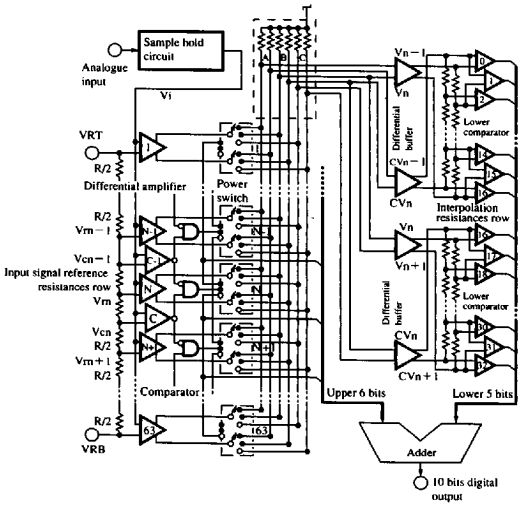
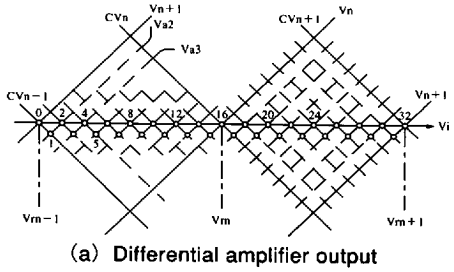
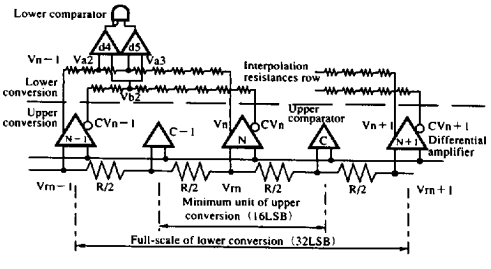


Fig. 1 AN8130K block diagram



(a) Differential amplifier output



(b) Conversion equivalent circuit

Fig. 2 Principle of lower conversion

The input voltage to the lower comparator has been amplified by the differential amplifier in the prior step. By this process, dispersion of emitter base normal direction voltage V_{BE}, ΔV_{BE} (the input transistor of lower comparator) becomes equivalently an inverse number of amplification rate. The full-scale of the lower conversion is connected with the minimum unit of the upper conversion (16LSB), overlapped with one side (8LSB). For this reason, conversion error which occurs in the upper comparator can be compensated up to 8LSB, thus providing the high accuracy conversion.

3.2 S/H Conversion

The S/H circuit ofthe AN8130K consists of the diode bridge, holding capacitor and buffer amplifier. The analogue input voltage is accumulated in the holding capacitor through the diode bridge. Then, the buffer amplifier in the post step drives the serial/parallel connection A/D converter. Since this buffer amplifier functions as CMOS input, the bias current is not flown, and holding capacitance can be reduced, allowing the high speed processing. The S/H circuit has the following characteristics : for 10-bit accuracy, aquisition time is 20ns, setting time is 2ns ; for sampling frequency of 25MHz and input frequency of 10MHz, total harmonics distortion is −59bB, S/N is 65dB. Thus, the S/H circuit employed in the AN8130K has sufficiently appropriate characteristics as S/H circuit for 10-bit A/D converter.

4. Application

Fig. 3 shown application circuit of the AN8130K. The supply voltage is set to ±5V, the reference voltages to 0, 2V. The analogue input ranges from −2 to 0V. The digital input and output is at TTL level. Use the separate power supplys for the analogue power supply pins (AV_{CC}, AV_{EE}) and the digital power supply pin (DV_{CC}). Connect the analogue ground and the digital ground at one point as near as possible to the analogue ground pin.

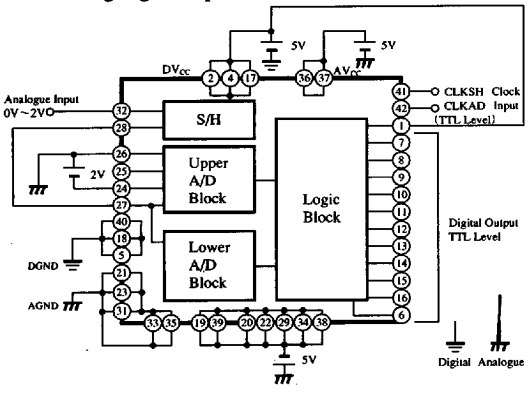


Fig. 3 AN8130K Application Circuit

5. Characteristics

Table 1 shows the major characteristics of the AN8130K. Fig. 4 shows the conversion characteristics when the sampling frequency is 16MHz and the input frequency is 5kHz

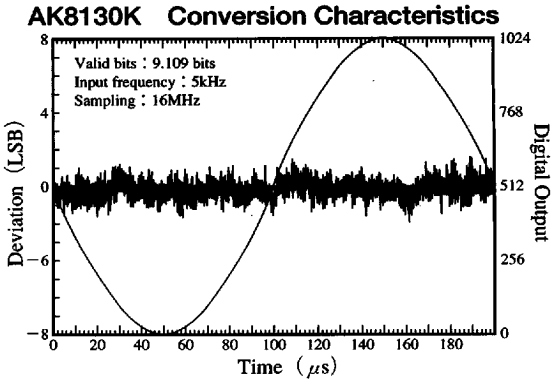


Fig.4 AN8130K Conversion Characteristics

6. References

1) Akira Matuzawa et al, "A 10b 30MHz 2−step Parallel Bi-CMOS ADC with Internal S/H" (ISSCC' 90)
2) Masa-aki Kanoh et al., "10bits 30MSPS Serial/ Prallel Connection A/D Converter "
(Electronic Information Communication Society Spring National Symposium in 1990)
3) Ichiro Tada et al., "High-Speed High -Accuracy Bi-CMOS Sample Holding Circuit" (Electronic Information Communication Society Spring National Symposium in 1990)

Table 1 Major Characteristics

Parameter \ Model	AN8130K (10-Bits A/D converter)
Resolution	10bits
Maximum conversion frequency	20MHz
Non-linearity error (typ.)	±1LSB
Differential non-linearity error (typ.)	±0.5LSB
No missing code	Guaranteed
SNR	52dB (1MHz input, 20MHz clock) 47dB (8MHz input, 20MHz clock)
Input signal band	10MHz
Droop rate	0.2mV/μs
Input voltage range	0 to −2V
Supply voltage	±5V
Consumption power	750mW
I/O level	TTL
Package	42-lead plastic DIL (Shrink type)