

DM74LS244

Octal 3-STATE Buffer/Line Driver/Line Receiver

General Description

These buffers/line drivers are designed to improve both the performance and PC board density of 3-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

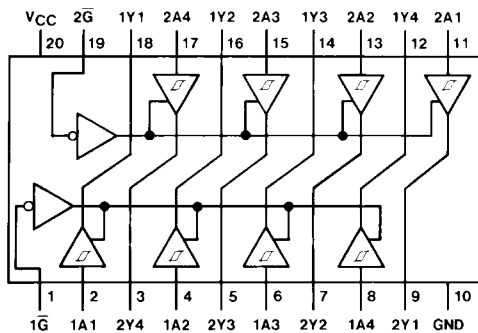
- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current) 24 mA
- Typical I_{OH} (source current) -15 mA
- Typical propagation delay times
 - Inverting 10.5 ns
 - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
 - Inverting 130 mW
 - Noninverting 135 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS244WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS244N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs		Output
$\bar{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = LOW Logic Level
H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			–15	mA
I _{OL}	LOW Level Output Current			24	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = –18 mA			–1.5	V
HYS	Hysteresis (V _{T+} – V _{T–}) Data Inputs Only	V _{CC} = Min	0.2	0.4		V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, V _{IH} = Min V _{IL} = Max, I _{OH} = –1 mA	2.7			V
		V _{CC} = Min, V _{IH} = Min V _{IL} = Max, I _{OH} = –3 mA	2.4	3.4		
		V _{CC} = Min, V _{IH} = Min V _{IL} = 0.5V, I _{OH} = Max	2			
V _{OL}	LOW Level Output Voltage	V _{CC} = Min I _{OL} = 12 mA			0.4	V
		V _{IL} = Max I _{OL} = Max			0.5	
		V _{IH} = Min				
I _{OZH}	Off-State Output Current, HIGH Level Voltage Applied	V _{CC} = Max V _{IL} = Max	V _O = 2.7V		20	μA
I _{OZL}	Off-State Output Current, LOW Level Voltage Applied	V _{IH} = Min	V _O = 0.4V		–20	μA
I _I	Input Current at Maximum Input Voltage	V _{CC} = Max	V _I = 7V		0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max	V _I = 2.7V		20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max	V _I = 0.4V	–0.5	–200	μA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	–40		–225	mA
I _{CC}	Supply Current	V _{CC} = Max, Outputs Open	Outputs HIGH		13	mA
			Outputs LOW		27	
			Outputs Disabled		32	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

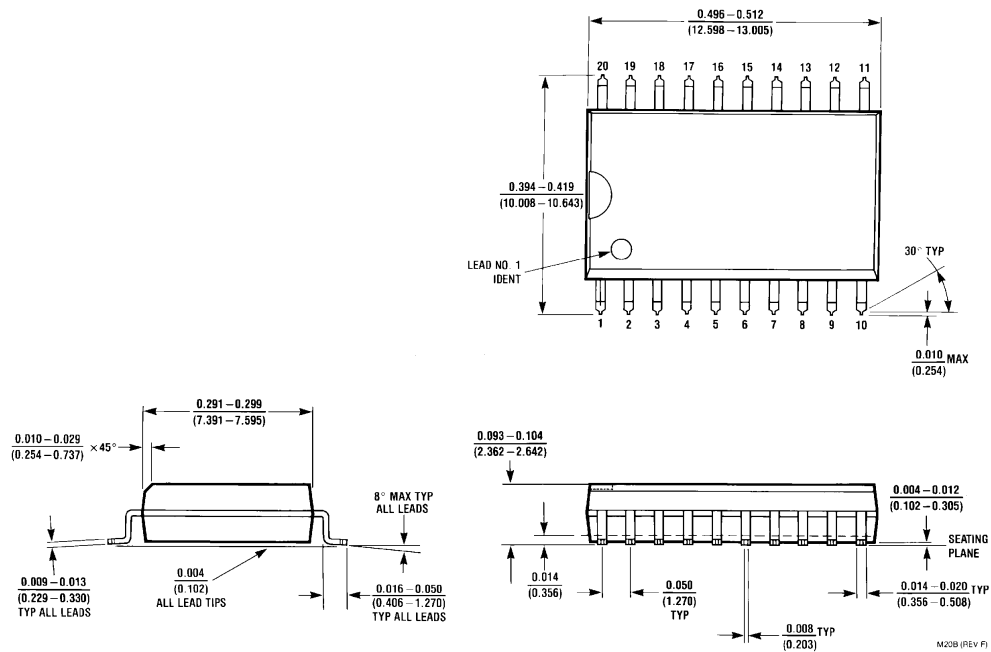
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at $V_{CC} = 5V$, $T_A = 25^\circ C$

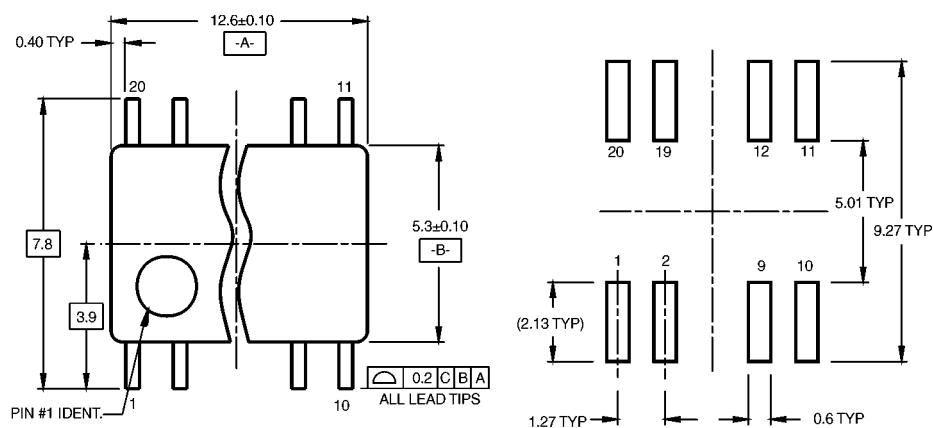
Symbol	Parameter	Conditions	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$	18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$	18	ns
t_{PZL}	Output Enable Time to LOW Level	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$	30	ns
t_{PZH}	Output Enable Time to HIGH Level	$C_L = 45 \text{ pF}$ $R_L = 667\Omega$	23	ns
t_{PLZ}	Output Disable Time from LOW Level	$C_L = 5 \text{ pF}$ $R_L = 667\Omega$	25	ns
t_{PHZ}	Output Disable Time from HIGH Level	$C_L = 5 \text{ pF}$ $R_L = 667\Omega$	18	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$	21	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$	22	ns
t_{PZL}	Output Enable Time to LOW Level	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$	33	ns
t_{PZH}	Output Enable Time to HIGH Level	$C_L = 150 \text{ pF}$ $R_L = 667\Omega$	26	ns

Physical Dimensions inches (millimeters) unless otherwise noted

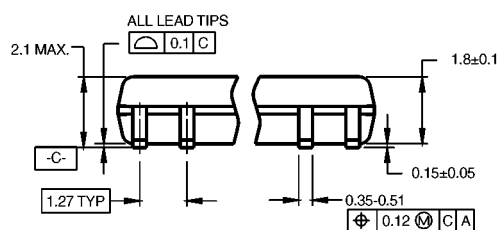


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B

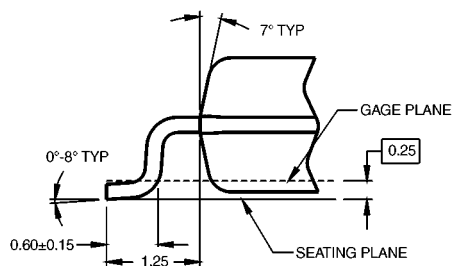
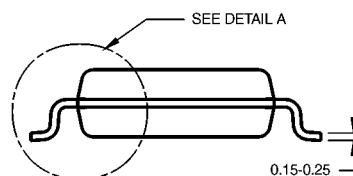
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

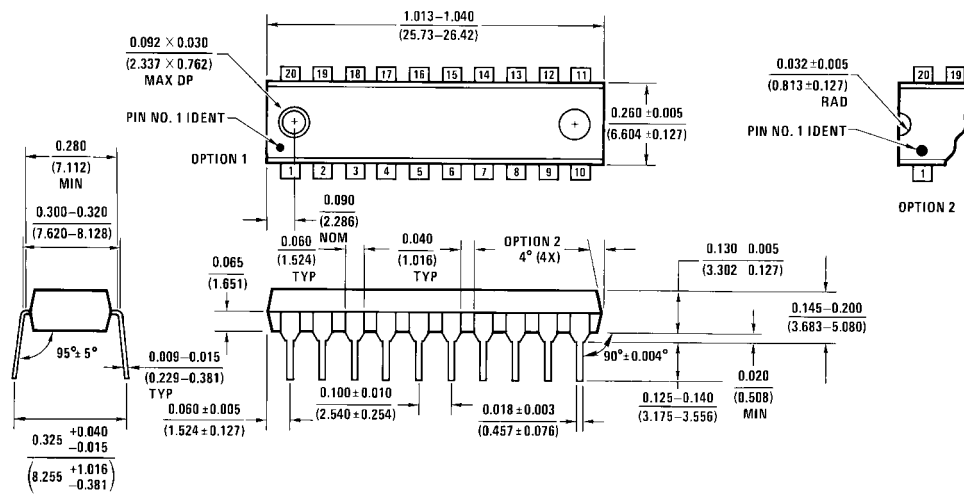
NOTES:

- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com