Si2161

DVB-T Demodulator

Description

The Si2161 is a compact, standalone DVB-T digital TV demodulator ideally matching Silicon Labs' Si2170/1/2 new hybrid silicon tuner product family. The analog front-end consists of two ADCs with wide dynamic range (12-bit) to allow operation with standard IF (~36 MHz), Low-IF, or Zero-IF inputs. This enables the use of the Si2161 with any TV tuner, either metal can or silicon tuner based.

The demodulator supports all modes of DVB-T (EN 300 744), including hierarchical modes. In addition to DVB-T's 2 K and 8 K FFT modes, the Si2161 also includes a 4 K FFT mode, "native" and "in-depth" deinterleavers, and extended TPS to be compliant with DVB-H (EN 300 744 Annex F). The Si2161 can then receive DVB-H programs in fixed receiver applications (without decoding DVB-H's additional MPE FEC layer).

An embedded 32-bit DSP controls device operation. Sophisticated on-chip algorithms ensure optimum reception even under difficult channel conditions, such as echoes outside the guard interval, pre-echoes, or strong impulse noise. For ease-of-use, DSP firmware is preloaded into ROM (device is immediately active at powerup). Nevertheless, there is a possibility of downloading additional patch code via the I^2C interface, e.g. to adjust the demodulator to unexpected conditions or reception impairments.

The Si2161 supports ultra-fast channel scanning for VHF/UHF terrestrial DTV channels, thanks to proprietary features. For supported tuners, the complete algorithm for fast channel scan, *QuickScan*, is provided as a downloadable patch file. *QuickScan* runs on the embedded DSP to limit the host CPU burden.

Serial or parallel master MPEG TS output modes are supported. Furthermore, a TS slave parallel mode is available via a GPIF port and provides a glueless interface to Silicon Labs' MCU devices with embedded USB interface. The user can optionally program a 32-PID hardware filter to reduce the output TS bit rate.

An internal I^2C pass-through logic switch acts as an I^2C repeater. This provides a "quiet" I^2C bus to the RF front end.

A maximum of six general-purpose inputs/outputs are available; three GPIOs also feature Δ/Σ and interrupt output capabilities. Best-in-class demodulation performance is achieved while still maintaining very low-power operation.

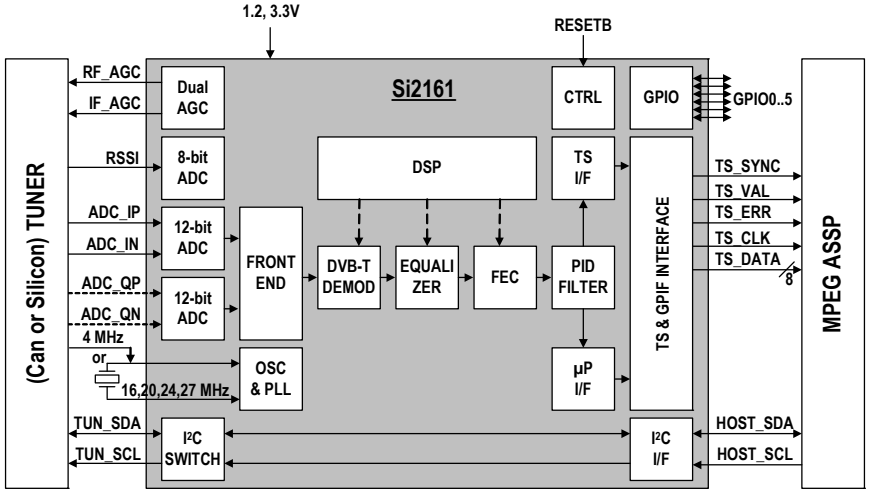
The Si2161 guarantees a low-cost system implementation due to its minimal BOM and very small package footprint.

Features

- DVB-T (ETSI EN 300 744) demodulator and FEC decoder.
- NorDig Unified 2.0, D-Book 4.0 compliant.
- Suitable for low-power design: 130 mW (typical, 36 MHz IF sampling mode).
- Dual 12-bit ADCs: accept 1st IF, low IF, or zero-IF inputs in 5, 6, 7, or 8 MHz channel bandwidths.
- DSP-based synchronization and control with embedded ROM code avoids the need for code download at startup.
- Supports patch code downloads for in-field upgradeability.
- Independent AGC controls (for IF & RF), plus RSSI measurement.
- ACI filtering: fixed 8 MHz SAW filter even for 7 MHz channel.
- Advanced performance for SFN networks.
- Impulsive noise protection algorithm.
- Ultra-fast automatic UHF/VHF band scanning (*QuickScan*).
- Master TS output modes, parallel or serial (with tri-state function).
- Slave TS parallel output: external device polls data from an embedded FIFO, providing a seamless interface to any USB controller.
- On-chip PID filtering to reduce TS output bit rate.
- Up to six GPIOs.
- Two 5 V-tolerant I^2C control buses (host-side, tuner-side) with on-chip I^2C repeater.
- 4, 16, 20, 24, or 27 MHz clock/crystal reference.
- 3.3 and 1.2 V power supplies only.
- Very compact QFN-36, 5 x 6 mm, RoHS-compliant package.

Applications

- Digital terrestrial STB, NIM, and iDTV set
- Digital terrestrial PC-TV tuner peripheral
- Digital Picture Frame with TV front-end
- Portable DVB-T receiver/DVD player/PMP
- Personal Video Recorder (DVD or HDD-based)

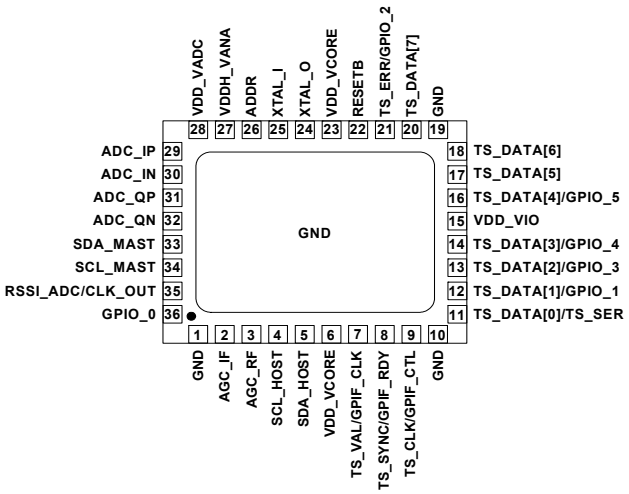


Selected Electrical Specifications

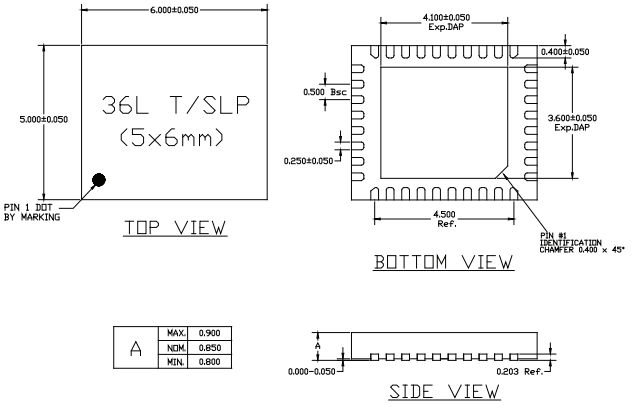
Parameter	Min	Typ	Max	Unit
General				
Ambient Temperature	0	25	85	°C
Power-up Time	—	—	10	ms
I^2C Speed (Host side)	<1	—	400	kHz
Input Clock or Supported Xtal Frequency	—	4*/16/20/24/27	—	MHz
VDD_VCORE Supply	1.14	1.2	1.26	V
VDD_VIO Supply**	1.62	1.80 to 3.30	3.60	V
VDD_VADC	1.14	1.2	1.26	V
VDDH_VANA	3.00	3.30	3.60	V
Input ADC (2 x 12-bits)				
Input Differential Voltage Range	—	1	—	Vpp
IF Oversampling Mode Clock	37	48	60	MHz
IF Sub-sampling Mode Clock	18.5	27	32.5	MHz
ZIF Mode Sampling Clock	18.5	48	60	MHz
System Clock	—	—	85	MHz
TS Output Rates				
Serial Mode Clock	—	—	42	MHz
Power Consumption				
DVB-T 8 MHz, IF Mode (adc_clk @ 56 MHz), Parallel TS	—	140	—	mW
Total Stand-by Power Consumption	—	13	—	mW

***Note:** Clock only.
****Note:** 5 V tolerant I^2C bus requires VDD_VIO supply set @ 3.3 V.

Pin Assignments



5 x 6 mm SLP QFN-36 Package Information



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Silicon Laboratories:

Si2161-D-GMR Si2163-D-GMR