Mixed-Signal Front End for Broadband Applications

AD9878

FEATURES

Low cost 3.3 V CMOS MxFE™ for broadband applications
DOCSIS, EURO-DOCSIS, DVB, DAVIC compliant
232 MHz quadrature digital upconverter
12-bit direct IF DAC (TxDAC+™)
Up to 65 MHz carrier frequency DDS
Programmable sampling clock rates
Analog Tx output level adjust
Dual 12-bit, 29 MSPS direct IF ADCs with video clamp input
10-bit, 29 MSPS sampling ADC
8-bit sigma-delta auxiliary DAC
Direct interface to AD8321/AD8323 or AD8322/AD8327 PGA cable driver

APPLICATIONS

Cable set-top boxes
Cable and wireless modems

FUNCTIONAL BLOCK DIAGRAM

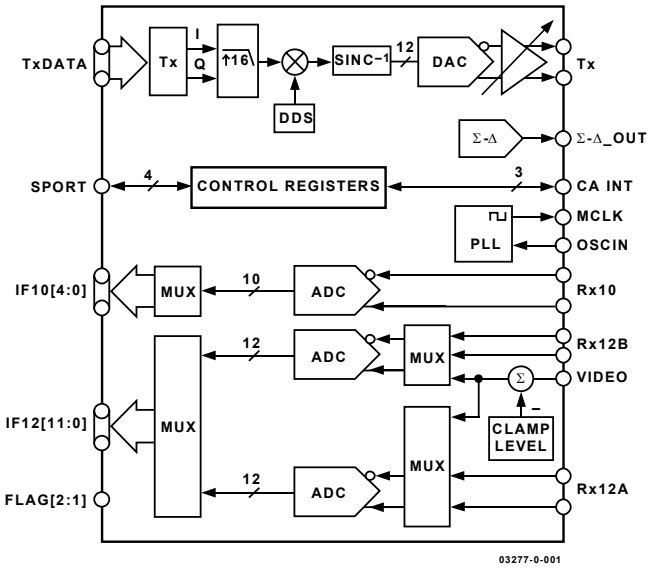

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD9878 is a single-supply cable modem/set-top box mixed-signal front end. The device contains a transmit path interpolation filter, a complete quadrature digital upconverter, and transmit DAC. The receive path contains dual 12-bit ADCs and a 10-bit ADC. All internally required clocks and an output system clock are generated by the PLL from a single crystal oscillator or clock input.

The transmit path interpolation filter provides an upsampling factor of 16× with an output signal bandwidth up to 5.8 MHz. Carrier frequencies up to 65 MHz with 26 bits of frequency tuning resolution can be generated by the direct digital synthesizer (DDS). The transmit DAC resolution is 12 bits and can run at sampling rates as high as 232 MSPS. Analog output scaling from 0 dB to 7.5 dB in 0.5 dB steps is available to preserve SNR when reduced output levels are required.

The 12-bit ADCs provide excellent undersampling performance, allowing this device to deliver better than 10 ENOBs with IF inputs up to 70 MHz. The 12-bit IF ADCs can sample at rates up to 29 MHz, allowing them to process wideband signals.

The AD9878 includes a programmable sigma-delta DAC, which can be used to control an external component such as a variable gain amplifier (VGA) or a voltage controlled tuner.

The AD9878 also integrates a CA port that enables a host processor to interface with the AD8321/AD8323 or AD8322/AD8327/AD8328 programmable gain amplifier (PGA) cable drivers via the MxFE serial port (SPORT).

The AD9878 is available in a 100-lead LQFP package. The AD9878 is specified over the extended industrial (–40°C to +85°C) temperature range.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

Table 1. ELECTRICAL CHARACTERISTICS

(V_{AS} = 3.3 V ± 5%, V_{DS} = 3.3 V ± 10%, f_{OSCIN} = 27 MHz, f_{SYSCLK} = 216 MHz, f_{MCLK} = 54 MHz (M = 8), ADC Clock Derived from OSCIN, R_{SET} = 4.02 kΩ, Max. Fine Gain, 75 Ω DAC Load.)

PARAMETER	Temp	Test Level	Min	Typ	Max	Unit
OSCIN and XTAL CHARACTERISTICS						
Frequency Range	Full	II	3		29	MHz
Duty Cycle	25ºC	II	35	50	65	%
Input Impedance	25ºC	III		100||3		MΩ||pF
MCLK Cycle to Cycle Jitter (f_{MCLK} derived from PLL)	25ºC	III		6		ps rms
Tx DAC CHARACTERISTICS						
Maximum Sample Rate	Full	II	232			MHz
Resolution	N/A	N/A		12		Bits
Full-Scale Output Current	Full	II	4	10	20	mA
Gain Error (Using Internal Reference)	Full	II	–2.5	–1	+2.5	% FS
Offset Error	25°C	III		±1.0		% FS
Reference Voltage (REFIO Level)	25°C	III		1.23		V
Differential Nonlinearity (DNL)	25°C	III		±2.5		LSB
Integral Nonlinearity (INL)	25°C	III		±8		LSB
Output Capacitance	25°C	III		5		pF
Phase Noise @ 1 kHz Offset, 42 MHz Carrier	25°C	III		–110		dBc/Hz
Output Voltage Compliance Range	Full	II	–0.5		+1.5	V
Wideband SFDR						
5 MHz Analog Out, I_{OUT} = 10 mA	Full	I	62.4	68		dB
65 MHz Analog Out, I_{OUT} = 10 mA	Full	I	50.3	53.5		dB
Narrow-Band SFDR (±1 MHz Window)						
5 MHz Analog Out, I_{OUT} = 10 mA	Full	I	71	74		dB
65 MHz Analog Out, I_{OUT} = 10 mA	Full	I	61	64		dB
Tx MODULATOR CHARACTERISTICS						
I/Q Offset	Full	II	50	55		dB
Pass-Band Amplitude Ripple (f < f_{IQCLK}/8)	Full	II			±0.1	dB
Pass-Band Amplitude Ripple (f < f_{IQCLK}/4)	Full	II			±0.5	dB
Stop-Band Response (f > f_{IQCLK} × 3/4)	Full	II			–63	dB
Tx GAIN CONTROL						
Gain Step Size	25°C	III		0.5		dB
Gain Step Error	25°C	III		<0.05		dB
Settling Time, 1% (Full-Scale Step)	25°C	III		1.8		µs
10-BIT ADC CHARACTERISTICS						
Resolution	N/A	N/A		10		Bits
Maximum Conversion Rate	Full	II	29			MHz
Pipeline Delay	N/A	N/A		4.5		ADC cycles
Analog Input						
Input Voltage Range	Full	II		2		Vppd
Differential Input Impedance	25°C	III		4||2		kΩ||pF
Full Power Bandwidth	25°C	III		90		MHz
Dynamic Performance (f = 5 MHz)						
Signal-to-Noise and Distortion (SINAD)	Full	I	57.6	59.7		dB
Effective Number of Bits (ENOB)	Full	I	9.2	9.6		Bits
Total Harmonic Distortion (THD)	Full	I		–71.1	–63.6	dB
Spurious-Free Dynamic Range (SFDR)	Full	I	65.7	72.4		dB
Reference Voltage Error, REFT10–REFB10 (1.0 V)	Full	I		±4	±200	mV

PARAMETER	Temp	Test Level	Min	Typ	Max	Unit
Dynamic Performance (f = 50 MHz)						
Signal-to-Noise and Distortion (SINAD)	Full	I	54.8	57.8		dB
Effective Number of Bits (ENOB)	Full	I	8.8	9.3		Bits
Total Harmonic Distortion (THD)	Full	I		–63.3	–56.9	dB
Spurious-Free Dynamic Range (SFDR)	Full	I	56.9	63.7		dB
12-BIT ADC CHARACTERISTICS						
Resolution	N/A	N/A		12		Bits
Maximum Conversion Rate	Full	II	29			MHz
Pipeline Delay	N/A	N/A		5.5		ADC cycles
Analog Input						
Input Voltage Range	Full	III		2		Vppd
Differential Input Impedance	25°C	III		4||2		kΩ||pF
Aperture Delay	25°C	III		2.0		ns
Aperture Uncertainty (Jitter)	25°C	III		1.2		ps rms
Full Power Bandwidth	25°C	III		85		MHz
Input Referred Noise	25°C	III		75		µV
Reference Voltage Error, REFT12–REFB12 (1 V)	Full	I	–200	±16	+200	mV
Dynamic Performance (A_{IN} = –0.5 dBFS, f = 5 MHz)						
ADC Sample Clock = OSCIN						
Signal-to-Noise and Distortion (SINAD)	Full	I	61.0	67		dB
Effective Number of Bits (ENOBs)	Full	I	9.8	10.8		Bits
Signal-to-Noise Ratio (SNR)	Full	I	64.2	66		dB
Total Harmonic Distortion (THD)	Full	I		–72.7	–61.7	dB
Spurious-Free Dynamic Range (SFDR)	Full	I	62.8	74.6		dB
ADC Sample Clock = PLL						
Signal-to-Noise and Distortion (SINAD)	Full	II	60.4	64.4		dB
Effective Number of Bits (ENOBs)	Full	II	9.74	10.4		Bits
Signal-to-Noise Ratio (SNR)	Full	II	62.4	65.1		dB
Total Harmonic Distortion (THD)	Full	II		–72.7	–61.8	dB
Spurious-Free Dynamic Range (SFDR)	Full	II	62.7	74.6		dB
Dynamic Performance (A_{IN} = –0.5 dBFS, f = 50 MHz)						
ADC Sample Clock = OSCIN						
Signal-to-Noise and Distortion (SINAD)	Full	II	59.4	62.9		dB
Effective Number of Bits (ENOB)	Full	II	9.5	10.1		Bits
Signal-to-Noise Ratio (SNR)	Full	II	61.6	63.7		dB
Total Harmonic Distortion (THD)	Full	II		–71.7	–61.5	dB
Spurious-Free Dynamic Range (SFDR)	Full	II	62.5	72		dB
Differential Phase	25°C	III		<0.1		Degrees
Differential Gain	25°C	III		<1		LSB
VIDEO ADC PERFORMANCE (f = 5 MHz)						
ADC Sample Clock = OSCIN						
Signal-to-Noise and Distortion (SINAD)	Full	II	46.7	53		dB
Signal-to-Noise Ratio (SNR)	Full	II	54.3	63.2		Bits
Total Harmonic Distortion (THD)	Full	II		–50.2	–45.9	dB
Spurious-Free Dynamic Range (SFDR)	Full	II	45.9	50		dB

PARAMETER	Temp	Test Level	Min	Typ	Max	Unit
CHANNEL-TO-CHANNEL ISOLATION						
Tx DAC-to-ADC Isolation (5 MHz Analog Output)						
Isolation between Tx and 10-Bit ADC	25°C	III		>60		dB
Isolation between Tx and 12-Bit ADCs	25°C	III		>80		dB
ADC-to-ADC Isolation						
(A_{IN} = –0.5 dBFS, f = 5 MHz)						
Isolation between IF10 and IF12A/B	25°C	III		>85		dB
Isolation between IF12A and IF12B	25°C	III		>85		dB
TIMING CHARACTERISTICS (10 pF LOAD)						
Wake-Up Time	N/A	N/A			200	T_{MCLK} cycles
Minimum RESET Pulsewidth Low (t_{RL})	N/A	N/A	5			t_{MCLK} cycles
Digital Output Rise/Fall Time	Full	II	2.8		4	ns
Tx/Rx Interface						
MCLK Frequency (f_{MCLK})	Full	II			66	MHz
TxSYNC/TxIQ Setup Time (t_{SU})	Full	II	3			ns
TxSYNC/TxIQ Hold Time (t_{HD})	Full	II	3			ns
MCLK Rising Edge to RxSYNC Valid Delay (t_{MD})	Full	II	0		1.0	ns
OSCOUT Rising or Falling Edge to						
RxSYNC Valid Delay (t_{OD})	Full	II	$T_{OSC}/4 - 2.0$		$T_{OSC}/4 + 3.0$	ns
OSCOUT Edge to MCLK Falling Edge (t_{EE})	Full	II	–1.0		+1.0	ns
SERIAL CONTROL BUS						
Maximum SCLK Frequency (f_{SCLK})	Full	II			15	MHz
Minimum Clock Pulsewidth High (t_{PWH})	Full	II	30			ns
Minimum Clock Pulsewidth Low (t_{PWL})	Full	II	30			ns
Maximum Clock Rise/Fall Time	Full	II			1	µs
Minimum Data/Chip-Select Setup Time (t_{DS})	Full	II	25			ns
Minimum Data Hold Time (t_{DH})	Full	II	0			ns
Maximum Data Valid Time (t_{DV})	Full	II			30	ns
CMOS LOGIC INPUTS						
Logic "1" Voltage	25°C	II	$V_{DRVDD} - 0.7$			V
Logic "0" Voltage	25°C	II			0.4	V
Logic "1" Current	25°C	II			12	µA
Logic "0" Current	25°C	II			12	µA
Input Capacitance	25°C	III		3		pF
CMOS LOGIC OUTPUTS (1 mA Load)						
Logic "1" Voltage	25°C	II	$V_{DRVDD} - 0.6$			V
Logic "0" Voltage	25°C	II			0.4	V
POWER SUPPLY						
Supply Current, I_S (Full Operation)	25°C	II		184	204	mA
Analog Supply Current I_{AS}	25°C	III		105	115	mA
Digital Supply Current I_{DS}	25°C	III		79	89	mA
Supply Current, I_S						
Standby ($\overline{PWRDN}$ Pin Active)	25°C	II		46	53	mA
Full Power-Down (Register 02 = 0xFF)	25°C	III		46	52	mA
Power-Down Tx Path (Register 02 = 0x60)	25°C	III		124		mA
Power-Down IF12 Rx Paths (Register 02 = 0x1B)	25°C	III		131	159	mA
Power Supply Rejection (Differential Signal)						
Tx DAC	25°C	III		<0.25		% FS
10-Bit ADC	25°C	III		<0.0001		% FS
12-Bit ADC	25°C	III		<0.0004		% FS

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Power Supply (V_{AVDD}, V_{DVDD}, V_{DRVDD})	3.9 V
Digital Output Current	5 mA
Digital Inputs	–0.3 V to V_{DRVDD} + 0.3 V
Analog Inputs	–0.3 V to V_{AVDD} + 0.3 V
Operating Temperature	–40°C to +85°C
Maximum Junction Temperature	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C

Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

EXPLANATION OF TEST LEVELS

I. Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for industrial operating temperature range (–40°C to +85°C).

II. Parameter is guaranteed by design and/or characterization testing.

III. Parameter is a typical value only.

N/A. Test level definition is not applicable.

THERMAL CHARACTERISTICS

Thermal Resistance:

100-Lead LQFP: θ_{JA} = 40.5°C/W

DEFINITIONS OF SPECIFICATIONS

Differential Nonlinearity Error (DNL, No Missing Codes)
An ideal converter exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 10-bit resolution indicates that all 1,024 codes, respectively, must be present over all operating ranges.

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Phase Noise
Single-sideband phase noise power is specified relative to the carrier (dBc/Hz) at a given frequency offset (1 kHz) from the carrier. Phase noise can be measured directly in single-tone transmit mode with a spectrum analyzer that supports noise marker measurements. It detects the relative power between the carrier and the offset (1 kHz) sideband noise and takes the resolution bandwidth (rbw) into account by subtracting 10 × log(rbw). It also adds a correction factor that compensates for the implementation of the resolution bandwidth, log display, and detector characteristic.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Spurious-Free Dynamic Range (SFDR)
The difference, in dB, between the rms amplitude of the DAC's output signal (or ADC's input signal) and the peak spurious signal over the specified bandwidth (Nyquist bandwidth, unless otherwise noted).

Pipeline Delay (Latency)
The number of clock cycles between conversion initiation and the associated output data being made available.

Offset Error
The first code transition should occur at an analog value ½ LSB above negative full scale. Offset error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value ½ LSB above negative full scale. The last transition should occur for an analog value 1½ LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Aperture Delay
The aperture delay is a measure of the Sample-and-Hold Amplifier (SHA) performance that specifies the time delay between the rising edge of the sampling clock input to when the input signal is held for conversion.

Aperture Uncertainty (Jitter)
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the ADC.

Input Referred Noise
The rms output noise is measured using histogram techniques. The ADC output codes' standard deviation is calculated in LSB, and converted to an equivalent voltage. This results in a noise figure that can be directly referred to the input of the MxFE.

Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Effective Number of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, it is possible to get a measure of performance expressed as N, the effective number of bits: $N = (SINAD - 1.76)dB/6.02$ Thus, the effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal, and is expressed as a percentage or in decibels.

Power Supply Rejection
Power supply rejection specifies the converter's maximum full-scale change when the supplies are varied from nominal to minimum and maximum specified voltages.

Channel-to-Channel Isolation (Crosstalk)
In an ideal multichannel system, the signal in one channel will not influence the signal level of another channel. The channel-to-channel isolation specification is a measure of the change that occurs in a grounded channel as a full-scale signal is applied to another channel.

TYPICAL PERFORMANCE CHARACTERISTICS

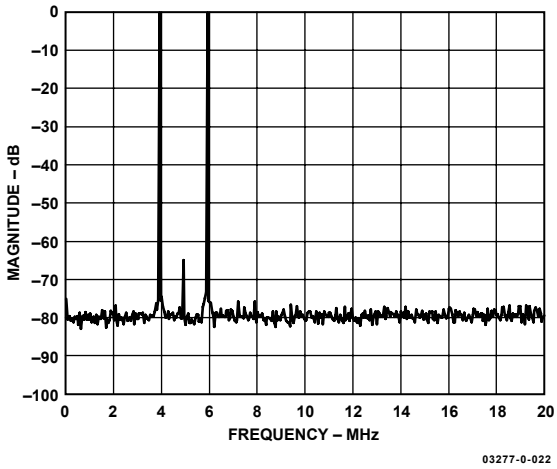

Figure 2. Dual Sideband Spectral Plot, f_C = 5 MHz, f = 1 MHz, R_{SET} = 10 kΩ (I_{OUT} = 4 mA), RBW = 1 kHz

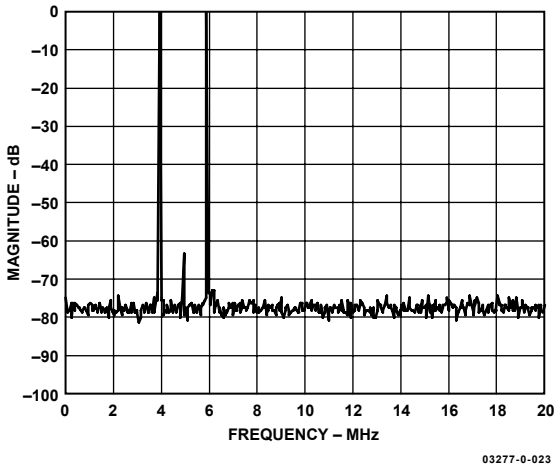

Figure 3. Dual Sideband Spectral Plot, f_C = 5 MHz, f = 1 MHz, R_{SET} = 4 kΩ (I_{OUT} = 10 mA), RBW=1 kHz

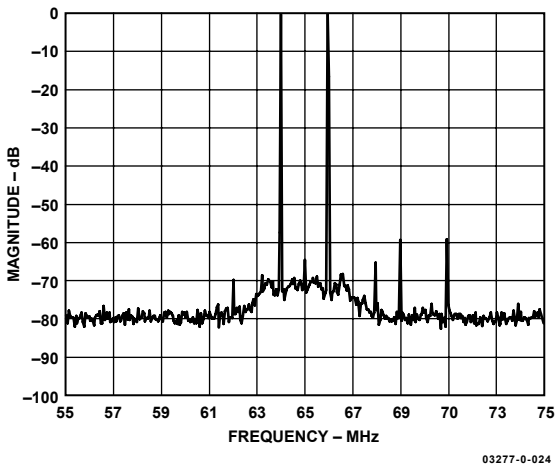

Figure 4. Dual Sideband Spectral Plot, f_C = 65 MHz, f = 1 MHz, R_{SET} = 10 kΩ (I_{OUT} = 4 mA), RBW = 1 kHz

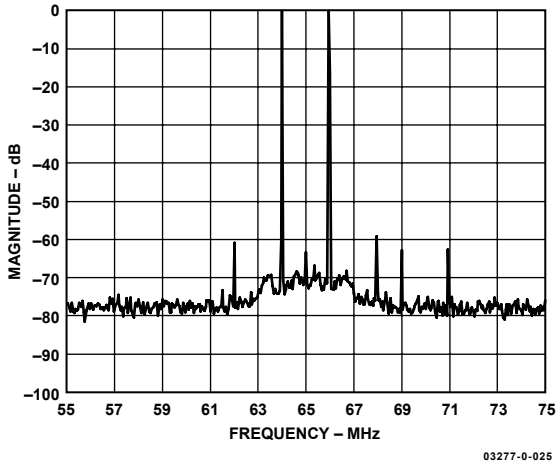

Figure 5. Dual Sideband Spectral Plot, f_C = 65 MHz, f = 1 MHz, R_{SET} = 4 kΩ (I_{OUT} = 10 mA), RBW = 1 kHz

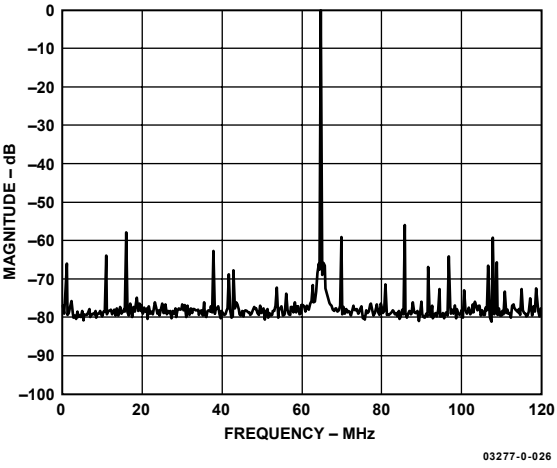

Figure 6. Single Sideband @ 65 MHz, RBW = 2 kHz, f_C = 66 MHz, f = 1 MHz, R_{SET} = 10 kΩ (I_{OUT} = 4 mA)

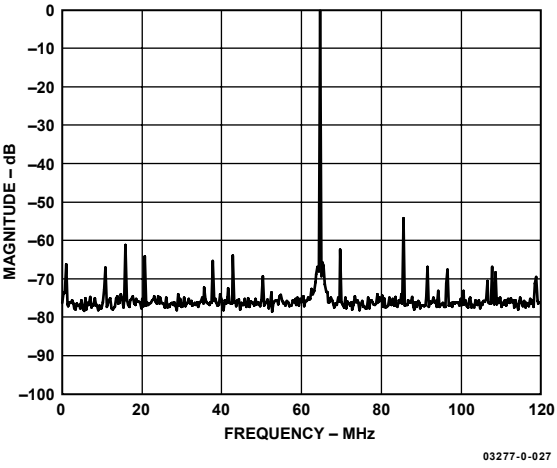

Figure 7. Single Sideband @ 65 MHz, RBW = 2 kHz, f_C = 66 MHz, f = 1 MHz, R_{SET} = 4 kΩ (I_{OUT} = 10 mA)

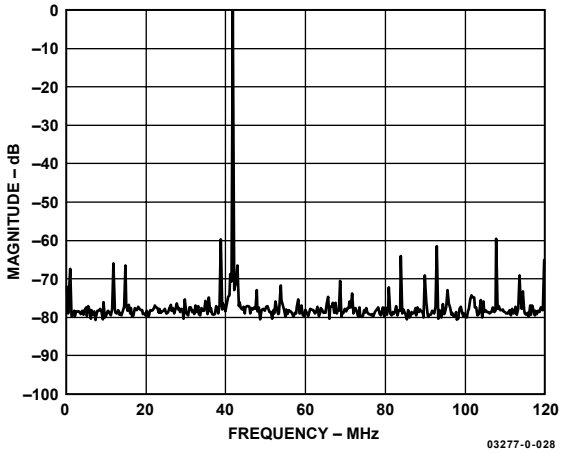

Figure 8. Single Sideband @ 42 MHz, RBW = 2 kHz ,f_C = 43 MHz, f = 1 MHz, R_{SET} = 10 kΩ (I_{OUT} = 4 mA)

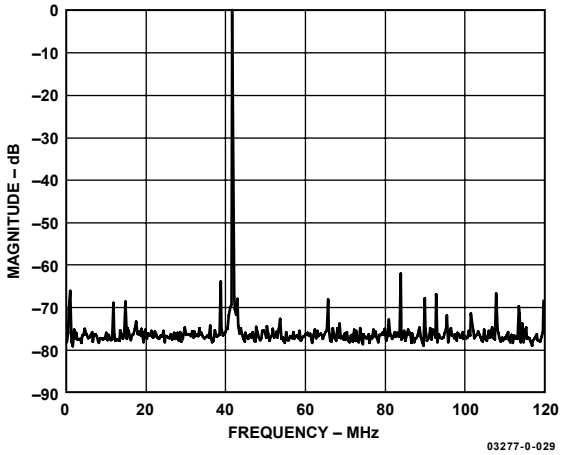

Figure 9. Single Sideband @ 42 MHz, RBW = 2 kHz, f_C = 43 MHz, f = 1 MHz, R_{SET} = 4 kΩ (I_{OUT} = 10 mA)

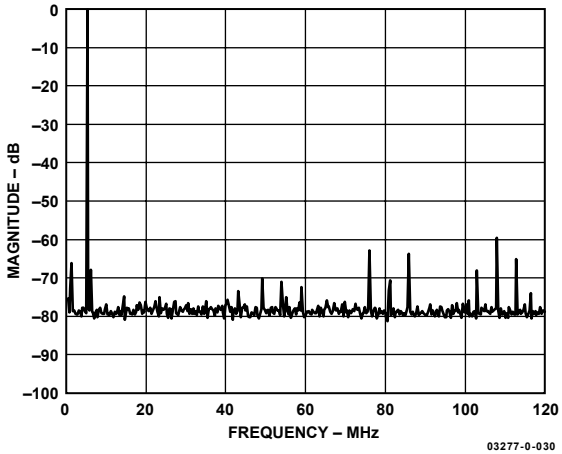

Figure 10. Single Sideband @ 5 MHz, RBW = 2 kHz, f_C = 6 MHz, f = 1 MHz, R_{SET} = 10 kΩ (I_{OUT} = 4 mA)

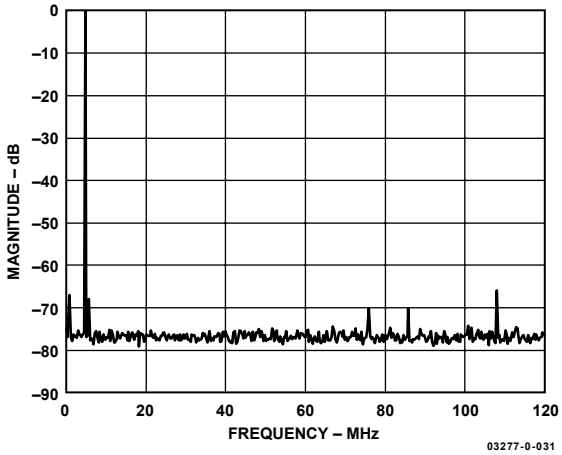

Figure 11. Single Sideband @ 5 MHz, RBW = 2 kHz, f_C = 6 MHz, f = 1 MHz, R_{SET} = 4 kΩ (I_{OUT} = 10 mA)

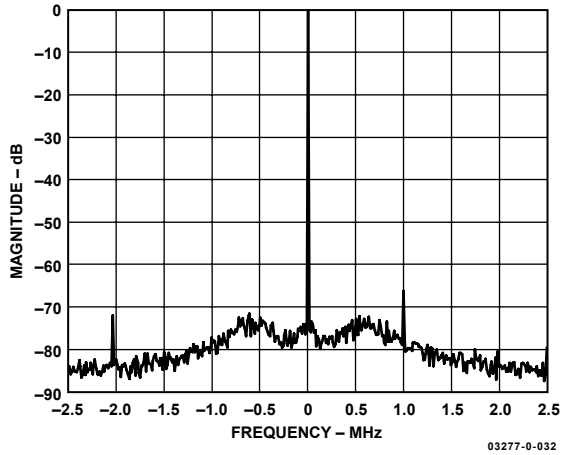

Figure 12. Single Sideband @ 65 MHz, RBW = 500 Hz, f_C = 66 MHz, f = 1 MHz, R_{SET} = 10 kΩ (I_{OUT} = 4 mA)

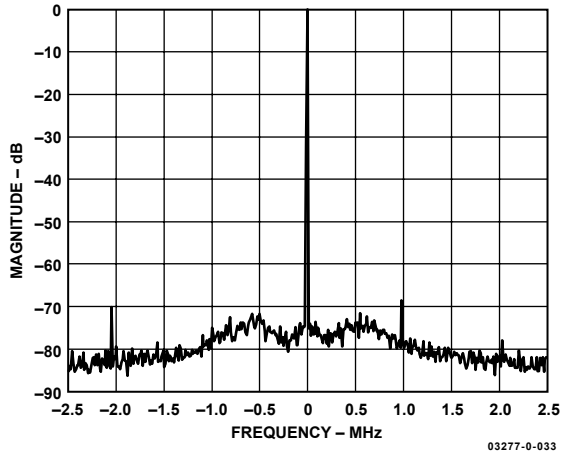

Figure 13. Single Sideband @ 65 MHz, RBW = 500 Hz, f_C = 66 MHz, f = 1 MHz, R_{SET} = 4 kΩ (I_{OUT} = 10 mA)

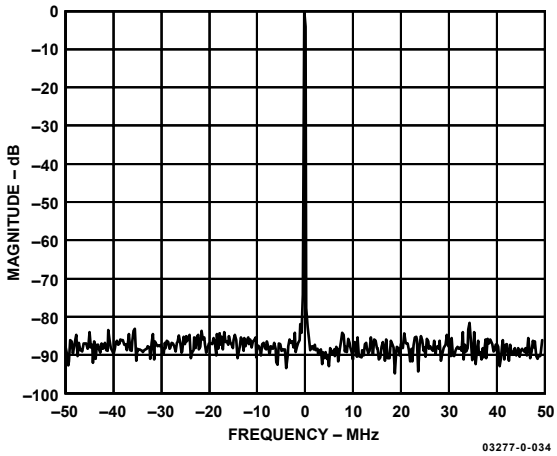

Figure 14. Single Sideband @ 65 MHz, RBW = 50 Hz, f_C = 66 MHz, f = 1 MHz, R_{SET} = 10 kΩ (I_{OUT} = 4 mA)

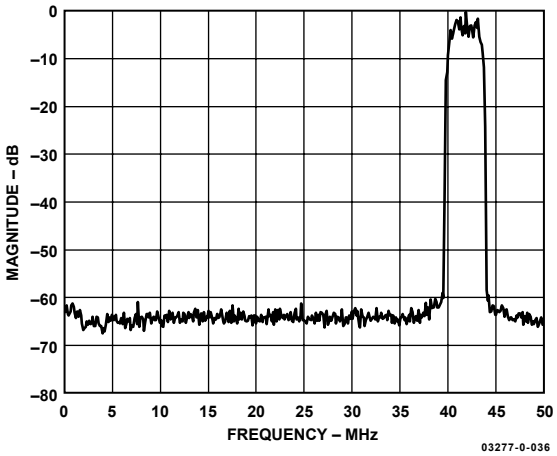

Figure 16. 16-QAM @ 42 MHz Spectral Plot, RBW = 1 kHz

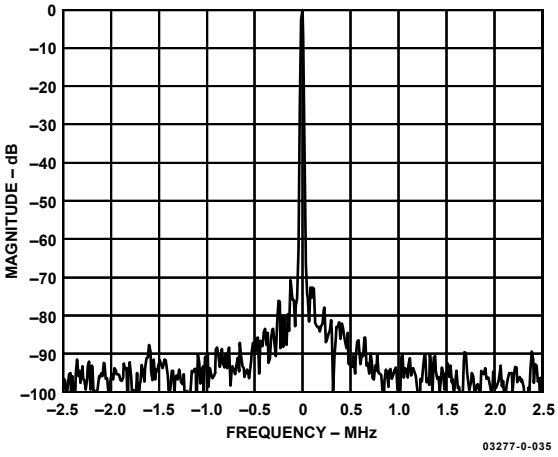

Figure 15. Single Sideband @ 65 MHz, RBW = 10 Hz, f_C = 66 MHz, f = 1 MHz, R_{SET} = 10 kΩ (I_{OUT} = 4 mA)

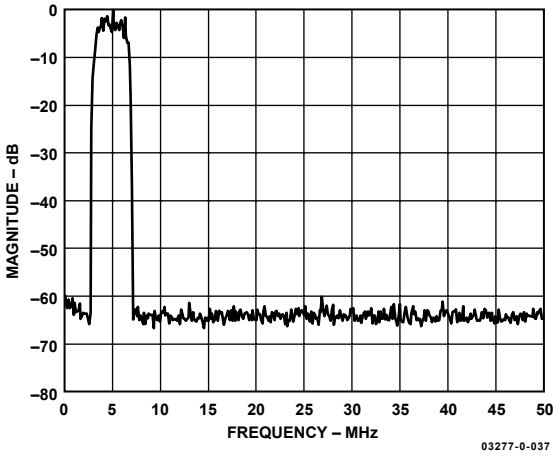

Figure 17. 16-QAM @ 5 MHz Spectral Plot, RBW = 1 kHz

REGISTER BIT DEFINITIONS

Table 3. AD9878 Register Map

Address (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (hex)	Type
00	SDIO Bidirectional	LSB First	Reset	OSC IN Multiplier M[4:0]					0x08	Read/Write
01	PLL Lock Detect	MCLK Divider R[5:0]							0x00	Read/Write
02	Power Down PLL	Power Down DAC Tx	Power Down Digital Tx	Power Down ADC12A	Power Down ADC12B	Power Down ADC10	Power Down Reference ADC12A	Power Down Reference ADC12B	0x00	Read/Write
03			Video Input into ADC12B	Flag 2			Flag 1	Flag 0 Enable	0x00	Read/Write
04	Flag 0	Sigma-Delta Output Control Word [7:0]							0x00	Read/Write
05									0x00	Read/Write
06									0x00	Read-Only
07	Video Input Enable	Clamp Level for Vidio Input [6:0]							0x00	Read/Write
08	ADC Clocked Direct from OSCIN		Rx Port Fast Edge Rate	Power Down Rx Sync Gen	Power-Down Reference ADC10		Send ADC12A Data Only	Send ADC12B Data Only	0x80	Read/Write
09									0x00	Read/Write
0A									0x00	Read/Write
0B									0x00	Read/Write
0C					Version [3:0]				0x00	Read/Write
0D					Tx Frequency Tuning Word Profile 1 LSBs [1:0]		Tx Frequency Tuning Word Profile 0 LSBs [1:0]		0x00	Read/Write
0E					DAC Fine Gain Control [3:0]				0x00	Read/Write
0F			Tx Path Select Profile 1		Tx Path AD8321/3 Gain Control Mode	Tx Path Bypass $sinc^{-1}$ Filter	Tx Path Spectral Inversion	Tx Path Transmit Single Tone	0x00	Read/Write
10	Tx Path Frequency Tuning Word Profile 0 [9:2]								0x00	Read/Write
11	Tx Path Frequency Tuning Word Profile 0 [17:10]								0x00	Read/Write
12	Tx Path Frequency Tuning Word Profile 0 [25:18]								0x00	Read/Write
13	Cable Driver Amplifier Coarse Gain Control Profile 0 [7:4]				Fine Gain Control Profile 0 [3:0]				0x00	Read/Write
14	Tx Path Frequency Tuning Word Profile 1 [9:2]								0x00	Read/Write
15	Tx Path Frequency Tuning Word Profile 1 [17:10]								0x00	Read/Write
16	Tx Path Frequency Tuning Word Profile 1 [25:18]								0x00	Read/Write
17	Cable Driver Amplifier Coarse Gain Control Profile 1 [7:4]				Fine Gain Control Profile 1 [3:0]				0x00	Read/Write

REGISTER 0—INITIALIZATION

Bits 0 to 4: OSCIN Multiplier

This register field is used to program the on-chip multiplier (PLL) that generates the chip's high frequency system clock, f_{SYSCLK}. For example, to multiply the external crystal clock f_{OSCIN} by 16 decimal, program Register 0, Bits 4:0 as 0x10. The default value of M is 0x08. Valid entries range from 1 to 31. When M is chosen equal to 1, the PLL is disabled and all internal clocks are derived directly from OSCIN. The PLL requires 200 MCLK cycles to regain frequency lock after a change in M, the clock multiplier value. After the recapture time of the PLL, the frequency of f_{SYSCLK} is stable.

Bit 5: Reset

Writing a 1 to this bit resets the registers to their default values and restarts the chip. The Reset bit always reads back 0. The bits in Register 0 are not affected by this software reset. However, a low level at the $\overline{\text{RESET}}$ pin would force all registers, including all bits in Register 0, to their default state.

Bit 6: LSB First

Active high indicates SPI serial port access of instruction byte and data registers is least significant bit (LSB) first. Default low indicates most significant bit (MSB) first format.

Bit 7: SDIO Bidirectional

Active high configures the serial port as a three signal port with the SDIO pin used as a bidirectional input/output pin. Default low indicates the serial port uses four signals with SDIO configured as an input and SDO configured as an output.

REGISTER 1—CLOCK CONFIGURATION

Bits [5:0]: MCLK Divider.

This register determines the output clock on the OSCOUT pin. At default 0 (R = 0), OSCOUT provides a buffered version of the OSCIN clock signal for other chips. The register can also be used to divide the chip's master clock f_{MCLK} by R, where R is an integer number between 2 and 63. The generated reference clock on OSCOUT pin can be used for external frequency controlled devices.

Bit 7: PLL Lock Detect

When this bit is set low, the OSCOUT pin functions in its default mode and provides an output clock with frequency f_{MCKL}/R as described above. If this bit is set to 1, the OSCOUT pin is configured to indicate whether the PLL is locked to f_{OSCIN}. In this mode the OSCOUT pin should be low-pass filtered with an RC filter of 1.0 kΩ and 0.1 μF. A high output on OSCOUT indicates that the PLL has achieved lock with f_{OSCIN}.

REGISTER 2—POWER-DOWN

Sections of the chip that are not used can be powered down when the corresponding bits are set high. This register has a default value of 0x00; all sections active.

Bit 0: Power-Down ADC 12B Voltage Reference

Active high powers down the voltage reference circuit for ADC12B.

Bit 1: Power-Down ADC12A Voltage Reference

Active high powers down the voltage reference circuit for ADC12A.

Bit 2: Power-Down ADC10

Active high powers down the 10-bit ADC.

Bit 3: Power-Down ADC12B

Active high powers down the ADC12B.

Bit 4: Power-Down ADC12A

Active high powers down the ADC12A.

Bit 5: Power-Down Tx

Active high powers down the digital transmit section of the chip, similar to the function of the $\overline{\text{PWRDN}}$ pin.

Bit 6: Power-Down DAC Tx

Active high powers down the DAC.

Bit 7: Power-Down PLL

Active high powers down the OSCIN multiplier.

REGISTER 3—FLAG CONTROL

Bit 0: Flag 0 Enable

Active high, the SDELTA pin will maintain a fixed logic level determined directly by the MSB of the sigma-delta control word of Register 4.

Bit 1: Flag 1

The logic level of this bit will be applied at the FLAG1 pin.

Bit 4: Flag 2

The logic level of this bit will be applied at the FLAG2 pin.

Bit 5: Video Input into ADC12B

If the video input is enabled, setting this bit high sends the signal applied to the VIDEO IN pin to the ADC12B. Otherwise, the signal applied to the VIDEO IN pin is sent to the ADC12A.

REGISTER 4—SIGMA-DELTA CONTROL WORD

Bits [7:0]: Sigma-Delta Control Word

The sigma-delta control word is 8 bits wide and controls the duty cycle of the digital output on the SIGDELT pin. Changes to the sigma-delta control word take effect immediately for every register write. Sigma-delta output control words have a default value of 0. The control words are in straight binary format with 0x00 corresponding to the bottom of scale or 0% duty cycle, and 0xFF corresponding to the top of scale or near 100% duty cycle.

Bit 7: Flag 0 (Sigma-Delta Control Word MSB)

When the Flag 0 Enable bit (Register 3, Bit 0) is set, the logic level of this bit will appear on the output of the SIGDELT pin.

REGISTER 07—VIDEO INPUT CONFIGURATION

Bits [6:0]: Clamp Level Control Value

The 7-bit clamp level control value is used to set an offset to the automatic clamp level control loop. The actual ADC output will have a clamp level offset equal to 16 times the clamp level control value as shown:

Clamp Level Offset Clamp Level Control Value = (x)16

The default value for the clamp level control value is 0x20. This results in an ADC output clamp level offset of 512 LSBs. The valid programming range for the clamp level control value is from 0x16 to 0x127.

REGISTER 8—ADC CLOCK CONFIGURATION

Bit 0: Send ADC12B Data Only

When this bit is set high, the device enters a nonmultiplexed mode and only the data from the ADC12B will be sent to the IF[11:0] digital output port.

Bit 1: Send ADC12A Data Only

When this bit is set high, the device enters a nonmultiplexed mode and only the data from the ADC12A will be sent to the IF[11:0] digital output port.

Note: If both the Send ADC12B Data Only and Send ADC12A Data Only register bits are set high, the device will send both ADC12A and ADC12B data in multiplexed mode.

Bit 3: Power-Down ADC10 Voltage Reference

Active high powers down the voltage reference circuit for ADC10.

Bit 4: Power Down RxSYNC Generator

Setting this bit to 1 powers down the 10-bit ADC's sampling clock and makes the RxSYNC output pin stay low. It can be used for additional power saving on top of the power-down selections in Register 2.

Bit 5: Rx PORT Fast Edge Rate

Setting this bit to 1 increases the output drive strength of all digital output pins except MCLK, REFCLK, SIGDELT, and FLAG[2:1]. These pins always have high output drive capability.

Bit 7: ADC Clocked Directly from OSCIN

When set high, the ADC sampling clock is derived directly from the input clock at OSCIN. In this mode, the clock supplied to the OSCIN pin should originate from an external crystal or low jitter crystal oscillator. When this bit is low, the ADC sampling clock is derived from the internal PLL and the frequency of the clock is equal to $f_{OSCIN} \times M/8$.

REGISTER C—DIE REVISION

Bits [3:0]: Version

The die version of the chip can be read from this register.

REGISTER D—Tx FREQUENCY TUNING WORDS LSBS

This register accommodates the two least significant bits each for both of the frequency tuning words. See the description of the burst parameter below.

REGISTER E—DAC GAIN CONTROL

This register allows the user to program the DAC gain if the TxGain Control Select Bit 3 in Register F is set to 0.

Bits [3:0]	DAC Gain (dB)
0000	0.0 (default)
0001	0.5
0010	1.0
0011	1.5
…	…
1110	7.0
1111	7.5

REGISTER F—Tx PATH CONFIGURATION

Bit 0: Single Tone Tx Mode

Active high configures the AD9878 for single-tone applications (e.g., FSK). The AD9878 will supply a single frequency output as determined by the frequency tuning word selected by the active profile. In this mode, the TxIQ input data pins are ignored but should be tied to a valid logic voltage level. Default value is 0 (inactive).

Bit 1: Spectral Inversion Tx

When set to 1, inverted modulation is performed:

$$MODULATOR\_OUT = [I\cos(\omega t) + Q\sin(\omega t)].$$

Default is logic 0, non-inverted modulation:

$$MODULATOR\_OUT = [I\cos(\omega t) - Q\sin(\omega t)].$$

Bit 2: Bypass Inv Sinc Tx Filter

Active high, configures the AD9878 to bypass the sin(x)/x compensation filter. Default value is 0 (inverse sinc filter enabled).

Bit 3: CA Interface Mode Select

This bit changes the manner in which transmit gain control is performed. Typically either AD8321/AD8323 (default 0) or AD8322/AD8327 (1) variable gain cable amplifiers are programmed over the chip's 3-wire CA interface. The Tx Gain Control Select changes the interpretation of the bits in Registers 13, 17, 1B, and 1F. See the Cable Driver Gain Control section below.

Bit 5: Profile Select

The AD9878 quadrature digital upconverter is capable of storing two preconfigured modulation modes called profiles. Each profile defines a transmit frequency tuning word and cable driver amplifier gain (/DAC gain) setting. The Profile Select bit or PROFILE pin programs the current register profile to be used. The Profile Select bit should always be 0 if the PROFILE pin is used to switch between profiles. Using the Profile Select bit as a means of switching between different profiles requires the PROFILE pin to be tied low.

REGISTERS 10 THROUGH 17: BURST PARAMETER

Tx Frequency Tuning Words

The frequency tuning word (FTW) determines the DDS generated carrier frequency (f_C) and is formed via a concatenation of register addresses.

The 26-bit FTW is spread over four register addresses. Bit 25 is the MSB and Bit 0 is the LSB. The carrier frequency equation is given as:

$$f_C = (FTW \times f_{SYSCLK})/2^{26}$$

where :

$f_{SYSCLK} = M \times f_{OSCIN}$, and $FTW <$ 0x2000

Changes to FTW bytes take effect immediately.

Cable Driver Gain Control

The AD9878 has a 3-pin interface to the AD832x family of programmable gain cable driver amplifiers. This allows direct control of the cable driver's gain through the AD9878. In its default mode, the complete 8-bit register value is transmitted over the 3-wire cable amplifier (CA) interface. If Bit 3 of Register F is set high, Bits [7:4] of Registers 0x13 and 0x17 will determine the 8-bit word sent over the CA interface according to the table below:

Bits [7:4]	CA Interface Transmit Word
0000	0000 0000 (default)
0001	0000 0001
0010	0000 0010
0011	0000 0100
0100	0000 1000
0101	0001 0000
0110	0010 0000
0111	0100 0000
1000	1000 0000

In this mode the lower bits of Registers 0x13 and 0x17 determine the fine gain setting of the DAC output:

Bits [3:0]	DAC Fine Gain (dB)
0000	0.0 (default)
0001	0.5
0010	1.0
0011	1.5
...	...
1110	7.0
1111	7.5

New data is automatically sent over the 3-wire CA interface (and DAC gain adjust) whenever the value of the active gain control register changes or a new profile is selected. The default value is 0x00 (lowest gain).

The formula for the combined output level calculation of AD9878 fine gain and AD8327 or AD8322 coarse gain is:

$$V_{8327} = V_{9878(0)} + (fine)/2 + (coarse) - 19$$

$$V_{8322} = V_{9878(0)} + (fine)/2 + (coarse) - 14$$

where:

fine = decimal value of Bits [3:0]

coarse = decimal value of Bits [7:4]

$V_{9878(0)}$: Level at AD9878 output in dBmV for *fine* = 0.

V_{8327}: Level at output of AD8327 in dBmV.

V_{8322}: Level at output of AD8322 in dBmV.

SERIAL INTERFACE FOR REGISTER CONTROL

The AD9878 serial port is a flexible, synchronous serial communications port that allows easy interface to many industry standard microcontrollers and microprocessors. The interface allows read/write access to all registers that configure the AD9878. Single or multiple byte transfers are supported. Also, the interface can be programmed to read words either MSB first or LSB first. The AD9878's serial interface port I/O can be configured to have one bidirectional I/O (SDIO) pin or two unidirectional I/O (SDIO/SDO) pins.

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD9878. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9878, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9878 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle.

The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9878.

The eight remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9878 and the system controller. Phase 2 of the communication cycle is a transfer of 1 to 4 data bytes as determined by the instruction byte. Normally, using one multi-byte transfer is the preferred method. However, single-byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

Instruction Byte

The instruction byte contains the following information:

MSB 17	16	15	14	13	12	11	LSB 10
R/W	N1	N0	A4	A3	A2	A1	A0

The R/W bit of the instruction byte determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates a read operation. Logic low indicates a write operation. The [N1:N0] bits determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table 4. The timing diagrams are shown in Figure 18 and Figure 19.

Table 4.

N1	N0	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

The Bits [A4:A0] determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9878.

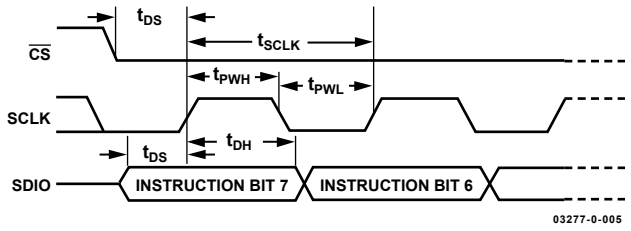

Figure 18. Timing Diagram for Register Write

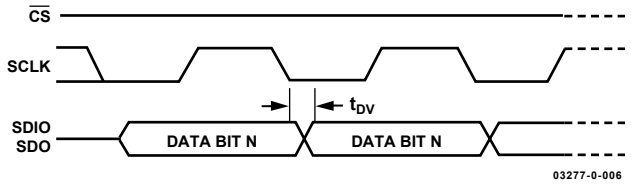

Figure 19. Timing Diagram for Register Read

Serial Interface Port Pin Description

SCLK—Serial Clock. The serial clock pin is used to synchronize data transfers from the AD9878 and to run the serial port state machine. The maximum SCLK frequency is 15 MHz. Input data to the AD9878 is sampled on the rising edge of SCLK. Output data changes on the falling edge of SCLK.

$\overline{CS}$—Chip Select. Active low input starts and gates a communication cycle. It allows multiple devices to share a common serial port bus. The SDO and SDIO pins go to a high impedance state when $\overline{CS}$ is high. Chip select should stay low during the entire communication cycle.

SDIO—Serial Data I/O. Data is always written into the AD9878 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 7 of Register 0. The default is Logic 0, which configures the SDIO pin as unidirectional.

SDO—Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9878 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB Transfers

The AD9878 serial port can support most significant bit (MSB) first or least significant bit (LSB) first data formats (see Figure 20 and Figure 21). This functionality is controlled by the LSB First bit in Register 0. The default mode is MSB First. When this bit is set active high, the AD9878 serial port is in LSB First format. In LSB First mode, the instruction byte and data bytes must be written from the least significant bit to the most significant bit. In LSB First mode, the serial port internal byte address generator increments for each byte of the multibyte communication cycle.

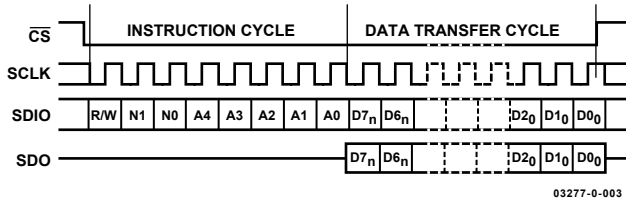

Figure 20. Serial Register Interface Timing, MSB First

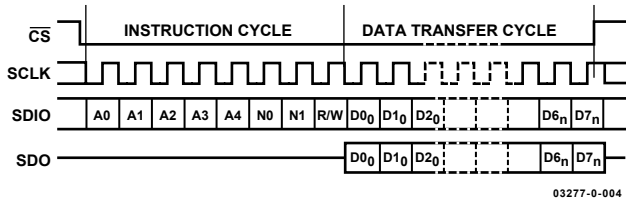

Figure 21. Serial Register Interface Timing, LSB First

When this bit is set default low, the AD9878 serial port is in MSB First format. In MSB First mode, the instruction byte and data bytes must be written from the most significant bit to the least significant bit. In MSB First mode, the serial port internal byte address generator decrements for each byte of the multibyte communication cycle.

When incrementing from 0x1F, the address generator changes to 0x00. When decrementing from 0x00, the address generator changes to 0x1F.

Notes on Serial Port Operation

The AD9878 serial port configuration bits reside in Bits 6 and 7 of Register Address 0x00. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register may occur during the middle of the communication cycle. Measures must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply when setting the Reset bit in Register Address 0x00. All other registers are set to their default values, but the software reset does not affect the bits in Register Address 0x00. It is recommended to use only single-byte transfers when changing serial port configurations or initiating a software reset. A write to Bits 1, 2, and 3 of Address 0x00 with the same logic levels as Bits 7, 6, and 5 (bit pattern: XY1001YX binary) allows the user to reprogram a lost serial port configuration and to reset the registers to their default values. A second write to Address 0x00 with the Reset bit low and the serial port configuration as specified above (XY), reprograms the OSCIN multiplier setting. A changed f_{SYSCLK} frequency is stable after a maximum of 200 f_{MCLK} cycles (wake-up time).

THEORY OF OPERATION

For a general understanding of the AD9878, refer to Figure 22, a block diagram of the device architecture. The device consists of a transmit path, receive path, and auxiliary functions, such as a PLL, a sigma-delta DAC, a serial control port, and a cable amplifier interface.

The transmit path contains an interpolation filter, a complete quadrature digital up-converter, an inverse sinc filter, and a 12-bit current output DAC.

The receive path contains a 10-bit ADC and a dual 12-bit ADC. All internally required clocks and an output system clock are generated by the PLL from a single crystal or clock input.

The 12-bit and 10-bit IF ADCs can convert direct IF inputs up to 70 MHz and run at sample rates up to 33 MSPS. A video input with an adjustable signal clamping level along with the 10-bit ADC allow the AD9878 to process an NTSC and a QAM channel simultaneously.

The programmable sigma-delta DAC can be used to control external components, such as variable gain amplifiers (VGAs) or voltage controlled tuners. The CAPORT provides an interface to the AD8321/AD8323 or AD8322/AD8327 programmable gain amplifier (PGA) cable drivers, enabling host processor control via the MxFE serial port (SPORT).

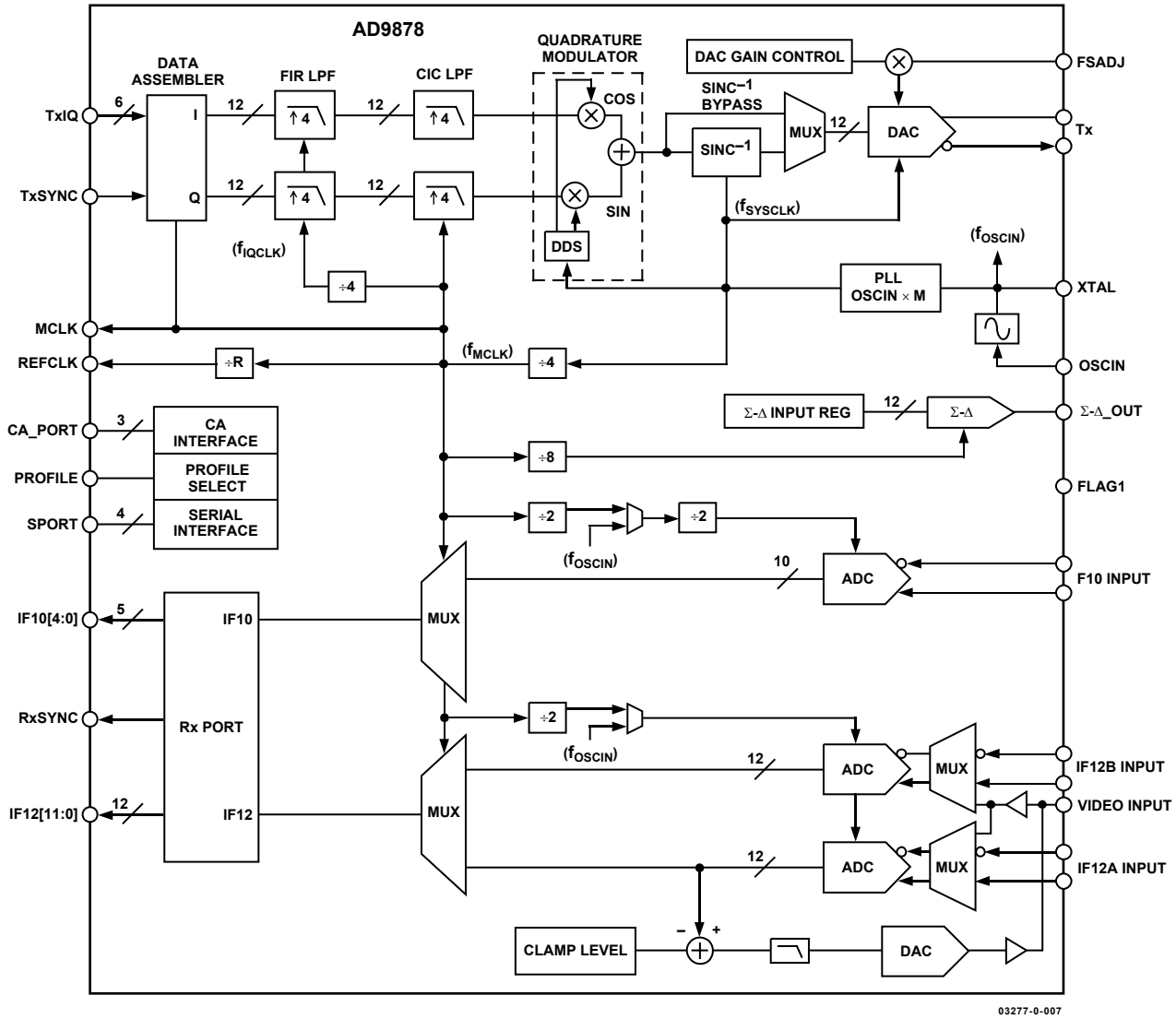

Figure 22. AD9878 Block Diagram

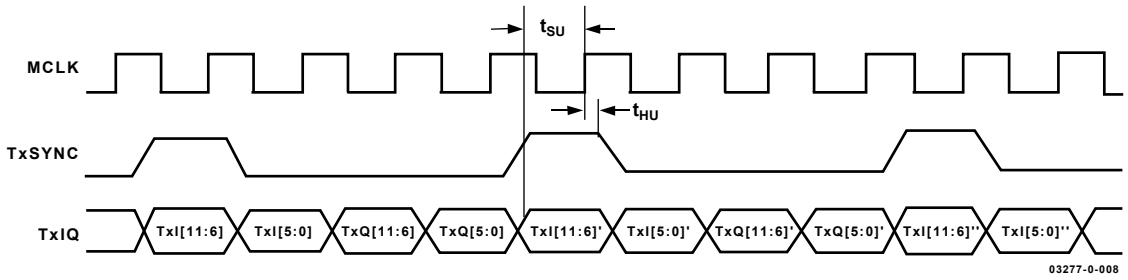

Figure 23. Tx Timing Diagram

Transmit Path

The transmit path contains an interpolation filter, a complete quadrature digital up-converter, an inverse sinc filter, and a 12-bit current output DAC. The maximum output current of the DAC is set by an external resistor. The Tx output PGA provides additional transmit signal level control. The transmit path interpolation filter provides an up-sampling factor of 16 with an output signal bandwidth as high as 5.8 MHz. Carrier frequencies up to 65 MHz with 26 bits of frequency tuning resolution can be generated by the direct digital synthesizer (DDS). The transmit DAC resolution is 12 bits and it can run at sampling rates up to 232 MSPS. Analog output scaling from 0 dB to 7.5 dB in 0.5 dB steps is available to preserve SNR when reduced output levels are required.

DATA ASSEMBLER

The AD9878 data path operates on two 12-bit words, the I and Q components, that form a complex symbol. The data assembler builds the 24-bit complex symbols from four consecutive 6-bit words read over the TxIQ [5:0] bus. These words are strobed into the data assembler synchronous to the master clock (MCLK). A high level on TxSYNC signals the start of a transmit symbol. The first two 6-bit words of the symbol form the I component; the second two 6-bit words form the Q component. Symbol components are assumed to be in twos complement format. The timing of the interface is fully described in the Transmit Timing section. The I/Q sample rate f_{IQCLK} puts a bandwidth limit on the maximum transmit spectrum. This is the familiar Nyquist limit (hereafter referred to as f_{NYQ}) and is equal to one-half f_{IQCLK}.

TRANSMIT TIMING

The AD9878 provides a master clock MCLK and expects 6-bit multiplexed TxIQ data on each rising edge (see Figure 23). Transmit symbols are framed with the TxSYNC input. TxSYNC high indicates the start of a transmit symbol. Four consecutive 6-bit data packages form a symbol (I MSB, I LSB, Q MSB, and Q LSB).

INTERPOLATION FILTER

Once through the Data Assembler, the IQ data streams are fed through a 4× FIR low-pass filter and a 4× Cascaded Integrator Comb (CIC) low-pass filter. The combination of these two filters results in the sample rate increasing by a factor of 16×. In addition to the sample rate increase, the half-band filters provide the low-pass filtering characteristic necessary to suppress the spectral images between the original sampling frequency and the new (16× higher) sampling frequency.

HALF-BAND FILTERS (HBFs)

HBF 1 and HBF 2 are both interpolating filters, each of which doubles the sampling rate. Together, HBF 1 and HBF 2 have 26 taps and provide a factor of four increase in the sampling rate ($4 \times f_{IQCLK}$ or $8 \times f_{NYQ}$).

In relation to phase response, both HBFs are linear phase filters. As such, virtually no phase distortion is introduced within the pass band of the filters. This is an important feature, as phase distortion is generally intolerable in a data transmission system.

CASCADED INTEGRATOR COMB (CIC) FILTER

The CIC filter is configured as a programmable interpolator and provides a sample rate increase by a factor of 4. The frequency response of the CIC filter is given by:

$$|H(f)| = \left[\left(\frac{1}{4}\right)\frac{1-e^{-j(2\pi f(4))}}{1-e^{j2\pi f}}\right]^3 = \left[\left(\frac{1}{4}\right)\frac{\sin(4\pi f)}{\sin(\pi f)}\right]^3$$

COMBINED FILTER RESPONSE

The combined frequency response of the HBF and CIC filters puts a limit on the input signal bandwidth that can be propagated through the AD9878.The usable bandwidth of the filter chain puts a limit on the maximum data rate that can be propagated through the AD9878. A look at the pass-band detail of the combined filter response (Figure 24) indicates that in order to maintain an amplitude error of no more than 1 dB, signal bandwidth is restricted to no more than about 60% of f_{NYQ}. Thus, in order to keep the bandwidth of the data in the flat portion of the filter pass band, the user must oversample the

baseband data by at least a factor of two prior to presenting it to the AD9878. Note that without oversampling, the Nyquist bandwidth of the base-band data corresponds to f_{NYQ}. As such, the upper end of the data bandwidth will suffer 6 dB or more of attenuation due to the frequency response of the digital filters. Furthermore, if the baseband data applied to the AD9878 has been pulse shaped, there is an additional concern. Typically, pulse shaping is applied to the baseband data via a filter having a raised cosine response. In such cases, an α value is used to modify the bandwidth of the data where the value of α is such that:

$$0 < \alpha < 1.$$

A value of 0 causes the data bandwidth to correspond to the Nyquist bandwidth. A value of 1 causes the data bandwidth to be extended to twice the Nyquist bandwidth. Thus, with 2× oversampling of the baseband data and α = 1, the Nyquist bandwidth of the data will correspond with the I/Q Nyquist bandwidth. As stated earlier, this results in problems near the upper edge of the data bandwidth due to the frequency response of the filters. The maximum value of α that can be implemented is 0.45. This is because the data bandwidth becomes:

$$1/2 \cdot (1+\alpha) f_{NYQ} = 0.725 f_{NYQ}$$

which puts the data bandwidth at the extreme edge of the flat portion of the filter response.

If a particular application requires an α value between 0.45 and 1, then the user must oversample the baseband data by at least a factor of four. Over the frequency range of the data to be transmitted, the combined HB1, HB2, and CIC filter introduces a worst-case droop of less than 0.2 dB.

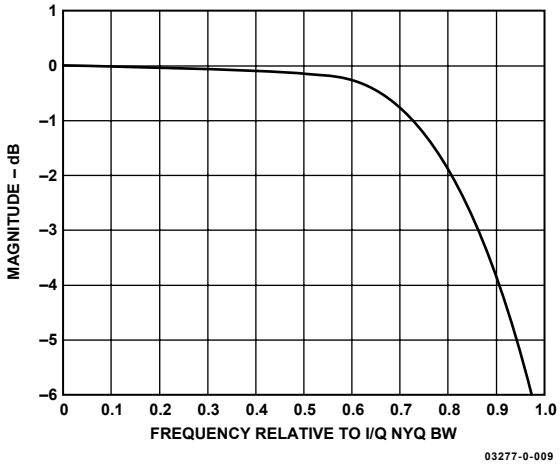

Figure 24. Cascaded Filter Pass Band

DIGITAL UPCONVERTER

The digital quadrature modulator stage following the CIC filters is used to frequency shift (upconvert) the baseband spectrum of the incoming data stream up to the desired carrier frequency. The carrier frequency is controlled numerically by a direct digital synthesizer (DDS). The DDS uses the internal system clock (f_{SYSCLK}) to generate the desired carrier frequency with a high degree of precision. The carrier is applied to the I and Q multipliers in quadrature fashion (90° phase offset) and summed to yield a data stream that is the modulated carrier. The modulated carrier becomes the 12-bit sample sent to the DAC.

Tx SIGNAL LEVEL CONSIDERATIONS

The quadrature modulator itself introduces a maximum gain of 3 dB in signal level. To visualize this, assume that both the I data and Q data are fixed at the maximum possible digital value, *x*. Then the output of the modulator, *z*, is

$$z = \left[x\cos(\omega t) - x\sin(\omega t)\right]$$

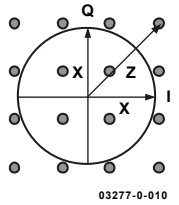

Figure 25. 16-Quadrature Modulation

It can be shown that $|z|$ assumes a maximum value of $|z| = \sqrt{x^2 + x^2} = x\sqrt{2}$ (a gain of +3 dB). However, if the same number of bits were used to represent the $|z|$ values that were used to represent the *x* values, an overflow would occur. To prevent this possibility, an effective –3 dB attenuation is internally implemented on the I and Q data path:

$$|z| = \sqrt{1/2 + 1/2} = x$$

The following example assumes a PK/rms level of 10 dB:

Maximum Symbol Component Input Value =
±2047 *LSBs* – 0.2 *dB* = ±2000 *LSBs*

Maximum Complex Input RMS Value =

2000 *LSBs* ± 6 *dB* – *Pk rms* (*dB*) = *1265 LSBs rms*

The maximum complex input rms value calculation uses both I and Q symbol components that add a factor of 2 (= 6 dB) to the formula. Table 5 shows typical I-Q input test signals with amplitude levels related to 12-bit full scale (FS).

Table 5. I–Q Input Test Signals

Analog Output	Digital Input	Input Level	Modulator Output Level
Single Tone ($f_C - f$)	I = cos(f) Q = cos(f + 90°) = –sin(f)	FS – 0.2 dB FS – 0.2 dB	FS – 3.0 dB
Single Tone ($f_C + f$)	I = cos(f) Q = cos(f + 270°) = +sin(f)	FS – 0.2 dB FS – 0.2 dB	FS – 3.0 dB
Dual Tone ($f_C \pm f$)	I = cos(f) FS – 0.2 dB FS Q = cos(f + 180°) = –cos(f) or Q = +cos(f)	FS – 0.2 dB FS – 0.2 dB	FS

Tx THROUGHPUT AND LATENCY

Data inputs affect the output fairly quickly but remain effective due to the AD9878's filter characteristics. Data transmit latency through the AD9878 is easiest to describe in terms of f_{SYSCLK} clock cycles ($4 \times f_{MCLK}$). The numbers quoted are when an effect is first seen after an input value change.

Latency of I/Q data entering the data assembler (AD9878 input) to the DAC output is 119 f_{SYSCLK} clock cycles (29.75 f_{MCLK} cycles). DC values applied to the data assembler input will take up to 176 f_{SYSCLK} clock cycles (44 f_{MCLK} cycles) to propagate and settle at the DAC output.

Frequency hopping is accomplished via changing the PROFILE input pin. The time required to switch from one frequency to another is less than 232 f_{SYSCLK} cycles (58.5 f_{MCLK} cycles).

D/A CONVERTER

A 12-bit digital-to-analog converter (DAC) is used to convert the digitally processed waveform into an analog signal. The worst-case spurious signals due to the DAC are the harmonics of the fundamental signal and their aliases (see the Analog Devices DDS Tutorial at www.analog.com/dds). The conversion process will produce aliased components of the fundamental signal at $n \times f_{SYSCLK} \pm f_{CARRIER}$ ($n = 1, 2, 3$). These are typically filtered with an external RLC filter at the DAC output. It is important for this analog filter to have a sufficiently flat gain and linear phase response across the bandwidth of interest so as to avoid modulation impairments. A relatively inexpensive seventh order elliptical low-pass filter is sufficient to suppress the aliased components for HFC network applications.

The AD9878 provides true and complement current outputs. The full-scale output current is set by the R_{SET} resistor at Pin 49 and the DAC Gain register. Assuming maximum DAC gain, the value of R_{SET} for a particular full-scale I_{OUT} is determined using the equation:

$$R_{SET} = 32\ V_{DACRSET}/I_{OUT} = 39.4/I_{OUT}$$

For example, if a full-scale output current of 20 mA is desired, then R_{SET} = (39.4/0.02), or approximately 2 kΩ.

The following equation calculates the full-scale output current including the programmable DAC gain control.

$$I_{OUT} = 39.4/R_{SET} \times 10^{(-7.5 + 0.5NGAIN)/20}$$

where N_{GAIN} is the value of DAC Fine Gain Control[3:0].

The full-scale output current range of the AD9878 is 4 mA to 20 mA. Full-scale output currents outside of this range will degrade SFDR performance. SFDR is also slightly affected by output matching; that is, the two outputs should be terminated equally for best SFDR performance. The output load should be located as close as possible to the AD9878 package to minimize stray capacitance and inductance. The load may be a simple resistor to ground, an op amp current-to-voltage converter, or a transformer-coupled circuit. It is best not to attempt to directly drive highly reactive loads, such as an LC filter. Driving an LC filter without a transformer requires that the filter be doubly terminated for best performance; that is, the filter input and output should both be resistively terminated with the appropriate values. The parallel combination of the two terminations will determine the load that the AD9878 sees for signals within the filter pass band. For example, a 50 Ω terminated input/output low-pass filter will look like a 25 Ω load to the AD9878. The output compliance voltage of the AD9878 is –0.5 V to +1.5 V. Any signal developed at the DAC output should not exceed +1.5 V; otherwise signal distortion will result. Furthermore, the signal may extend below ground as much as 0.5 V without damage or signal distortion. The AD9878 true and complement outputs can be differentially combined for common-mode rejection using a broadband 1:1 transformer.

Using a grounded center tap results in signals at the AD9878 DAC output pins that are symmetrical about ground. As previously mentioned, by differentially combining the two signals, the user can provide some degree of common-mode signal rejection.

A differential combiner might consist of a transformer or an op amp. The object is to combine or amplify only the difference between two signals and to reject any common—usually undesirable—characteristic, such as 60 Hz hum or clock feed-through that is equally present on both individual signals.

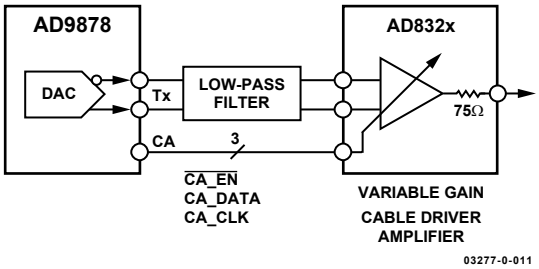

Figure 26. Cable Amplifier Connection

Connecting the AD9878 true and complement outputs to the differential inputs of the programmable gain cable drivers AD8321/AD8323 or AD8322/AD8327 (see Figure 26) provides an optimized solution for the standard compliant cable modem upstream channel. The cable driver's gain can be programmed through a direct 3-wire interface using the AD9878's profile registers.

PROGRAMMING THE AD8321/AD8323 OR AD8322/AD8327 CABLE DRIVER AMPLIFIER

Programming the gain of the AD832x family of cable driver amplifiers can be accomplished via the AD9878 cable amplifier control interface. Two 8-bit registers within the AD9878 (one per profile) store the gain value to be written to the serial 3-wire port. Typically, either the AD8321/AD8323 or AD8322/AD8327 variable gain cable amplifiers are connected to the chip's 3-wire cable amplifier interface. The Tx Gain Control Select bit in Register 0x0F changes the interpretation of the bits in Registers 0x13, 0x17, 0x1B, and 0x1F. See Figure 27 and Cable Driver Gain Control Register description.

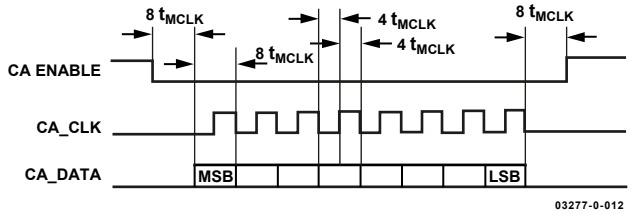

Figure 27. Cable Amplifier Interface Timing

Data transfers to the programmable gain cable driver amplifier are initiated by four conditions:

1. Power-Up and Hardware Reset—Upon initial power-up and every hardware reset, the AD9878 clears the contents of the Gain Control registers to 0, which defines the lowest gain setting of the AD832x. Thus, the AD9878 writes all 0s out of the 3-wire cable amplifier control interface.

2. Software Reset—Writing a 1 to Bit 5 of Address 0x00 initiates a software reset. On a software reset, the AD9878 clears the contents of the Gain Control registers to 0 for the lowest gain and sets the Profile Select to 0. The AD9878 writes all 0s out of the 3-wire cable amplifier control interface if the gain was on a different setting (different from 0) before.

3. Change in Profile Selection—The AD9878 samples the PROFILE input pin together with the two Profile Select bits and writes to the AD832x Gain Control registers when a change in profile and gain is determined. The data written to the cable driver amplifier comes from the AD9878 Gain Control register associated with the current profile.

4. Write to the AD9878 Cable Driver Amplifier Control Registers—The AD9878 will write gain control data associated with the current profile to the AD832x whenever the selected AD9878 cable driver amplifier gain setting is changed. Once a new stable gain value has been detected (48 to 64 MCLK cycles after initiation) data write starts with $\overline{\text{CA\_EN}}$ going low. The AD9878 will always finish a write sequence to the cable driver amplifier once it is started. The logic controlling data transfers to the cable driver amplifier uses up to 200 MCLK cycles and has been designed to prevent erroneous write cycles from ever occurring.

OSCIN CLOCK MULTIPLIER

The AD9878 can accept either an input clock into the OSCIN pin or a fundamental mode crystal across the OSCIN and XTAL pins as the device's main clock source. The internal PLL then generates the f_{SYSCLK} signal from which all other internal signals are derived. The DAC uses f_{SYSCLK} as its sampling clock. For DDS applications, the carrier is typically limited to about 30% of f_{SYSCLK}. For a 65 MHz carrier, the system clock required is above 216 MHz. The OSCIN multiplier function maintains clock integrity as evidenced by the AD9878 system's excellent phase noise characteristics and low clock-related spur in the output spectrum.

External loop filter components consisting of a series resistor (1.3 kΩ) and capacitor (0.01 μF) provide the compensation zero for the OSCIN multiplier PLL loop. The overall loop performance has been optimized for these component values.

CLOCK AND OSCILLATOR CIRCUITRY

The AD9878's internal oscillator generates all sampling clocks from a simple, low cost, parallel resonance, fundamental frequency quartz crystal. Figure 28 shows how the quartz crystal is connected between OSCIN (Pin 61) and XTAL (Pin 60) with parallel resonant load capacitors as specified by the crystal manufacturer. The internal oscillator circuitry can also be overdriven by a TTL level clock applied to OSCIN with XTAL left unconnected.

$$f_{OSCIN} = f_{MCLK} \times M$$

An internal phase-locked loop (PLL) generates the DAC sampling frequency, f_{SYSCLK}, by multiplying the OSCIN frequency by M. The MCLK signal (Pin 23), f_{MCLK}, is derived by dividing f_{SYSCLK} by 4.

$$f_{SYSCLK} = f_{OSCIN} \times M$$

$$f_{MCLK} = f_{OSCIN} \times M/4$$

An external PLL loop filter (Pin 57) consisting of a series resistor and ceramic capacitor (Figure 28: R1 = 1.3 kΩ, C12 = 0.01 μF) is required for stability of the PLL. Also, a shield surrounding these components is recommended to minimize external noise coupling into the PLL's voltage controlled oscillator input (guard trace connected to AVDDPLL).

Figure 22 shows that ADCs are either sampled directly by a low jitter clock at OSCIN or by a clock that is derived from the PLL output. Operating modes can be selected in Register 8. Sampling the ADCs directly with the OSCIN clock requires MCLK programmed to be twice the OSCIN frequency.

PROGRAMMABLE CLOCK OUTPUT REFCLK

The AD9878 provides an auxiliary output clock on Pin 69, REFCLK. The value of the MCLK divider bit field, *R*, determines its output frequency as shown in the equations

$$f_{REFCLK} = f_{MCLK}/R, \text{ for } R = 2 \text{ to } 63$$

$$f_{REFCLK} = f_{OSCIN}, \text{ for } R = 0$$

In its default setting (0x00 in Register 1), the REFCLK pin provides a buffered output of f_{OSCIN}.

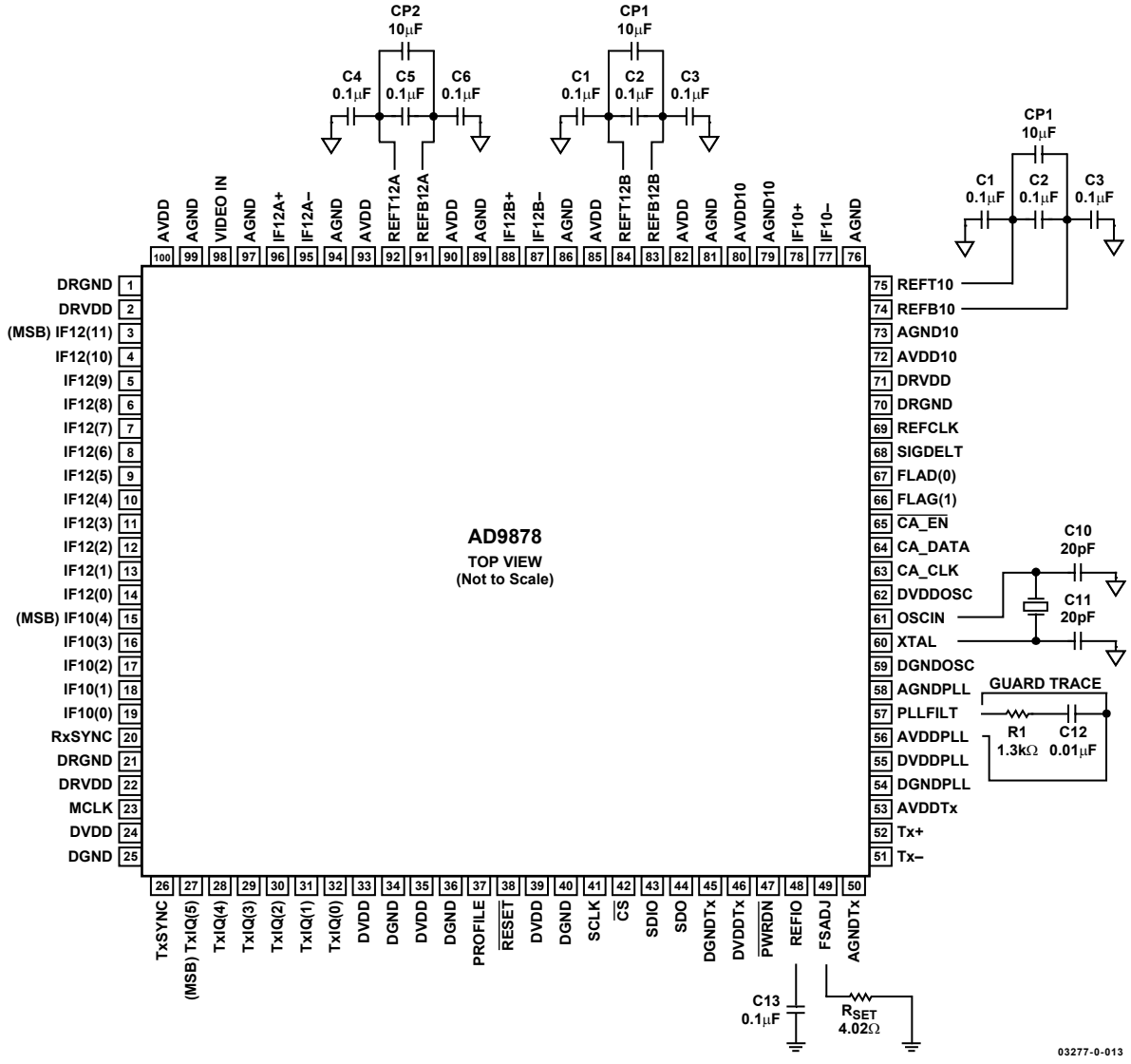

Figure 28. Basic Connection Diagram

RESET AND TRANSMIT POWER-DOWN

POWER-UP SEQUENCE

On initial power-up, the $\overline{\text{RESET}}$ pin should be held low until the power supply is stable (see Figure 29). Once $\overline{\text{RESET}}$ is deasserted, the AD9878 can be programmed over the serial port. The on-chip PLL requires a maximum of 1 ms after the rising edge of $\overline{\text{RESET}}$ or a change of the multiplier factor (M) to completely settle. It is recommended that the $\overline{\text{PWRDN}}$ pin be held low during the reset and PLL settling time. Changes to ADC Clock Select (Register 0x08) or Sys Clock Divider N (Register 0x01) should be programmed before the rising edge of $\overline{\text{PWRDN}}$. Once the PLL is frequency locked and after the $\overline{\text{PWRDN}}$ pin is brought high, transmit data can be sent reliably. If the $\overline{\text{PWRDN}}$ pin cannot be held low throughout the reset and PLL settling time period, then the Power-Down Digital Tx bit or the $\overline{\text{PWRDN}}$ pin should be pulsed after the PLL has settled. This will ensure correct transmit filter initialization.

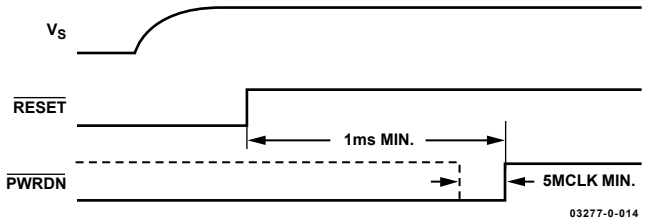

Figure 29. Power-Up Sequence for Tx Data Path

RESET

To initiate hardware reset, the $\overline{\text{RESET}}$ pin should be held low for at least 100 ns. All internally generated clocks except OSCOUT stop during reset. The rising edge of $\overline{\text{RESET}}$ resets the PLL clock multiplier and reinitializes the programmable registers to their default values. The same sequence as described above in the Power-Up Sequence section should be followed after a reset or change in M.

A software reset (writing a 1 into Bit 5 of Register 0x00) is functionally equivalent to the hardware reset but does not force Register 0x00 to its default value.

TRANSMIT POWER-DOWN

A low level on the $\overline{\text{PWRDN}}$ pin stops all clocks linked to the digital transmit data path and resets the CIC filter. Deasserting $\overline{\text{PWRDN}}$ reactivates all clocks. The CIC filter is held in a reset state for 80 MCLK cycles after the rising edge of $\overline{\text{PWRDN}}$ to allow for flushing of the half-band filters with new input data. Transmit data bursts should be padded with at least 20 symbols of null data directly before the $\overline{\text{PWRDN}}$ pin is deasserted. Immediately after the $\overline{\text{PWRDN}}$ pin is deasserted, the transmit burst should start with a minimum of 20 null data symbols (see Figure 30). This avoids unintended DAC output samples caused by the transmit path latency and filter settling time.

Software Power-Down Digital Tx (Bit 5 in Register 0x02) is functionally equivalent to the hardware $\overline{\text{PWRDN}}$ pin and takes effect immediately after the last register bit has been written over the serial port.

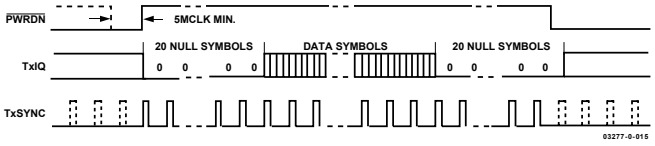

Figure 30. Timing Sequence to Flush Tx Data Path

SIGMA-DELTA OUTPUTS

The AD9878 contains an on-chip sigma-delta output that provides a digital logic bit stream with an average duty cycle that varies between 0% and (4095/4096)%, depending on the programmed code, as shown in Figure 31.

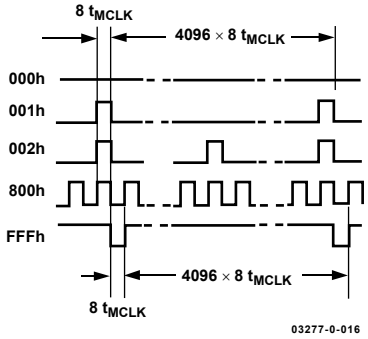

Figure 31. Sigma-Delta Output Signals

This bit stream can be low-pass filtered to generate a programmable dc voltage of:

$$V_{DC} = [(Sigma\text{-}Delta\ Code/4096) \times V_H] + V_L$$

where:

$$V_H = V_{DRVDD} - 0.6\ \text{V}$$

$$V_L = 0.4\ \text{V}$$

In cable modem set-top box applications, the output can be used to control external variable gain amplifiers or RF tuners. A simple single-pole RC low-pass filter provides sufficient filtering (see Figure 32).

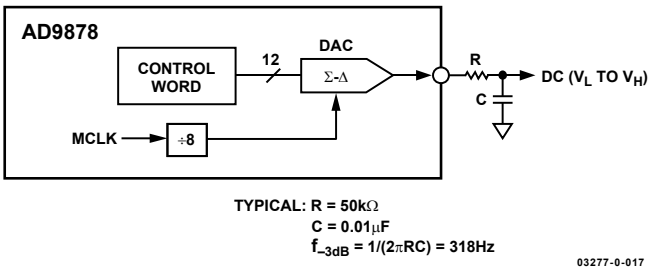

Figure 32. Sigma-Delta RC Filter

In more demanding applications where additional gain, level shift, or drive capability is required, a first or second order active filter might be considered (see Figure 33).

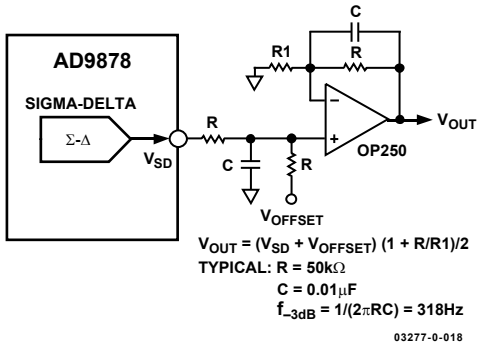

Figure 33. Sigma-Delta Active Filter with Gain and Offset

RECEIVE PATH (Rx)

The AD9878 includes three high speed, high performance ADCs. The 10-bit and dual 12-bit direct IF ADCs deliver excellent undersampling performance with input frequencies as high as 70 MHz. The sampling rate can be as high as 33 MSPS. The ADC sampling frequency can be derived directly from the OSCIN signal or from the on-chip OSCIN multiplier. For highest dynamic performance, it is recommended to choose an OSCIN frequency that can be directly used as the ADC sampling clock. Digital 12-bit ADC outputs are multiplexed to one 12-bit bus, clocked by a frequency (f_{MCLK}) of four times the sampling rate. The IF ADCs use a multiplexer to a 12-bit interface with an output word rate of f_{MCLK}.

IF10 AND IF12 ADC OPERATION

The IF10 and IF12 ADCs have a common architecture and share many of the same characteristics from an applications standpoint. Most of the information in the section below will be applicable to both IF ADCs. Differences, where they exist, will be highlighted.

INPUT SIGNAL RANGE AND DIGITAL OUTPUT CODES

The IF ADCs have differential analog inputs labeled IF+ and IF–. The signal input, V_{AIN}, is the voltage difference between the two input pins, $V_{AIN} = V_{IF+} - V_{IF-}$. The full-scale input voltage range is determined by the internal reference voltages, REFT and REFB, which define the top and bottom of the scale. The peak input voltage to the ADC is the difference between REFT and REFB, which is 1 V_{PD}. This results in the ADC full scale input voltage range of 2 V_{PPD}. The digital output code is straight binary and is illustrated in Table 6.

Table 6

IF12[11:0]	Input Signal Voltage
111...111	$V_{AIN} \geq +1.0$ V
111...111	$V_{AIN} = +1.0$ V – (1 LSB)
111...110	$V_{AIN} = +1.0$ V – (2 LSB)
...	…
100...001	$V_{AIN} = 0$ V + 1 LSB
100...000	$V_{AIN} = 0.0$ V
011...111	$V_{AIN} = 0$ V – 1 LSB
...	…
000...001	$V_{AIN} = -1.0$ V + (2 LSB)
000...000	$V_{AIN} = -1.0$ V
000...000	$V_{AIN} < -1.0$ V

DRIVING THE INPUT

The IF ADCs have differential switched capacitor sample-and-hold amplifier (SHA) inputs. The nominal differential input impedance is 4.0 kΩ||3 pF. This impedance can be used as the effective termination impedance when calculating filter transfer characteristics and voltage signal attenuation from nonzero source impedances. It should be noted, however, that for best performance, additional requirements must be met by the signal source. The SHA has input capacitors that must be recharged each time the input is sampled. This results in a dynamic input current at the device input, and demands that the source has low (<50 Ω) output impedance at frequencies up to the ADC sampling frequency. Also, the source must have settling to better than 0.1% in <1/2 ADC CLK period.

Another consideration for getting the best performance from the ADC inputs is the dc biasing of the input signal. Ideally, the signal should be biased to a dc level equal to the midpoint of the ADC reference voltages, REFT12 and REFB12. Nominally, this level will be 1.2 V. When ac-coupled, the ADC inputs will self-bias to this voltage and require no additional input circuitry. Figure 34 illustrates a recommended circuit that eases the burden on the signal source by isolating its output from the ADC input. The 33 Ω series termination resistors isolate the amplifier outputs from any capacitive load, which typically improves settling time. The series capacitors provide ac signal coupling which ensures that the ADC inputs operate at the

optimal dc bias voltage. The shunt capacitor sources the dynamic currents required to charge the SHA input capacitors, removing this requirement from the ADC buffer. The values of C_C and C_S should be calculated to get the correct HPF and LPF corner frequencies.

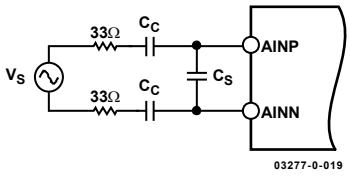

Figure 34. Simple ADC Drive Configuration

RECEIVE TIMING

The AD9878 sends multiplexed data to the IF10 and IF12 outputs on every rising edge of MCLK. RxSYNC frames the start of each IF10 data symbol. 10-bit and 12-bit ADCs are completely read on every second MCLK cycle. RxSYNC is high for every second 10-bit ADC data (if 10-bit ADC is not in power-down mode).The Rx timing diagram is shown in Figure 35.

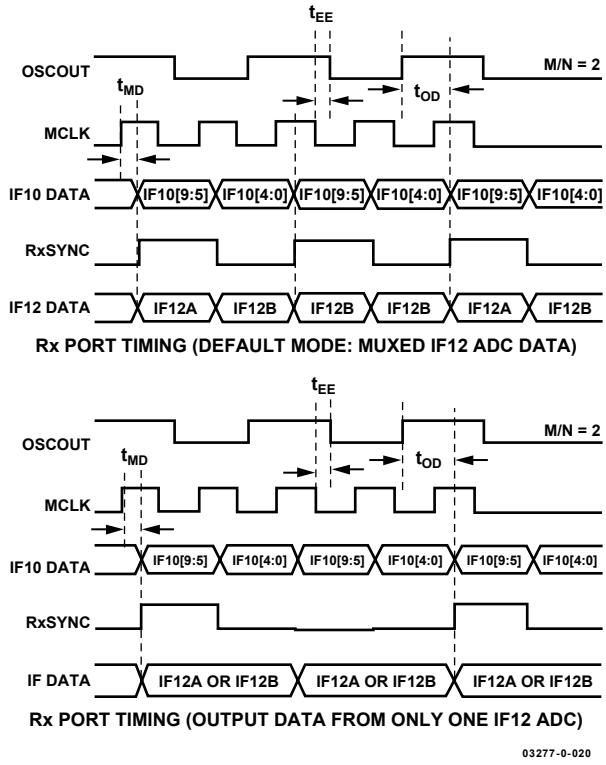

Figure 35. Rx Port Timing

ADC VOLTAGE REFERENCES

The AD9878 has three independent internal references for its 10-bit and 12-bit ADCs. Both 12-bit and 10-bit ADCs are designed for 2 V p-p input voltages with each of them having its own internal reference. Figure 28 shows the proper connections of the reference pins REFT and REFB. External references may be necessary for systems that require high accuracy gain matching between ADCs or for improvements in temperature drift and noise characteristics. External references REFT and REFB need to be centered at AVDD/2 with offset voltages as specified:

REFT-10, -12: AVDD/2 + 0.5 V
REFB-10, -12: AVDD/2 – 0.5 V

A differential level of 1 V between the reference pins results in a 2 V p-p ADC input level AIN. Internal reference sources can be powered down when external references are used (Register Address 0x02).

VIDEO INPUT

For sampling video-type waveforms, such as NTSC and PAL signals, the Video Input channel provides black level clamping. Figure 36 shows the circuit configuration for using the Video Channel input (Pin 98). An external blocking capacitor is used with the on-chip video clamp circuit to level-shift the input signal to a desired reference point. The clamp circuit automatically senses the most negative portion of the input signal, and adjusts the voltage across the input capacitor. This forces the black level of the input signal to be equal to the value programmed into the Clamp Level register (Register Address 0x07).Video Input can be multiplexed to the IF12A ADC (default) or to the IF12B ADC by programming Register Address 0x03.

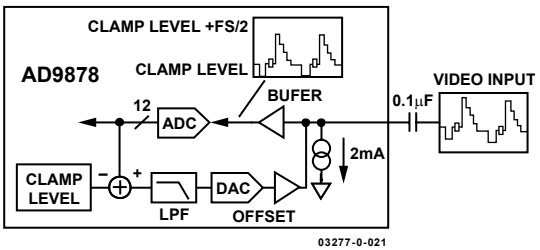

Figure 36. Video Clamp Circuit Input

PCB DESIGN CONSIDERATIONS

Although the AD9878 is a mixed-signal device, the part should be treated as an analog component. The digital circuitry on-chip has been specially designed to minimize the impact that the digital switching noise will have on the operation of the analog circuits. Following the power, grounding, and layout recommendations in this section will help the user get the best performance from the MxFE.

COMPONENT PLACEMENT

If the three following guidelines of component placement are followed, chances for getting the best performance from the MxFE are greatly increased.

- First, manage the path of return currents flowing in the ground plane so that high frequency switching currents from the digital circuits do not flow on the ground plane under the MxFE or analog circuits.
- Second, keep noisy digital signal paths and sensitive receive signal paths as short as possible.
- Third, keep digital (noise generating) and analog (noise susceptible) circuits as far away from each other as possible.

In order to best manage the return currents, pure digital circuits that generate high switching currents should be closest to the power supply entry. This will keep the highest frequency return current paths short, and prevent them from traveling over the sensitive MxFE and analog portions of the ground plane. Also, these circuits should be generously bypassed at each device to further reduce the high frequency ground currents. The MxFE should be placed adjacent to the digital circuits, such that the ground return currents from the digital sections will not flow in the ground plane under the MxFE. The analog circuits should be placed furthest from the power supply. The AD9878 has several pins that are used to decouple sensitive internal nodes. These pins are REFIO, REFB12A, REFT12A, REFB12B, REFT12B, REFB10, and REFT10. The decoupling capacitors connected to these points should have low ESR and ESL. The capacitors should be placed as close to the MxFE as possible and be connected directly to the analog ground plane. The resistor connected to the FSADJ pin and the RC network connected to the PLLFILT pin should also be placed close to the device and connected directly to the analog ground plane.

POWER PLANES AND DECOUPLING

The AD9878 evaluation board (Figure 38 and Figure 39) demonstrates a good power supply distribution and decoupling strategy. The board has four layers: two signal layers, one ground plane, and one power plane. The power plane is split into a 3 VDD section that is used for the 3 V digital logic circuits, a DVDD section that is used to supply the digital supply pins of the AD9878, an AVDD section that is used to supply the analog supply pins of the AD9878, and a VANLG section that supplies the higher voltage analog components on the board. The 3 VDD section will typically have the highest frequency currents on the power plane and should be kept the furthest from the MxFE and analog sections of the board.

The DVDD portion of the plane carries the current used to power the digital portion of the MxFE to the device. This should be treated similarly to the 3 VDD power plane and be kept from going underneath the MxFE or analog components. The MxFE should largely sit above the AVDD portion of the power plane. The AVDD and DVDD power planes may be fed from the same low noise voltage source; however, they should be decoupled from each other to prevent the noise generated in the DVDD portion of the MxFE from corrupting the AVDD supply. This can be done by using ferrite beads between the voltage source and DVDD, and between the source and AVDD. Both DVDD and AVDD should have a low ESR, bulk decoupling capacitor on the MxFE side of the ferrite as well as low ESR, ESL decoupling capacitors on each supply pin (i.e., the AD9878 requires 17 power supply decoupling capacitors). The decoupling capacitors should be placed as close to the MxFE supply pins as possible. An example of proper decoupling is shown in the AD9878 evaluation board schematic (Figure 38 and Figure 39).

GROUND PLANES

In general, if the component placing guidelines discussed earlier can be implemented, it is best to have at least one continuous ground plane for the entire board. All ground connections should be made as short as possible. This will result in the lowest impedance return paths and the quietest ground connections. If the components cannot be placed in a manner that would keep the high frequency ground currents from traversing under the MxFE and analog components, it may be necessary to put current steering channels into the ground plane to route the high frequency currents around these sensitive areas. These current steering channels should be made only when and where necessary.

SIGNAL ROUTING

The digital Rx and Tx signal paths should be kept as short as possible. Also, these traces should have a controlled impedance of about 50 Ω. This will prevent poor signal integrity and the high currents that can occur during undershoot or overshoot caused by ringing. If the signal traces cannot be kept shorter than about 1.5 inches, then series termination resistors (33 Ω to 47 Ω) should be placed close to all signal sources. It is a good idea to series terminate all clock signals at their source regardless of trace length. The receive signals are the most sensitive signals on the entire board. Careful routing of these signals is essential for good receive path performance. The IF+/IF– signals form a differential pair and should be routed together as a pair. By keeping the traces adjacent to each other, noise coupled onto the signals will appear as common mode and will be largely rejected by the MxFE receive input. Keeping the driving point impedance of the receive signal low and placing any low-pass filtering of the signals close to the MxFE will further reduce the possibility of noise corrupting these signals.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIOINS

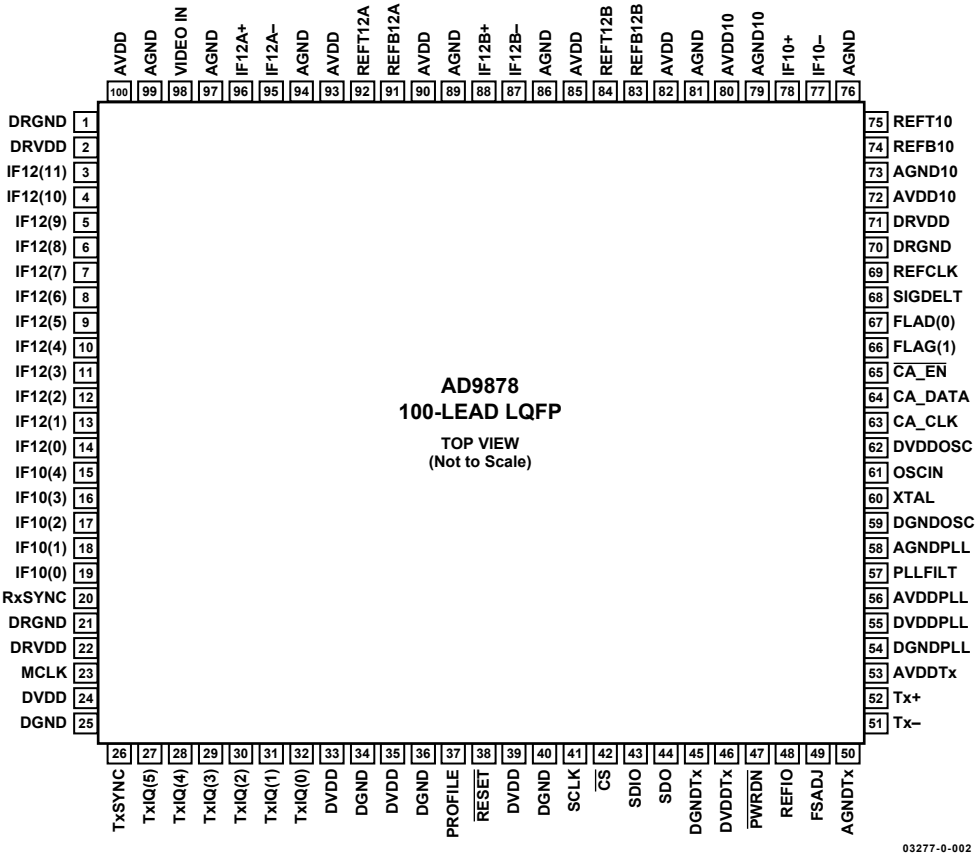

Figure 37. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Pin Function
1, 21, 70	DRGND	Pin Driver Digital Ground
2, 22, 71	DRVDD	Pin Driver Digital 3.3 V Supply
3–14	IF12[11:0]	12-Bit ADCs Digital Ouput
15–19	IF10[4:0]	10-Bit ADC Digital Ouput
20	RxSYNC	Sync Output, 10- and 12-Bit ADCs
23	MCLK	Master Clock Output
24, 35, 39	DVDD	Digital 3.3 V Supply
25, 34, 36, 40	DGND	Digital Ground
26	TxSYNC	Sync Input for Transmit Port
27:32	TxIQ[5:0]	Digital Input for Transmit Port
37	PROFILE	Profile Selection Input
38	$\overline{\text{RESET}}$	Chip Reset Input
41	SCLK	SPORT Clock
42	$\overline{\text{CS}}$	SPORT Chip Select
43	SDIO	SPORT Data I/O
44	SDO	SPORT Data Output
45	DGNDTx	Tx Path Digital Ground
46	DVDDTx	Tx Path Digital 3.3 V Supply
47	$\overline{\text{PWRDN}}$	Power-Down Transmit Path
48	REFIO	TxDAC Decoupling (to AGND)
49	FSADJ	DAC Output Adjust (External Res.)

Pin No.	Mnemonic	Pin Function
50	AGNDTx	Tx Path Analog Ground
51, 52	Tx–, Tx+	Tx Path Complementary Outputs
53	AVDDTx	Tx Path Analog 3.3 V Supply
54	DGNDPLL	PLL Digital Ground
55	DVDDPLL	PLL Digital 3.3 V Supply
56	AVDDPLL	PLL Analog 3.3 V Supply
57	PLLFILT	PLL Loop Filter Connection
58	AGNDPLL	PLL Analog Ground
59	DGNDOSC	Oscillator Digital Ground
60	XTAL	Crystal Oscillator Inverted Output
61	OSCIN	Oscillator Clock Input
62	DVDDOSC	Oscillator Digital 3.3 V Supply
63	CA_CLK	Serial Clock to Cable Driver
64	CA_DATA	Serial Data to Cable Driver
65	$\overline{\text{CA\_EN}}$	Serial Enable to Cable Driver
66, 67	FLAG[2:1]	Programmable Flag Outputs
68	SIGDELT	Sigma-Delta DAC Output
69	REFCLK	Reference Clock Output
72, 80	AVDD10	10-Bit ADC Analog 3.3 V Supply
73, 79	AGND10	10-Bit ADC Analog Ground
74	REFB10	10-Bit ADC Ref Decoupling Node
75	REFT10	10-Bit ADC Ref Decoupling Node
76, 81, 86, 89, 94, 97, 99	AGND	12-Bit ADC Analog Ground
77, 78	IF10-, IF10+	Differential Input to 10-bit ADC
82, 85, 90, 93, 100	AVDD	12-Bit ADC Analog 3.3 V Supply
83	REFB12B	ADC12B Ref Decoupling Node
84	REFT12B	ADC12B Ref Decoupling Node
87, 88	IF12B–, IF12B+	Differential Input to ADC12B
91	REFB12A	ADC12A Ref Decoupling Node
92	REFT12A	ADC12A Ref Decoupling Node
95, 96	IF12A–, IF12A+	Differential Input to ADC12A
98	VIDEO IN	Video Clamp Input

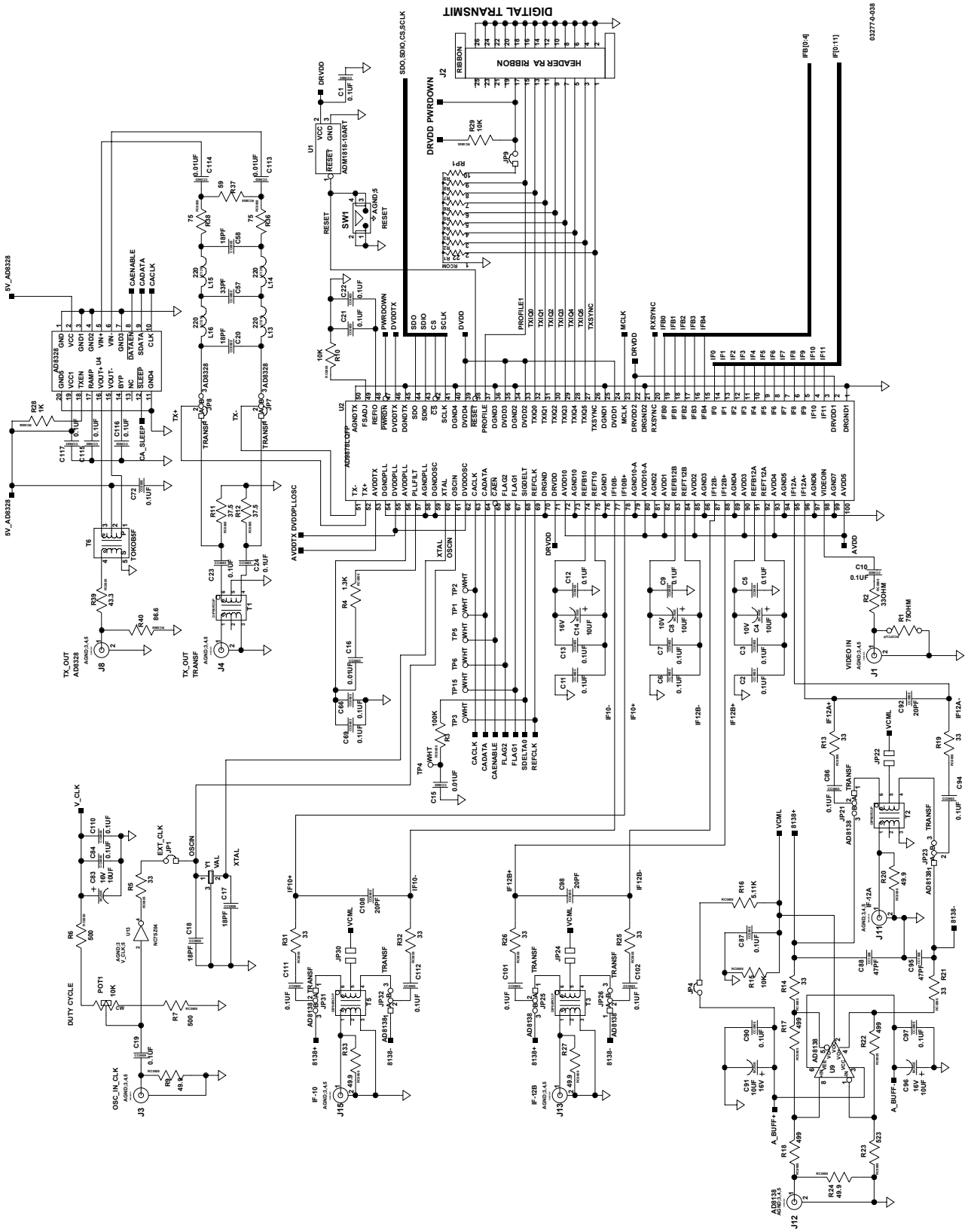

Figure 38. AD9878 Evaluation PCB Schematic (page1)

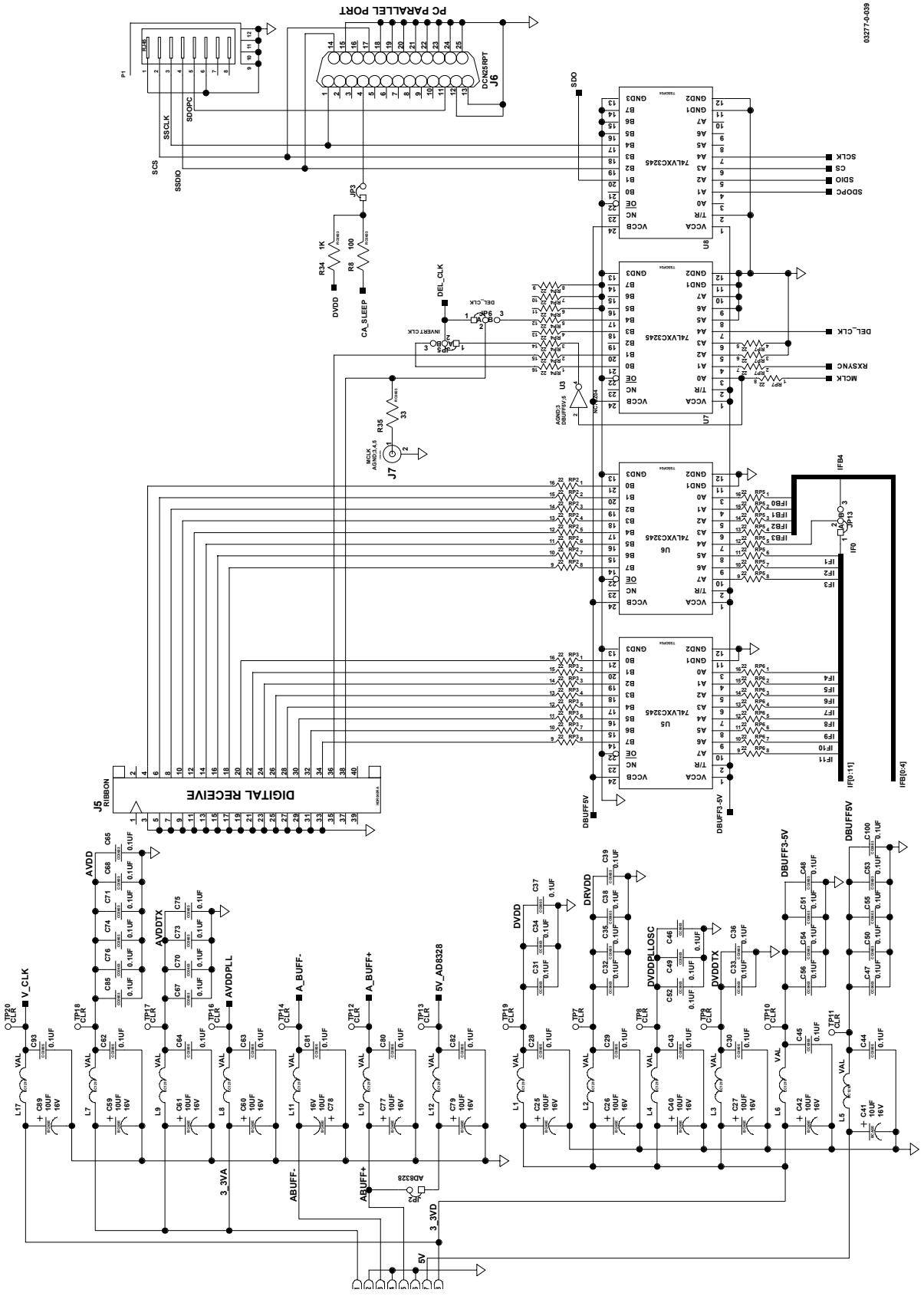

Figure 39. AD9878 Evaluation PCB Schematic (page2)

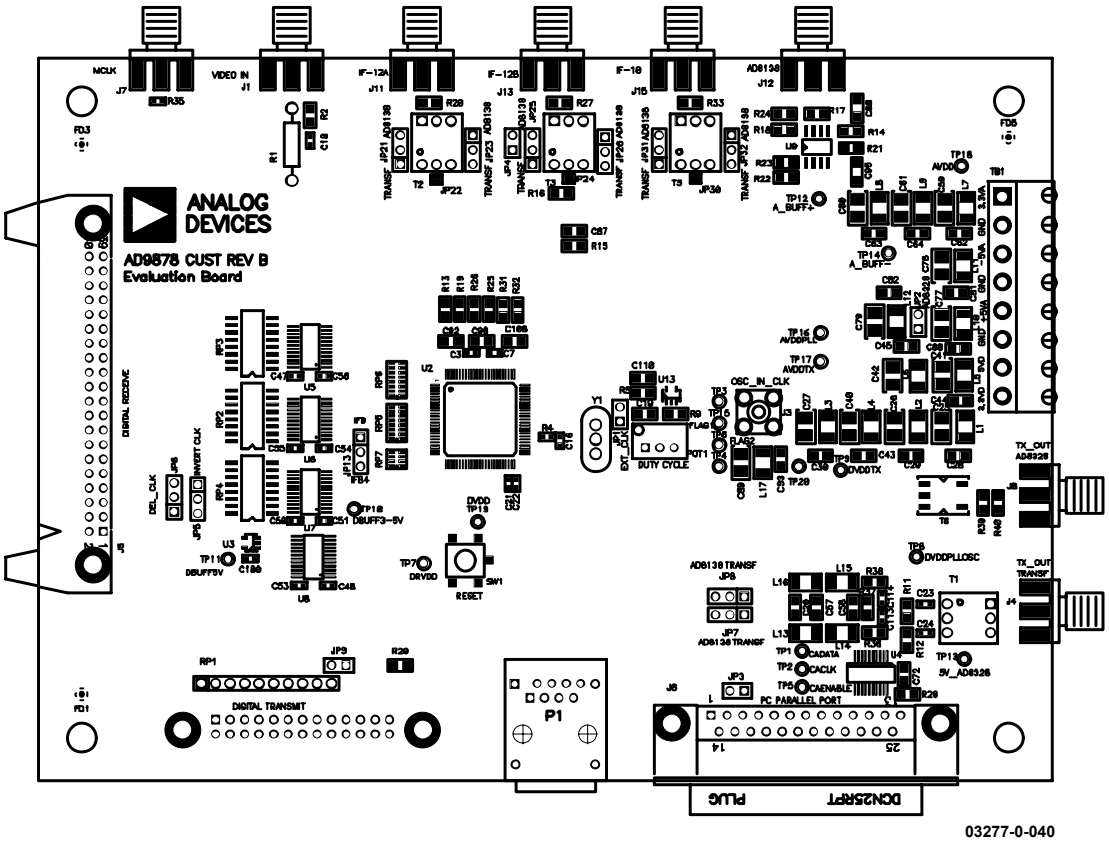

Figure 40. AD9878 Evaluation PCB—Top Assembly

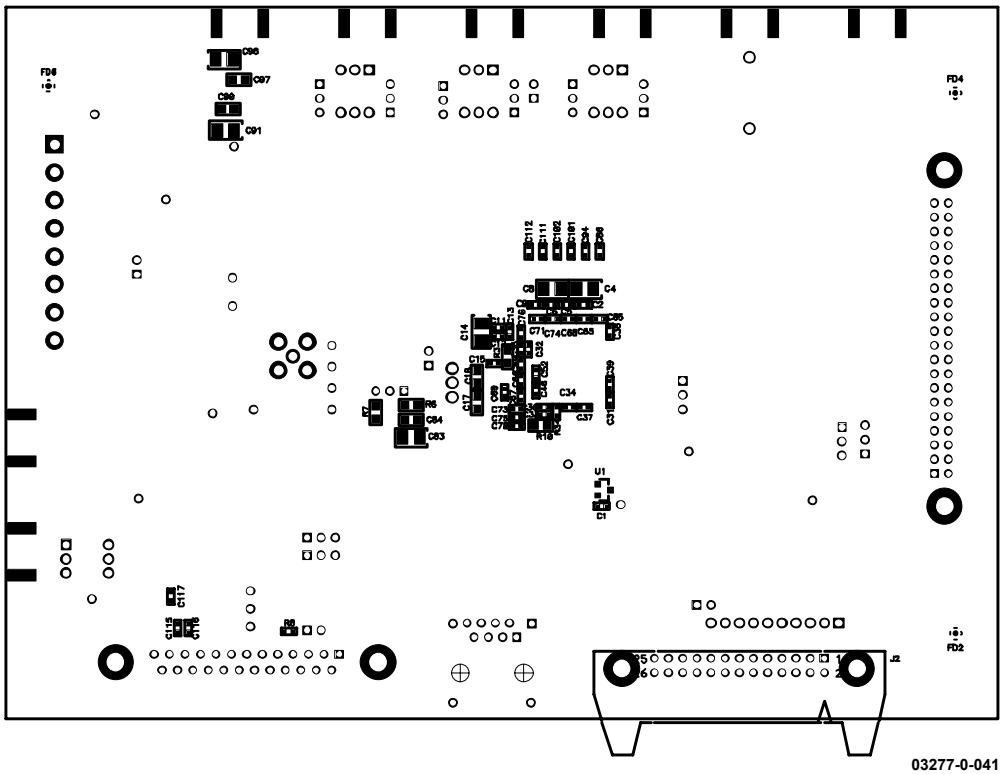

Figure 41. AD9878 Evaluation PCB—Bottom Assembly

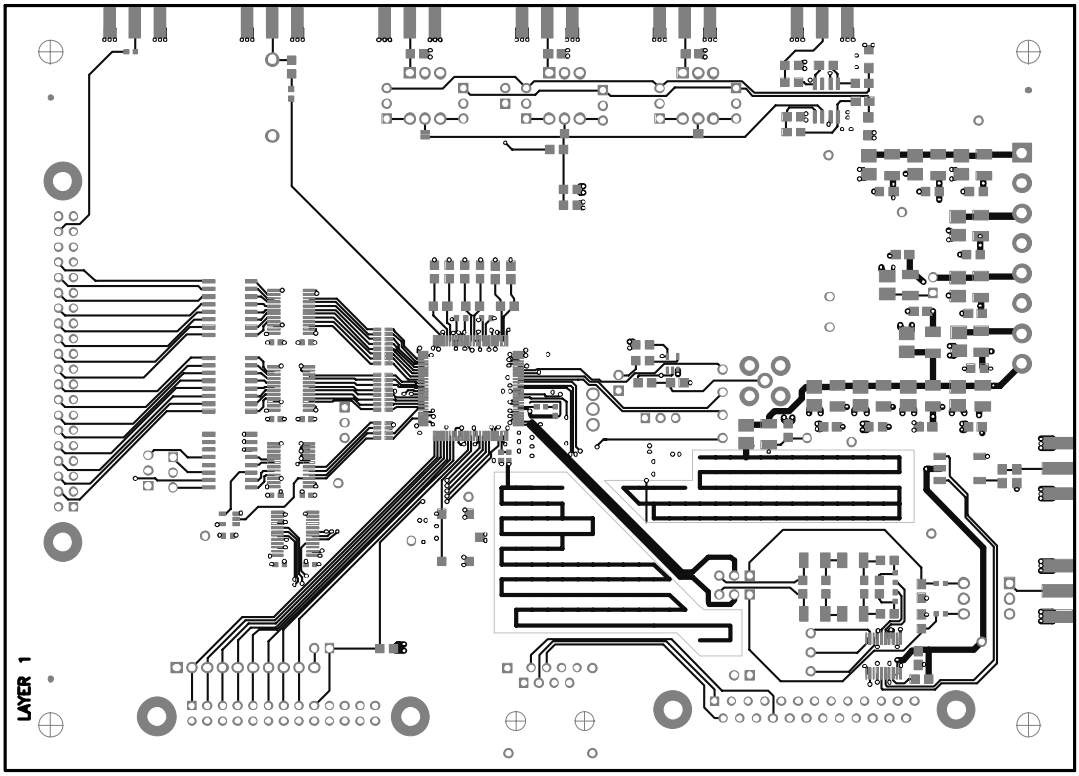

Figure 42. AD9878 Evaluation PCB Layout—Top Layer

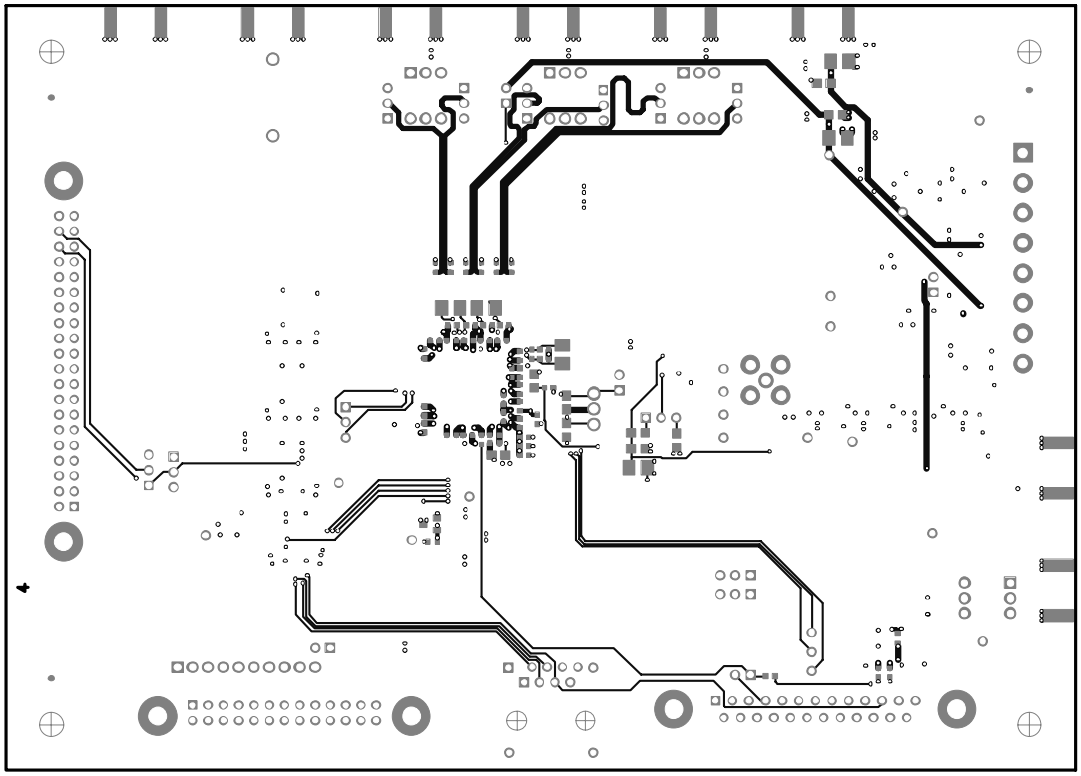

Figure 43. AD9878 Evaluation PCB Layout—Bottom Layer

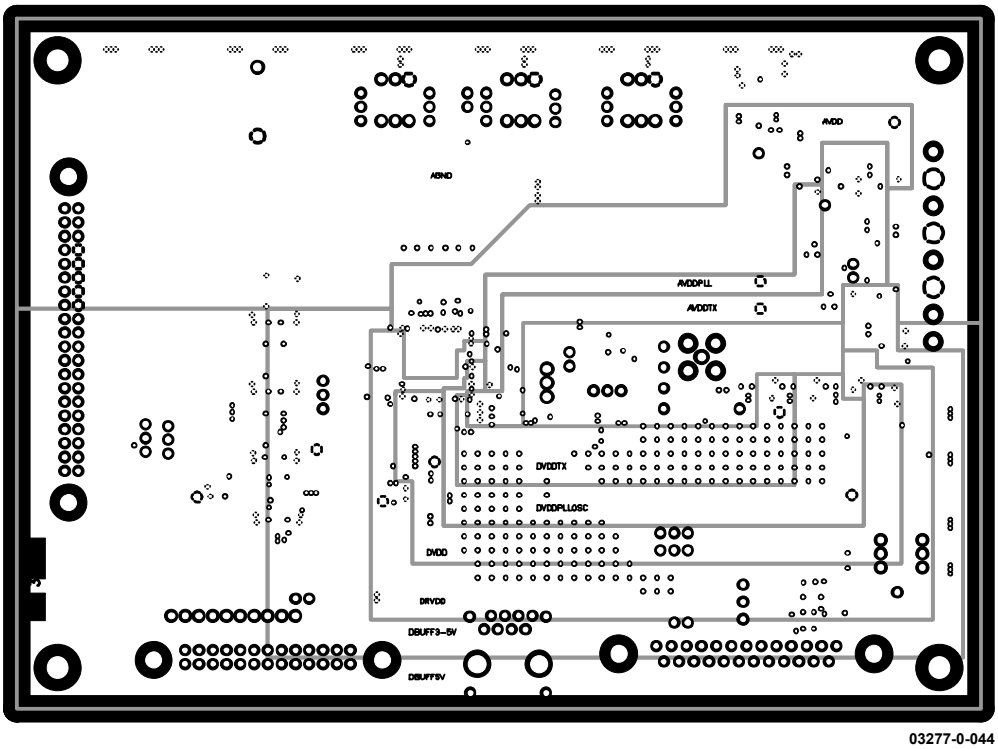

Figure 44. AD9878 Evaluation PCB—Power Plane

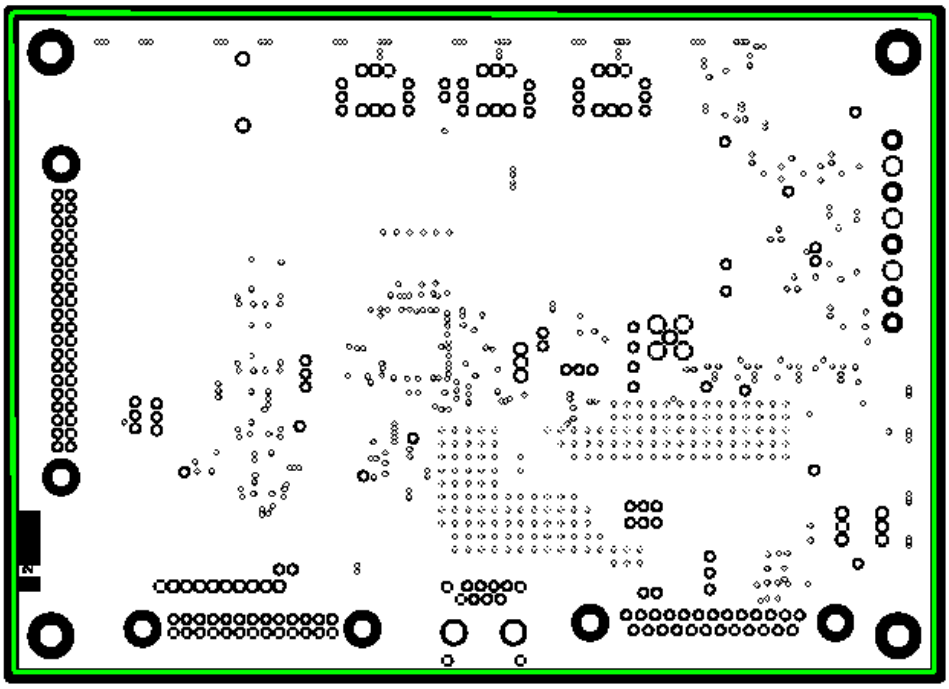

Figure 45. AD9878 Evaluation PCB—Ground Plane

OUTLINE DIMENSIONS

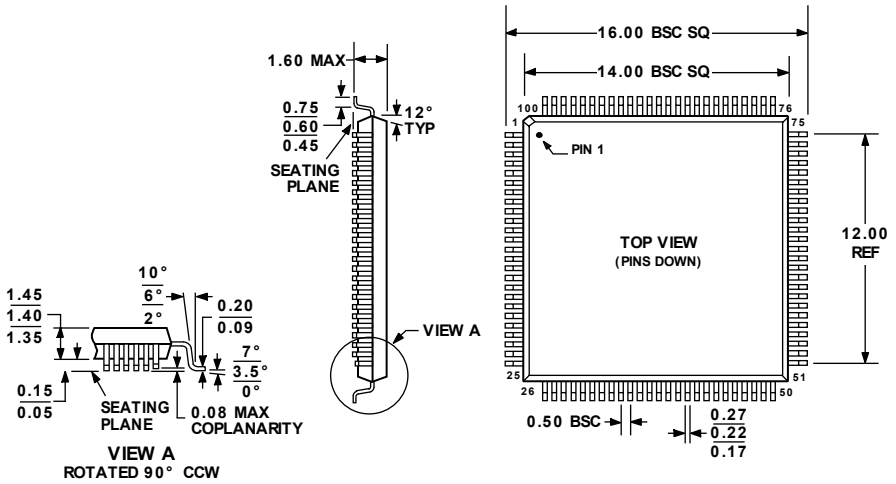

Figure 46. 100-Lead Low Profile Quad FlapPackage [LQFP] (ST-100)
Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9878BST	–40°C to +85°C	100-LQFP	ST-100
AD9878BSTRL	–40°C to +85°C	100-LQFP	ST-100

NOTES

NOTES

C03277-0-5/03(0)