



74VHC595-Q100; 74VHCT595-Q100

8-bit serial-in/serial-out or parallel-out shift register with output latches

Rev. 3 — 28 May 2024

Product data sheet

1. General description

The 74VHC595-Q100; 74VHCT595-Q100 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74VHC595-Q100; 74VHCT595-Q100 are 8-stage serial shift registers with a storage register and 3-state outputs. The shift registers have separate clocks.

Data is shifted on the positive-going transitions of the shift register clock input (SHCP). The data in each register is transferred to the storage register on a positive-going transition of the storage register clock input (STCP). If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7S) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - For 74VHC595-Q100: CMOS level
 - For 74VHCT595-Q100: TTL level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74VHC595D-Q100 74VHCT595D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74VHC595PW-Q100 74VHCT595PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74VHC595BQ-Q100 74VHCT595BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

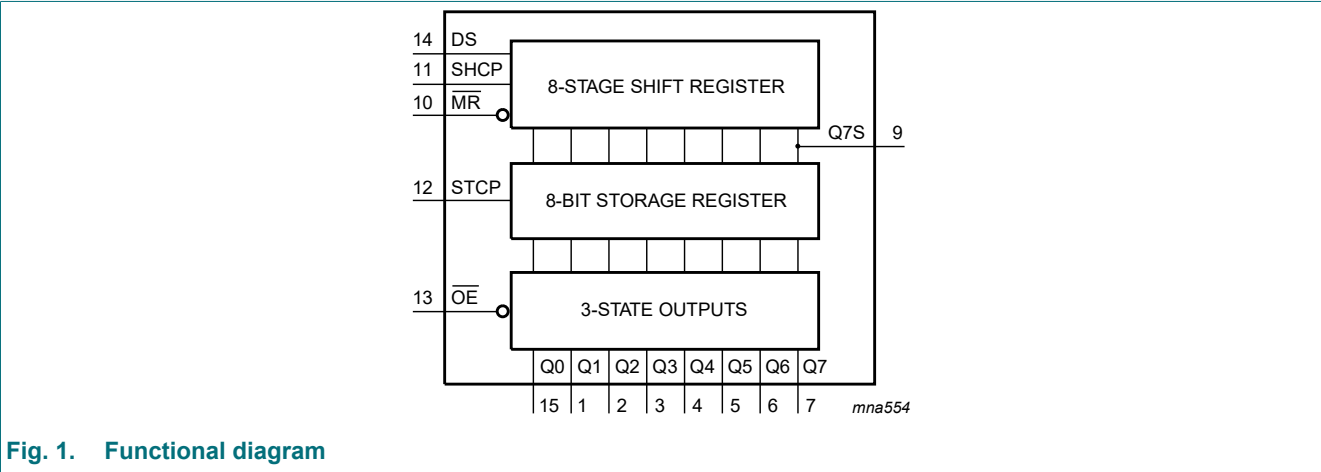


Fig. 1. Functional diagram

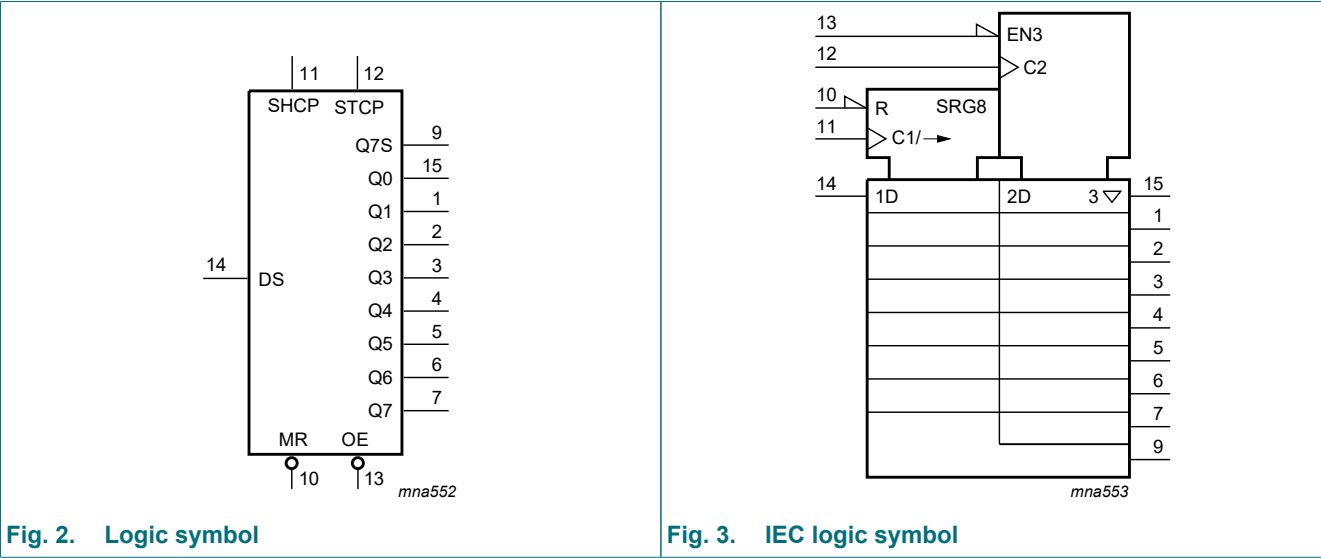


Fig. 2. Logic symbol

Fig. 3. IEC logic symbol

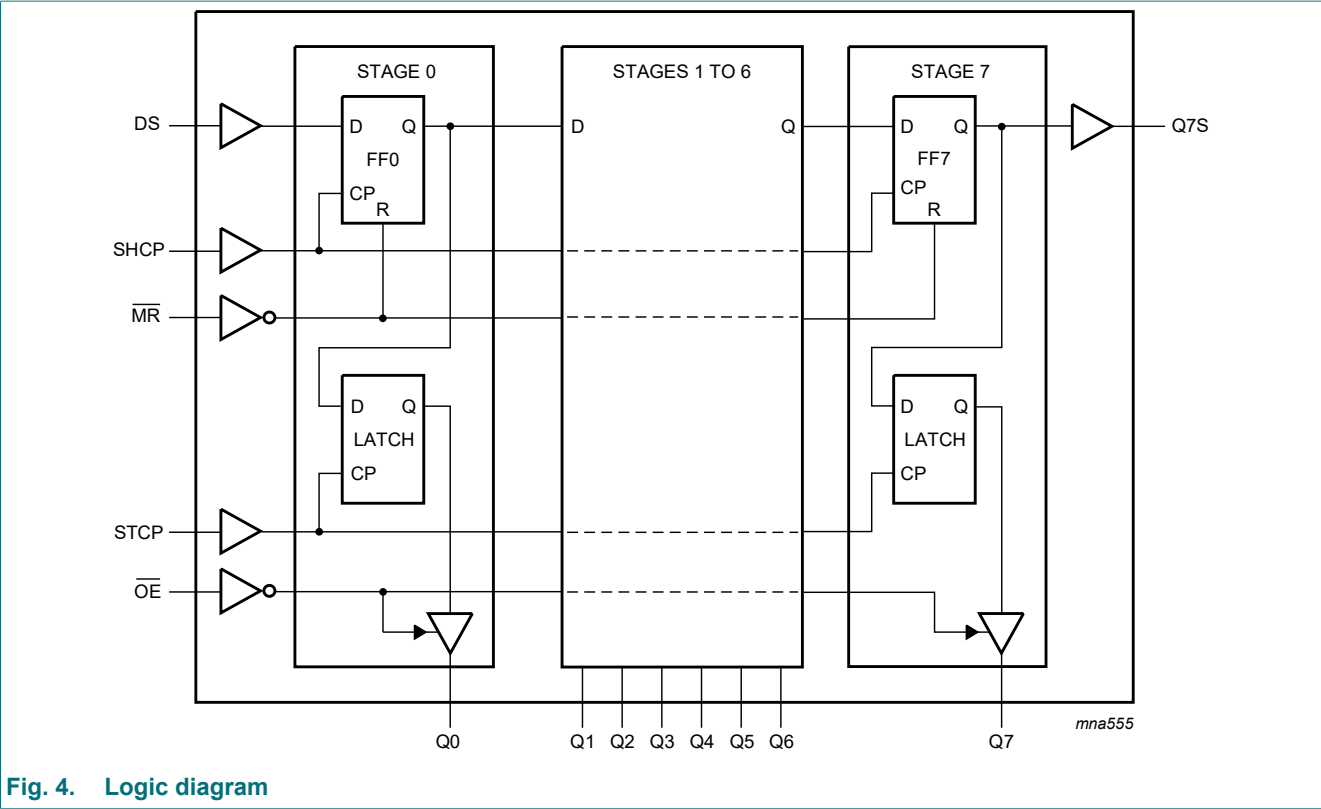
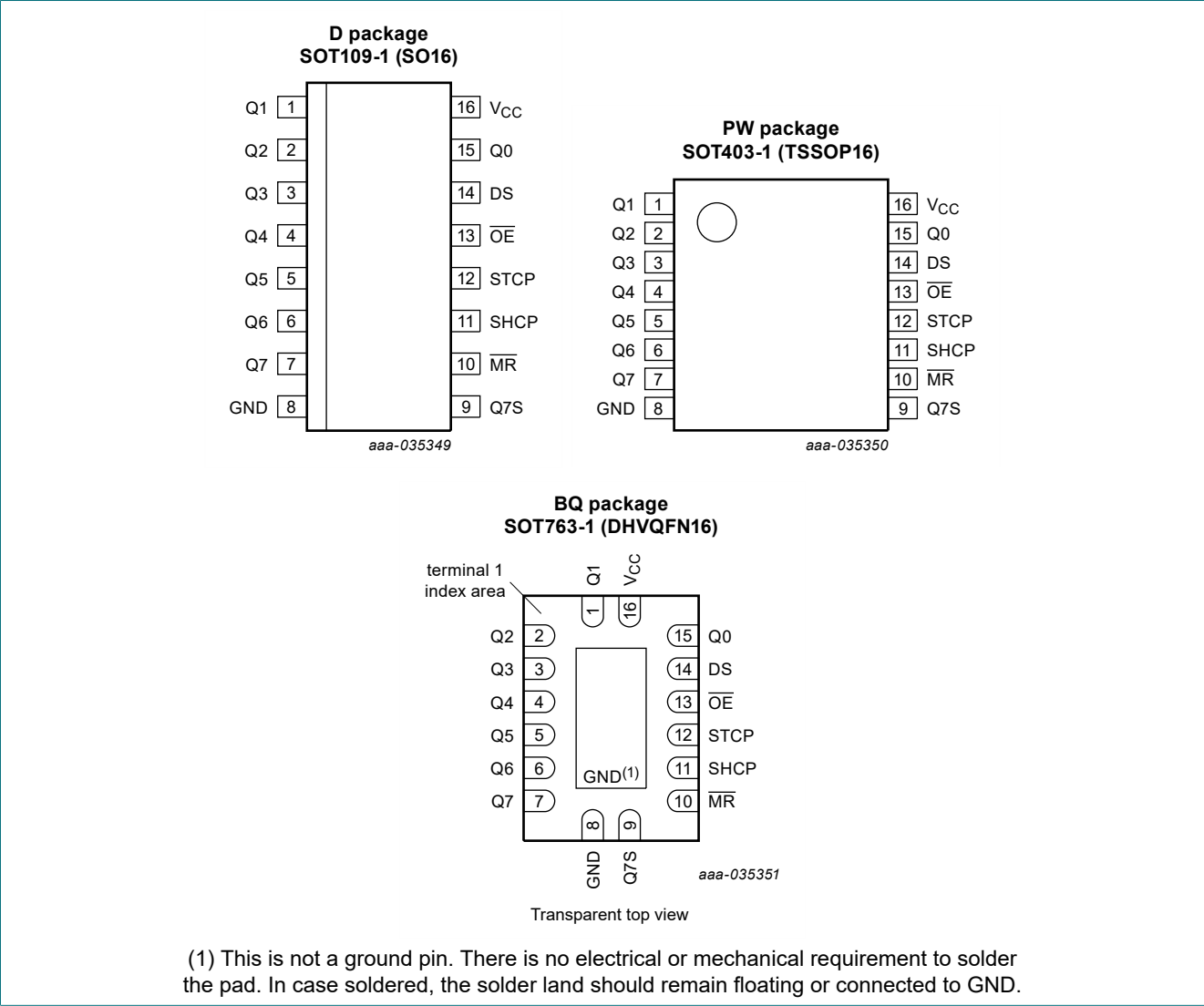


Fig. 4. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
MR	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
OE	13	output enable input (active LOW)
DS	14	serial data input

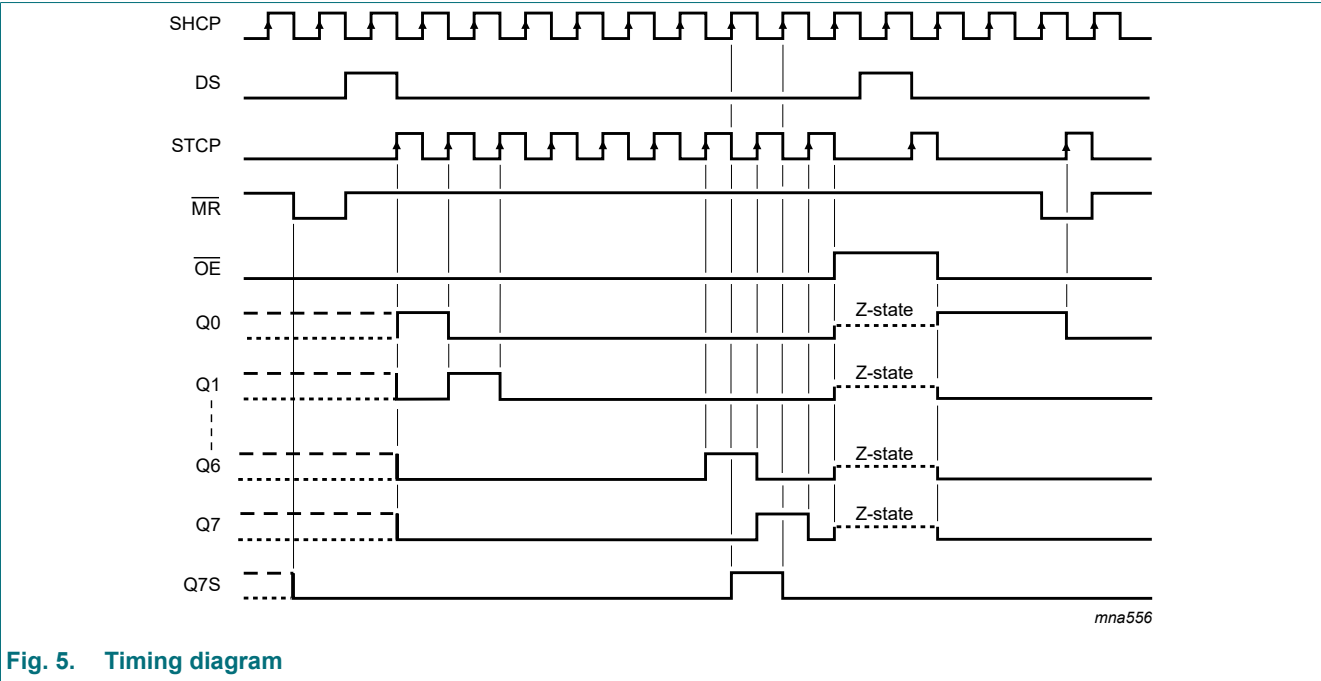
Symbol	Pin	Description
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage state; L = LOW voltage state; ↑ = LOW-to-HIGH transition; X = don't care; NC = no change; Z = high-impedance OFF-state.

Control				Input	Output		Function
SHCP	STCP	OE	MR	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on MR only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages



8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-0.5	+7.0	V

Symbol	Parameter	Conditions	Min	Max	Unit
I _{IK}	input clamping current	V _I < -0.5 V [1]	-20	-	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-20	+20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	74VHC595-Q100			74VHCT595-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.0 V to 3.6 V	-	-	100	-	-	-	ns/V
		V _{CC} = 4.5 V to 5.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74VHC595-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V

8-bit serial-in/serial-out or parallel-out shift register with output latches

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
		$I_O = 50\text{ }\mu\text{A}$; $V_{CC} = 3.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 0\text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	± 0.25	-	± 2.5	-	± 10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 5.5\text{ V}$	-	-	4.0	-	40	-	80	μA
C_I	input capacitance		-	3	10	-	10	-	10	pF
74VHCT595-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5\text{ V}$ to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5\text{ V}$ to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5\text{ V}$								
		$I_O = -50\text{ }\mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8.0\text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5\text{ V}$								
		$I_O = 50\text{ }\mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0\text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	$V_I = 5.5\text{ V}$ or GND; $V_{CC} = 0\text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	± 0.25	-	± 2.5	-	± 10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 5.5\text{ V}$	-	-	4.0	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V}$; other inputs at V_{CC} or GND; $I_O = 0\text{ A}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	3	10	-	10	-	10	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 11.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74VHC595-Q100										
t _{pd}	propagation delay	SHCP to Q7S; see Fig. 6 [2]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.7	13.0	1.0	15.0	1.0	16.5	ns
		C _L = 50 pF	-	7.7	16.5	1.0	18.5	1.0	20.1	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.0	8.2	1.0	9.4	1.0	10.5	ns
		C _L = 50 pF	-	5.4	10.0	1.0	11.4	1.0	12.5	ns
		STCP to Qn; see Fig. 7 [2]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.9	11.9	1.0	13.5	1.0	15.0	ns
		C _L = 50 pF	-	7.7	15.4	1.0	17.0	1.0	18.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.2	7.4	1.0	8.5	1.0	9.5	ns
		C _L = 50 pF	-	5.5	9.0	1.0	10.5	1.0	11.5	ns
		MR to Q7S; see Fig. 9 [3]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.9	12.8	1.0	13.7	1.0	15.0	ns
		C _L = 50 pF	-	7.4	16.3	1.0	17.2	1.0	18.7	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.4	8.0	1.0	9.1	1.0	10.0	ns
		C _L = 50 pF	-	5.6	10.0	1.0	11.1	1.0	12.0	ns
t _{en}	enable time	OE to Qn; see Fig. 10 [4]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.6	11.5	1.0	13.5	1.0	15.0	ns
		C _L = 50 pF	-	7.4	15.0	1.0	17.0	1.0	18.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.0	8.6	1.0	10.0	1.0	11.0	ns
C _L = 50 pF	-	5.3	10.6	1.0	12.0	1.0	13.0	ns		
t _{dis}	disable time	OE to Qn; see Fig. 10 [5]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.4	11.0	1.0	13.0	1.0	14.5	ns
		C _L = 50 pF	-	8.7	15.7	1.0	16.2	1.0	17.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.8	8.0	1.0	9.5	1.0	10.5	ns
C _L = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns		

8-bit serial-in/serial-out or parallel-out shift register with output latches

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
f _{max}	maximum frequency	SHCP or STCP; see Fig. 6 and Fig. 7								
		V _{CC} = 3.0 V to 3.6 V	80	125	-	60	-	40	-	MHz
		V _{CC} = 4.5 V to 5.5 V	130	170	-	110	-	90	-	MHz
t _W	pulse width	SHCP HIGH or LOW; see Fig. 6								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; see Fig. 7								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		MR LOW; see Fig. 9								
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
t _{su}	set-up time	DS to SHCP; see Fig. 8								
		V _{CC} = 3.0 V to 3.6 V	3.5	-	-	3.5	-	3.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; see Fig. 7								
		V _{CC} = 3.0 V to 3.6 V	8.5	-	-	8.5	-	8.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t _h	hold time	DS to SHCP; see Fig. 8								
		V _{CC} = 3.0 V to 3.6 V	1.5	-	-	1.5	-	1.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	ns
t _{rec}	recovery time	MR to SHCP; see Fig. 9								
		V _{CC} = 3.0 V to 3.6 V	3.0	-	-	3.0	-	3.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	2.5	-	-	2.5	-	2.5	-	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} ; all 9 outputs switching	[6]	-	180	-	-	-	-	pF

8-bit serial-in/serial-out or parallel-out shift register with output latches

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74VHCT595-Q100; V _{CC} = 4.5 V to 5.5 V										
t _{pd}	propagation delay	SHCP to Q7S; see Fig. 6 [2]								
		C _L = 15 pF	-	3.8	8.2	1.0	9.0	1.0	10.0	ns
		C _L = 50 pF	-	5.2	10.0	1.0	11.0	1.0	12.0	ns
		STCP to Qn; see Fig. 7 [2]								
		C _L = 15 pF	-	4.0	7.4	1.0	8.5	1.0	9.5	ns
		C _L = 50 pF	-	5.3	9.0	1.0	10.5	1.0	11.5	ns
		MR to Q7S; see Fig. 9 [3]								
		C _L = 15 pF	-	4.6	8.2	1.0	9.5	1.0	10.5	ns
	C _L = 50 pF	-	5.8	10.5	1.0	11.5	1.0	12.5	ns	
t _{en}	enable time	OE to Qn; see Fig. 10 [4]								
		C _L = 15 pF	-	4.8	9.0	1.0	11.0	1.0	12.0	ns
		C _L = 50 pF	-	6.2	11.6	1.0	13.0	1.0	14.5	ns
t _{dis}	disable time	OE to Qn; see Fig. 10 [5]								
		C _L = 15 pF	-	3.6	6.9	1.0	8.0	1.0	9.0	ns
		C _L = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns
f _{max}	maximum frequency	SHCP and STCP; see Fig. 6 and Fig. 7	130	170	-	110	-	90	-	MHz
t _W	pulse width	SHCP HIGH or LOW; see Fig. 6	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; see Fig. 7	5.0	-	-	5.0	-	5.0	-	ns
		MR LOW; see Fig. 9	5.0	-	-	5.0	-	5.0	-	ns
t _{su}	set-up time	DS to SHCP; see Fig. 8	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; see Fig. 7	5.0	-	-	5.0	-	5.0	-	ns
t _h	hold time	DS to SHCP; see Fig. 8	2.0	-	-	2.0	-	2.0	-	ns
t _{rec}	recovery time	MR to SHCP; see Fig. 9	3.0	-	-	3.0	-	3.0	-	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} ; all 9 outputs switching [6]	-	190	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{pd} is the same as t_{PZH} only.

[4] t_{en} is the same as t_{PZL} and t_{PZH}.

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

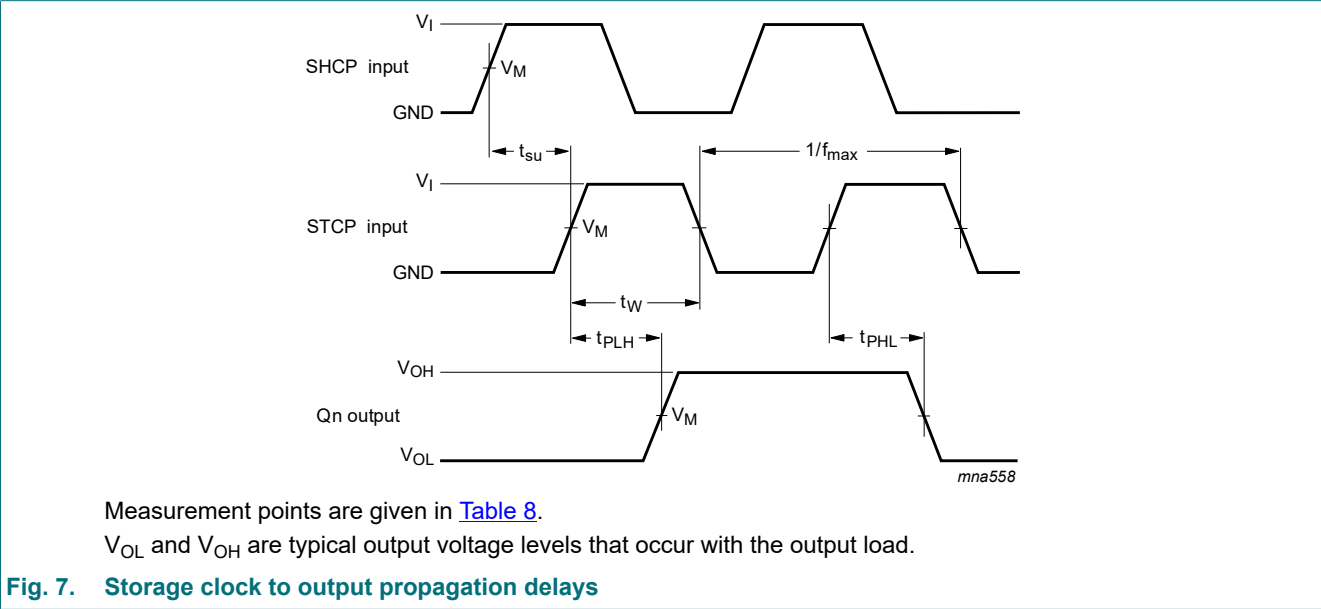
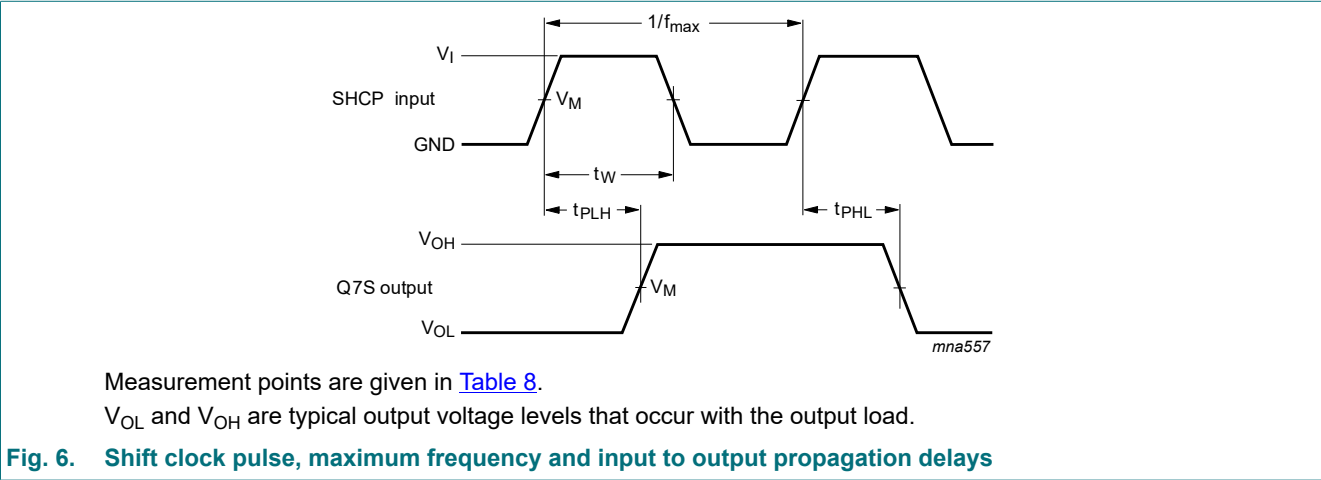
f_o = output frequency in MHz;

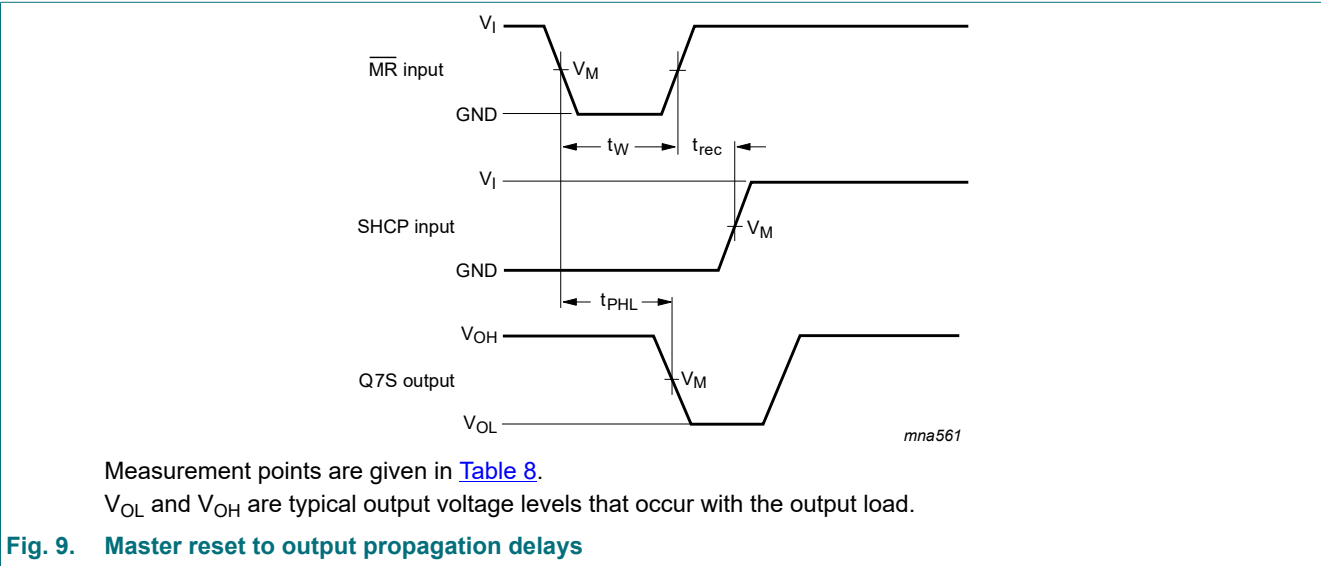
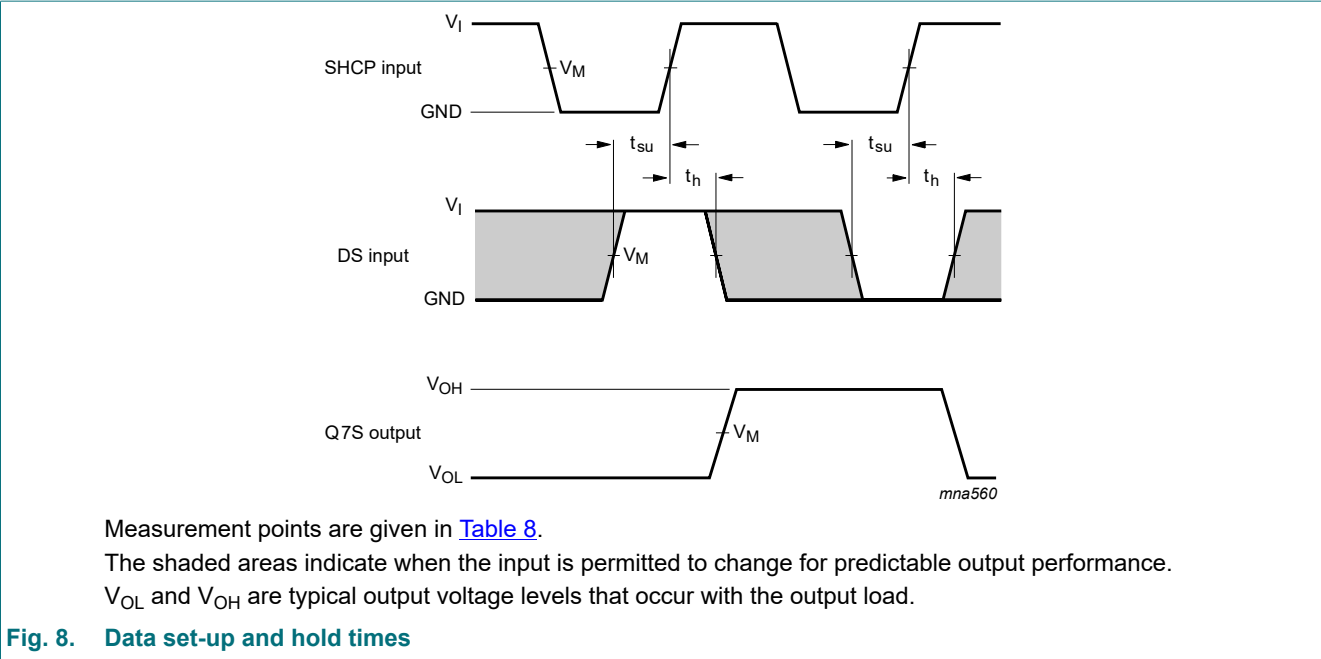
Σ(C_L × V_{CC}² × f_o) = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

11.1. Waveforms and test circuit





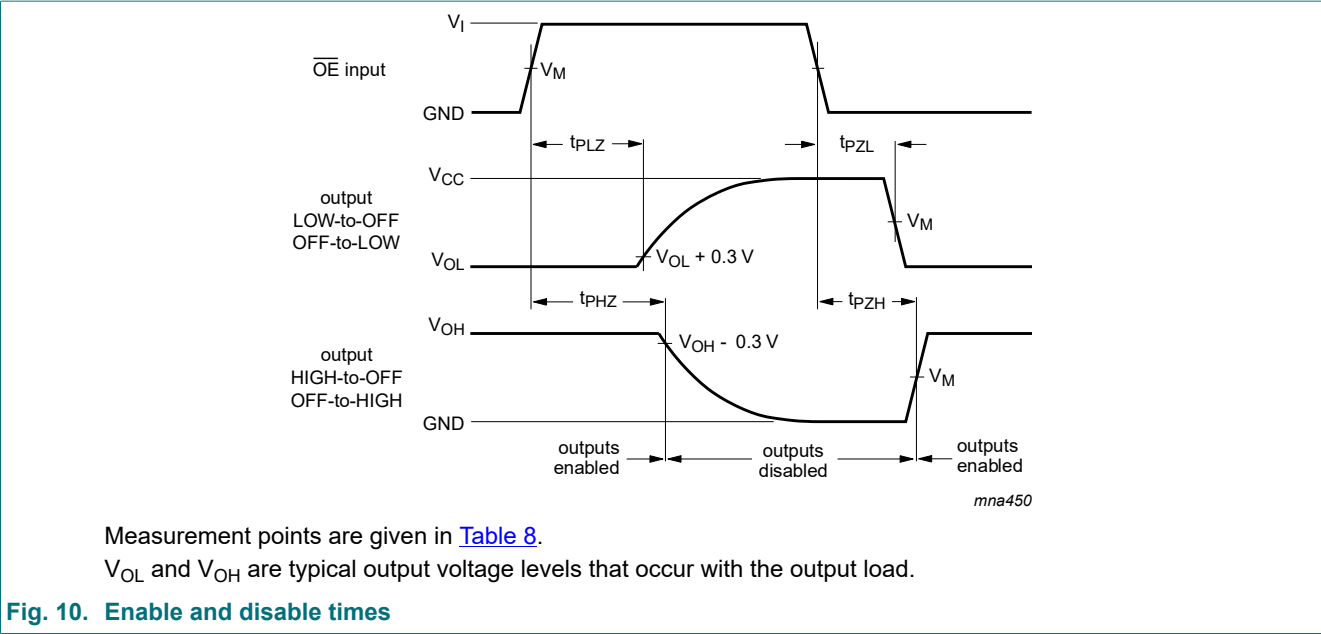


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74VHC595-Q100	$0.5V_{CC}$	$0.5V_{CC}$
74VHCT595-Q100	1.5 V	$0.5V_{CC}$

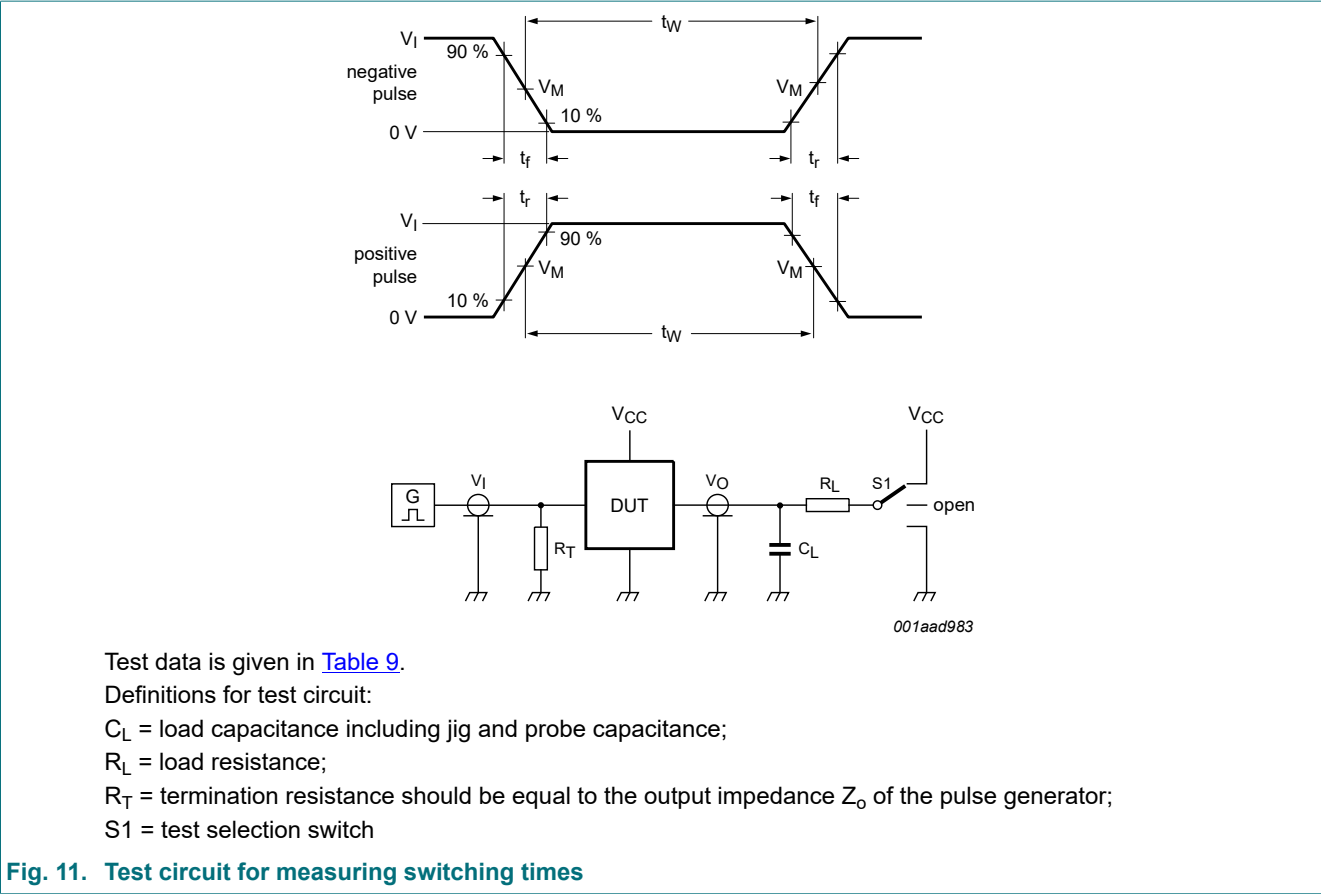


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74VHC595-Q100	V_{CC}	$\leq 3.0\text{ ns}$	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74VHCT595-Q100	3.0 V	$\leq 3.0\text{ ns}$	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

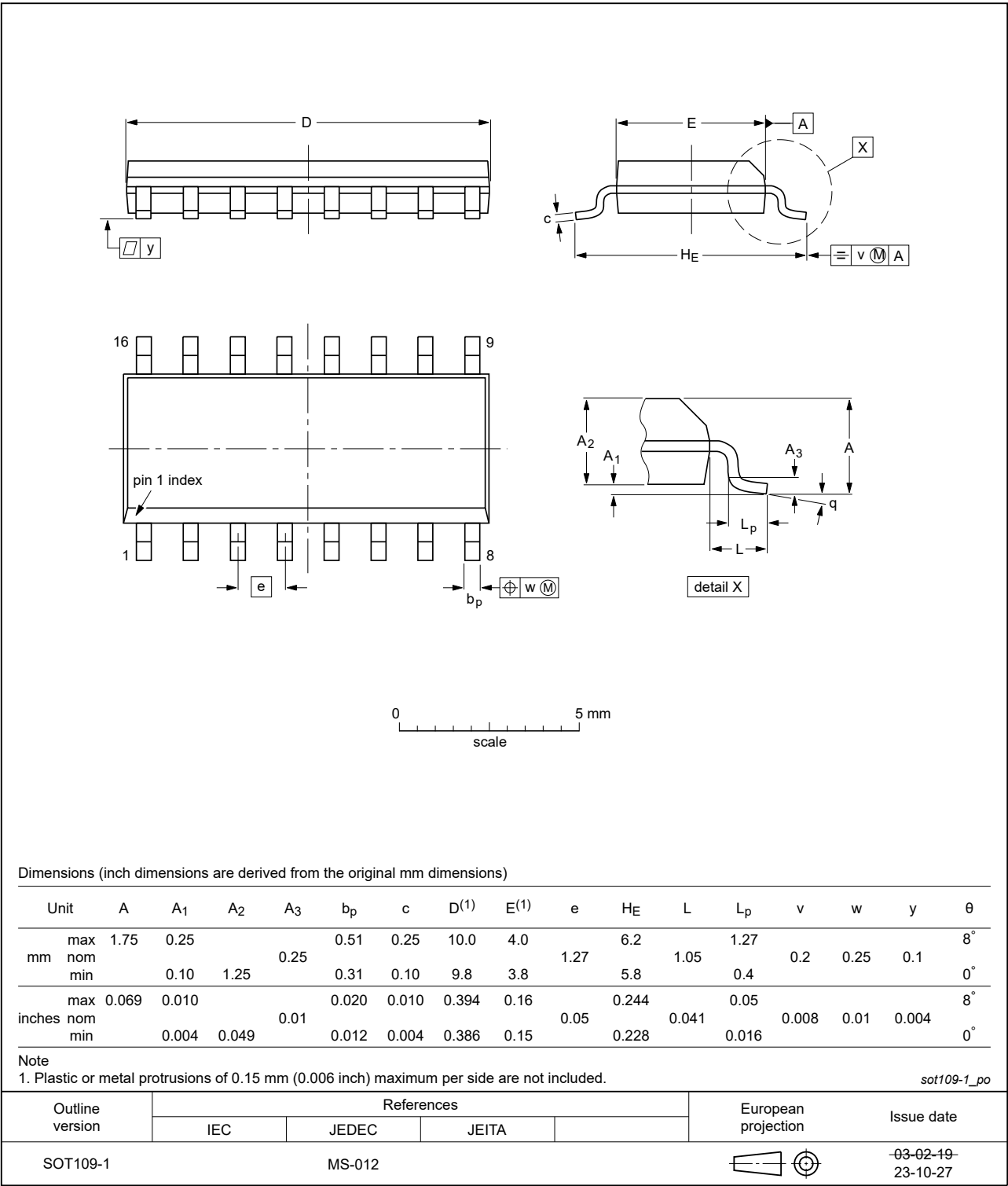


Fig. 12. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

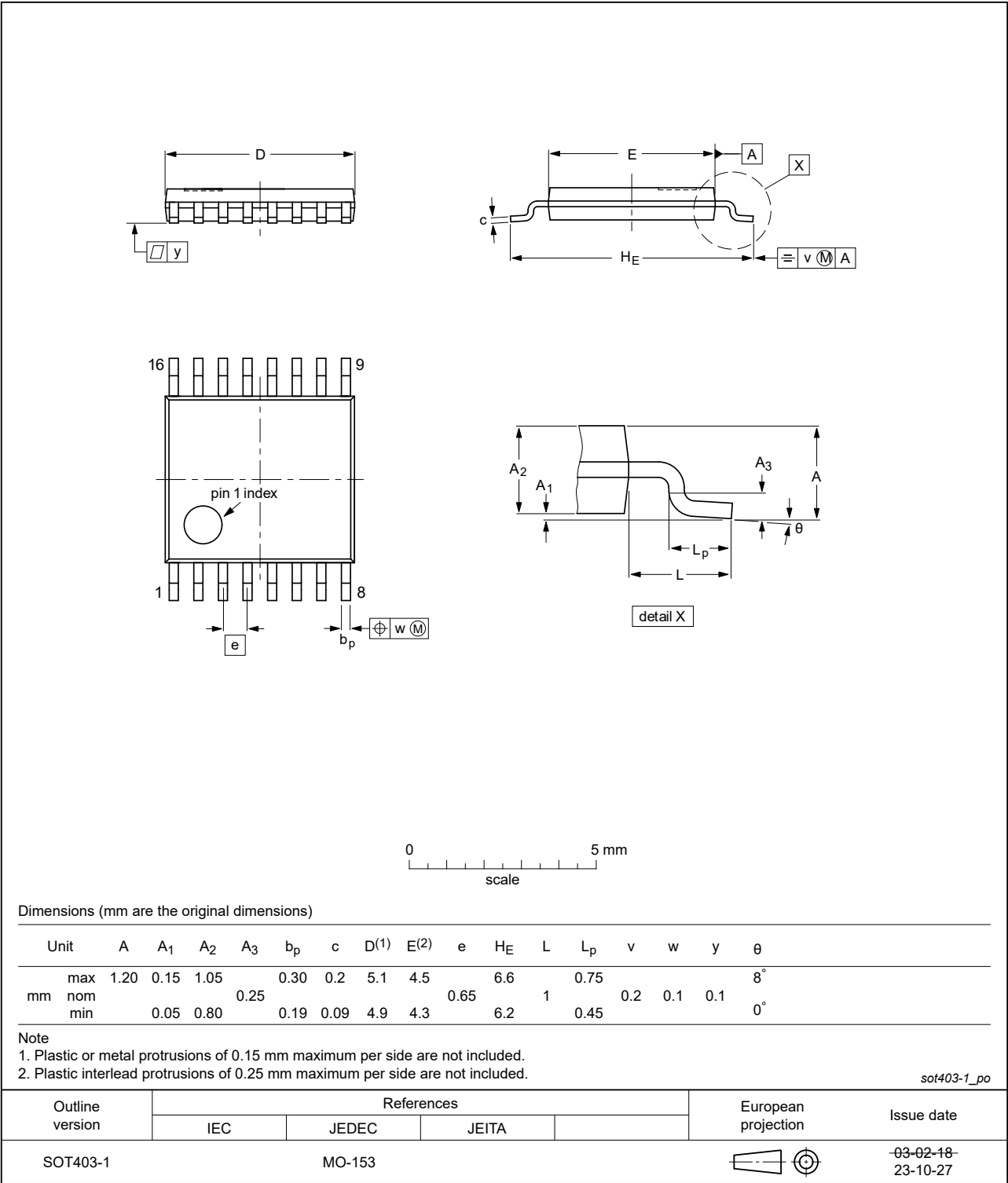


Fig. 13. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1



Fig. 14. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74VHC_VHCT595_Q100 v.3	20240528	Product data sheet	-	74VHC_VHCT595_Q100 v.2
Modifications:	Fig. 12, Fig. 13: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. Section 2: ESD specification updated according to the latest JEDEC standard.			
74VHC_VHCT595_Q100 v.2	20200625	Product data sheet	-	74VHC_VHCT595_Q100 v.1
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. Section 2 updated. Fig. 5: updated (SHCP waveform added). Table 4: Derating values for P_{tot} total power dissipation updated. Table 6: Conditions for I_{OZ} corrected.			
74VHC_VHCT595_Q100 v.1	20131115	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This Nexperia product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or

equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Ordering information.....2

5. Functional diagram.....2

6. Pinning information.....4

6.1. Pinning.....4

6.2. Pin description.....4

7. Functional description..... 5

8. Limiting values..... 5

9. Recommended operating conditions.....6

10. Static characteristics.....6

11. Dynamic characteristics.....8

11.1. Waveforms and test circuit..... 11

12. Package outline..... 15

13. Abbreviations..... 18

14. Revision history..... 18

15. Legal information.....19

© Nexperia B.V. 2024. All rights reserved

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 28 May 2024