TVP5158
Four-Channel NTSC/PAL Video Decoders

With Independent Scalers, Noise Reduction, Auto Contrast, and Flexible Output Formatter for Security and Other Multi-Channel Video Applications

Data Manual

TEXAS INSTRUMENTS

Contents

List of Figures

List of Tables

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Four-Channel NTSC/PAL Video Decoders

Check for Samples: TVP5158 TVP5157 TVP5156

1 Introduction

1.1 Features

- **Common Device Features (TVP5156, TVP5157, TVP5158)**
  - **Four separate video decoder channels having the following features for each channel**
    - **Accepts NTSC (J, M, 4.43) and PAL (B, D, G, H, I, M, N, Nc, 60) video data**
    - **Composite video inputs, Pseudo-differential video inputs to improved noise immunity**
    - **High-speed 10-bit ADC**
    - **Fully differential CMOS analog preprocessing channels with clamping**
    - **Integrated Anti-Aliasing filter**
    - **2D 5-line (5H) adaptive comb filter**
    - **Noise reduction and auto contrast**
    - **Robust automatic video standard detection (NTSC/PAL) and switching**
    - **Programmable hue, saturation, sharpness, brightness and contrast**
    - **Luma-peaking processing**
    - **Patented architecture for locking to weak, noisy, or unstable signals**
  - **Four independent scalers support horizontal and/or vertical 2:1 downscaling**
  - **Channel multiplexing capabilities with metadata insertion**
    - **Pixel-interleaved mode supports up to four-channel D1 multiplexed 8-bit output at 108 MHz**
    - **Supports concurrent NTSC and PAL inputs**
  - **Support crystal interface with on-chip oscillator and single clock input mode**
  - **Single 27-MHz clock input or crystal for all standards and all channels**
  - **Internal phase-locked loop (PLL) for line-locked clock (separate for each channel) and sampling**
  - **Standard programmable video output format**
    - **ITU-R BT.656, 8-bit 4:2:2 with embedded syncs**
    - **YCbCr 16-bit 4:2:2 with embedded syncs**
  - **Macrovision™ copy protection detection**
  - **3.3-V compatible I/O**
  - **128-pin TQFP package**
  - **Available in commercial (0°C to 70°C) temperature range**
- **Additional TVP5158/TVP5157 Specific Features**
  - **Integrated four-channel audio ADC with audio sample rate of 8 kHz or 16 kHz**
  - **Support Master and Slave mode I²S Output**
  - **Support audio cascade connection**
- **Additional TVP5158 Specific Features**
  - **Enhanced channel multiplexing capability – Line-interleaved mode**
  - **Four-channel D1 multiplexed output at 8 bit at 108 MHz**
  - **Video cascade connection for 8-Ch CIF, 8-Ch Half-D1, and 8-Ch CIF + 1-Ch D1 outputs**
  - **Also available in Industrial (-40°C to 85°C) temperature range**

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1.2   Applications

- Security/surveillance digital video recorders/servers and PCI products
- Automotive infotainment video hub
- Large format video wall displays
- Game systems

1.3   Related Products

- TVP5154A
- TVP5150AM1
- TVP5146M2
- TVP5147M1

1.4   Description

The TVP5158, TVP5157, and TVP5156 devices are 4-channel, high-quality NTSC/PAL video decoder that digitizes and decodes all popular base-band analog video formats into digital video output. Each channel of this decoder includes 10-bit 27-MSPS A/D converter (ADC). Preceding each ADC in the device, the corresponding analog channel contains an analog circuit that clamps the input to a reference voltage and applies the gain.

Composite input signal is sampled at 2x the ITU-R BT.601 clock frequency, line-locked alignment, and is then decimated to the 1x pixel rate. CVBS decoding uses five-line adaptive comb filtering for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts. A chroma trap filter is also available. On CVBS inputs, the user can control video characteristics such as contrast, brightness, saturation, and hue via an I^2C host port interface. Furthermore, luma peaking (sharpness) with programmable gain is included.

All 4 channels are independently controllable. These decoders share a single clock input for all channels and for all supported standards.

TVP5158 provides a glueless audio and video interface to TI DaVinci™ video processors. Video output ports support 8-bit ITU-R BT.656 and 16-bit 4:2:2 YCbCr with embedded synchronization. TVP5158 supports multiplexed pixel-interleaved and line-interleaved mode video outputs with metadata insertion. TVP5158 and TVP5157 integrate 4-Ch audio ADCs to reduce the BOM cost for surveillance market. Multiple TVP5158 devices can be cascade connected to support up to 8-Ch Video or 16-Ch audio processing.

Noise reduction and auto contrast functions improve the video quality under low light condition which is very critical for surveillance products.

The TVP5158, TVP5157, and TVP5156 can be programmed by using a single I^2C serial interface. I^2C commands can be sent to one or more decoder cores simultaneously, reducing the amount of I^2C activity necessary to configure each core. This is especially useful for fast downloading modified firmware to the decoder cores.

TVP5158, TVP5157, and TVP5156 use 1.1-V, 1.8-V, and 3.3-V power supplies for the analog/digital core and I/O. These devices are available in a 128-pin TQFP package.

Table 1-1. Device Options

Device Name	4-Ch Audio ADC	Line-Interleaved Modes
TVP5156	No	No
TVP5157	Yes	No
TVP5158	Yes	Yes

1.5 ORDERING INFORMATION

T$_A$	PACKAGED DEVICES TQFP 128-Pin PowerPAD™ Package
0°C to 70°C	TVP5156PNP
	TVP5157PNP
	TVP5158PNP
-40°C to 85°C	TVP5158IPNP

2 Terminal Assignments

2.1 Functional Block Diagram
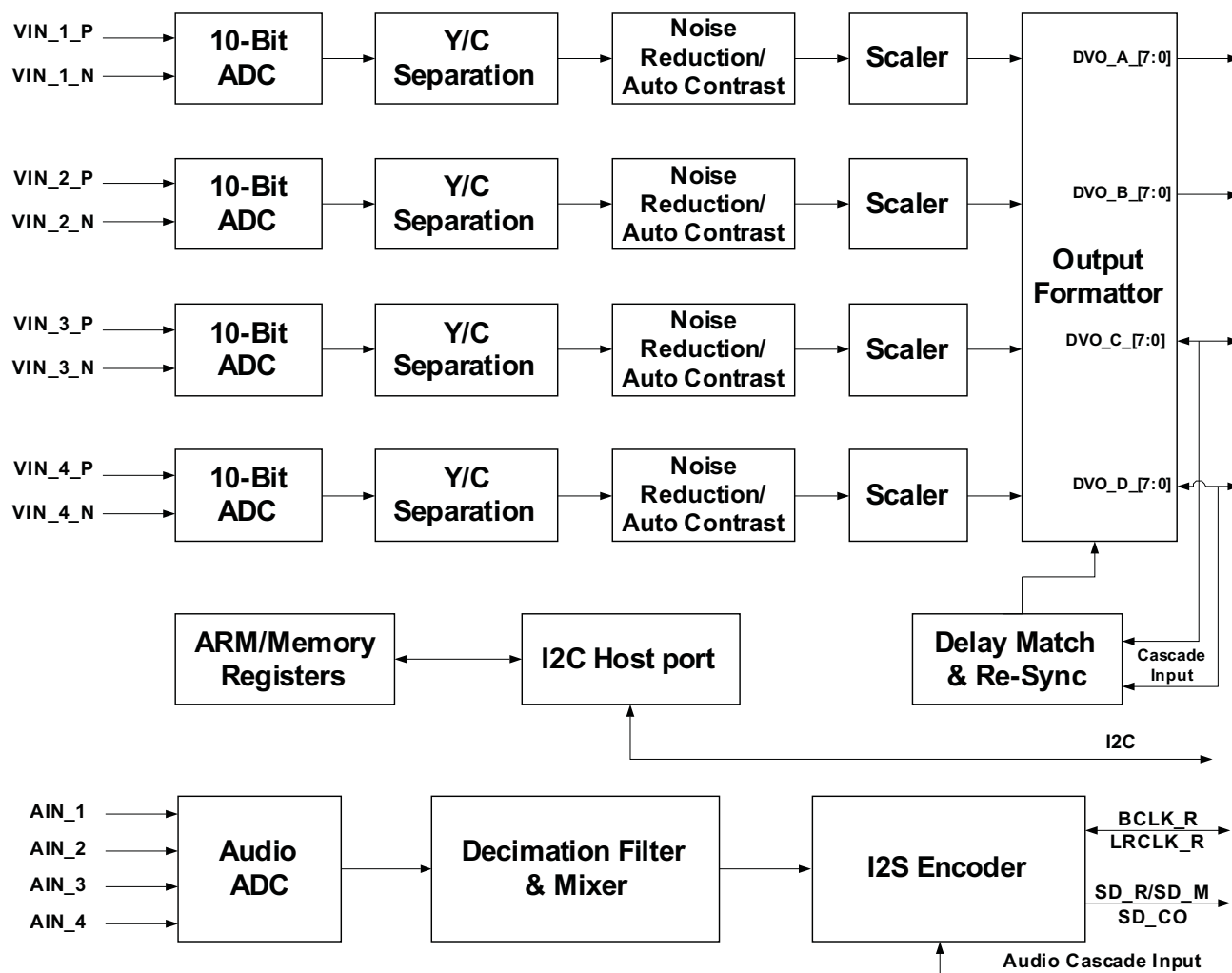
Figure 2-1. Functional Block Diagram

TVP5158
128-Pin TQFP Package

Top pins (left to right, 96 to 65):
VSSA (96), AIN_1 (95), AIN_2 (94), AIN_3 (93), AIN_4 (92), VDDA_1_8 (91), VSS (90), SD_M (89), SD_R (88), VSS (87), LRCLK_R (86), BCLK_R (85), VDD_1_1 (84), SD_CO (83), VSS (82), VDD_3_3 (81), I2CA0 (80), VSS (79), DVO_A_0 (78), DVO_A_1 (77), VDD_1_1 (76), DVO_A_2 (75), DVO_A_3 (74), VSS (73), DVO_A_4 (72), DVO_A_5 (71), VDD_3_3 (70), DVO_A_6 (69), DVO_A_7 (68), VDD_1_1 (67), I2CA1 (66), VSS (65)

Left pins (97 to 128):
- OSC_OUT — 97
- VSSA — 98
- XTAL_IN — 99
- XTAL_REF — 100
- XTAL_OUT — 101
- VDDA_1_8 — 102
- VDDA_1_1 — 103
- VSSA — 104
- VSSA — 105
- VDDA_1_1 — 106
- VDDA_1_8 — 107
- VIN_1_P — 108
- VIN_1_N — 109
- VSSA — 110
- VSSA — 111
- VIN_2_P — 112
- VIN_2_N — 113
- VDDA_1_8 — 114
- VDDA_1_8 — 115
- REXT_2K — 116
- VSSA — 117
- VSSA — 118
- VDDA_1_1 — 119
- VDDA_1_8 — 120
- VIN_3_P — 121
- VIN_3_N — 122
- VSSA — 123
- VSSA — 124
- VIN_4_P — 125
- VIN_4_N — 126
- VDDA_1_8 — 127
- VDAA_3_3 — 128

Right pins (64 to 33):
- 64 — VDD_1_1
- 63 — DVO_B_0
- 62 — DVO_B_1
- 61 — VSS
- 60 — DVO_B_2
- 59 — DVO_B_3
- 58 — VDD_3_3
- 57 — DVO_B_4
- 56 — DVO_B_5
- 55 — VSS
- 54 — DVO_B_6
- 53 — DVO_B_7
- 52 — VDD_1_1
- 51 — OCLK_P
- 50 — OCLK_N/CLKIN
- 49 — VSS
- 48 — I2CA2
- 47 — VSS
- 46 — DVO_C_0
- 45 — DVO_C_1
- 44 — VDD_1_1
- 43 — DVO_C_2
- 42 — DVO_C_3
- 41 — VDD_3_3
- 40 — DVO_C_4
- 39 — DVO_C_5
- 38 — VSS
- 37 — DVO_C_6
- 36 — DVO_C_7
- 35 — VDD_1_1
- 34 — NC
- 33 — VSS

Bottom pins (left to right, 1 to 32):
VSS (1), INTREQ (2), RESETB (3), SCL (4), SDA (5), VSS (6), T1 (7), T2 (8), T3 (9), T4 (10), T5 (11), VSS (12), VDD_1_1 (13), VSS (14), VDD_3_3 (15), LRCLK_CI (16), BCLK_CI (17), VDD_1_1 (18), SD_CI (19), VSS (20), DVO_D_7 (21), DVO_D_6 (22), VDD_1_1 (23), DVO_D_5 (24), DVO_D_4 (25), VSS (26), DVO_D_3 (27), DVO_D_2 (28), VDD_3_3 (29), DVO_D_1 (30), DVO_D_0 (31), VDD_1_1 (32)

Table 2-1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Analog Section			
VIN_1_P	108	I	Analog video input for ADC channel 1.
VIN_1_N	109	I	Common-mode reference input for ADC channel 1.
VIN_2_P	112	I	Analog video input for ADC channel 2.
VIN_2_N	113	I	Common-mode reference input for ADC channel 2.
VIN_3_P	121	I	Analog video input for ADC channel 3.
VIN_3_N	122	I	Common-mode reference input for ADC channel 3.
VIN_4_P	125	I	Analog video input for ADC channel 4.
VIN_4_N	126	I	Common-mode reference input for ADC channels.
REXT_2K	116	I	External resistor for AFE bias generator. Connect external 1.8kΩ resistor to ground.
AIN_1	95	I	Analog audio input for channel 1 (No Connect for TVP5156 Only)
AIN_2	94	I	Analog audio input for channel 2 (No Connect for TVP5156 Only)
AIN_3	93	I	Analog audio input for channel 3 (No Connect for TVP5156 Only)
AIN_4	92	I	Analog audio input for channel 4 (No Connect for TVP5156 Only)
XTAL_IN	99	I	External clock reference input. It may be connected to external oscillator with 1.8-V compatible clock signal or 27.0-MHz crystal oscillator.
XTAL_REF	100	G	Crystal reference. Connected to analog ground internally.
XTAL_OUT	101	O	External clock reference output. Not connected if XTAL_IN is driven by an external single-ended oscillator.
Analog Power			
VDDA_1_1	103, 106, 119	P	1.1V analog supply
VDDA_1_8	91, 102, 107, 114, 115, 120, 127	P	1.8V analog supply
VDDA_3_3	128	P	3.3V analog supply for all 4 video channels
VSSA	96, 98, 104, 105, 110, 111, 117, 118, 123, 124	G	Analog ground
Digital Power			
VSS	1, 6, 12, 14, 20, 26, 33, 38, 47, 49, 55, 61, 65, 73, 79, 82, 87, 90	G	Digital ground
VDD_1_1	13, 18, 23, 32, 35, 44, 52, 64, 67, 76, 84	P	Digital core supply. Connect to 1.1-V digital supply.
VDD_3_3	15, 29, 41, 58, 70, 81	P	Digital I/O supply. Connect to 3.3-V digital supply.
Digital Section			
INTREQ	2	O	Interrupt request. Interrupt signal to host processor.
RESETB	3	I	Reset. An active low signal that controls the reset state.
SCL	4	I/O	I²C serial clock (open drain)
SDA	5	I/O	I²C serial data (open drain)
OSC_OUT	97	O	Buffered crystal oscillator output. 1.8-V compatible.
OCLK_P	51	O	Output data clock+. All 4 digital video output ports are synchronized to this clock.
OCLK_N/CLKIN	50	I/O	Output data clock- for 2-Ch time-multiplexed mode or data clock input for 8-Ch video cascade mode
DVO_A_[7:0]	68, 69, 71, 72, 74, 75, 77, 78	O	Digital video output data bus.

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Product Folder Link(s): *TVP5158 TVP5157 TVP5156*

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DVO_B_[7:0]	53, 54, 56, 57, 59, 60, 62, 63	O	Digital video output data bus.
DVO_C_[7:0]	36, 37, 39, 40, 42, 43, 45, 46	I/O	Digital video output data bus. In cascade mode, all pins operate as input from another TVP5158 device.
DVO_D_[7:0]	21, 22, 24, 25, 27, 28, 30, 31	I/O	Digital video output data bus. In cascade mode, all pins operate as input from another TVP5158 device.
I2CA0	80	I	I^2C slave address bit 0
I2CA1	66	I	I^2C slave address bit 1
I2CA2	48	I	I^2C slave address bit 2
Digital Audio Section (Not supported on TVP5156)			
BCLK_R	85	I/O	I^2S bit clock for recording. Also known as I^2S serial clock (SCK). Supports master and slave modes.
LRCLK_R	86	I/O	I^2S left/right clock for recording. Also known as I^2S word select (WS). Supports master and slave modes.
SD_R	88	O	I^2S serial data output for recording.
SD_M	89	O	I^2S serial data output for mixed audio or recording.
SD_CO	83	O	Audio serial data output for cascade mode
LRCLK_CI	16	I	I^2S left/right clock input for cascade mode. Also known as I^2S word select (WS).
BCLK_CI	17	I	I^2S bit clock input for cascade mode. Also known as I^2S serial clock (SCK).
SD_CI	19	I	Audio serial data input for cascade mode.
No Connect Pins			
T1, T2, T3, T4, T5, NC	7, 8, 9, 10, 11, 34	NC	For normal operation, no connect

3 Functional Description

3.1 Video Analog Processing and A/D Converters

Each video decoder accepts one composite video input and performs video clamping, anti-aliasing filtering, video amplification, A/D conversion, and gain and offset adjustments to center the digitized video signal. Figure 3-1 shows the video analog processing and ADC block diagram.
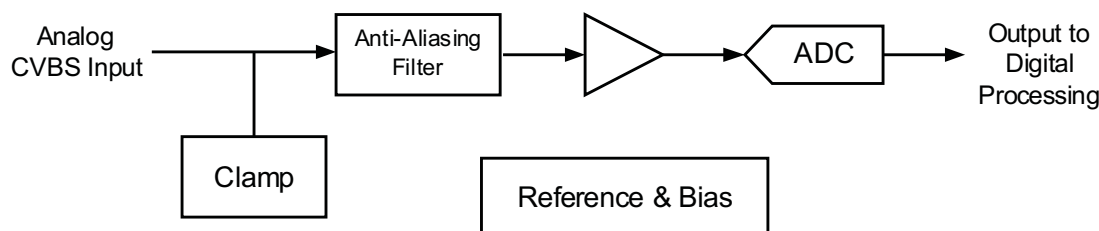
Figure 3-1. Video Analog Processing and ADC Block Diagram

3.1.1 Analog Video Input

Supports NTSC (J, M, 4.43) and PAL (B, D, G, H, I, M, N, Nc, 60) video standards. Each video decoder channel supports a composite video input with a pseudo-differential pin which improves the noise immunity and analog performance.

Each video decoder input should be ac-coupled through a 0.1-µF capacitor. The nominal parallel termination resistor before the input to the device is 75 Ω.

Each video decoder integrates an anti-aliasing filter to provide good stop-band rejection on the analog video input signal. Figure 3-2 shows the frequency response of the anti-aliasing filter.
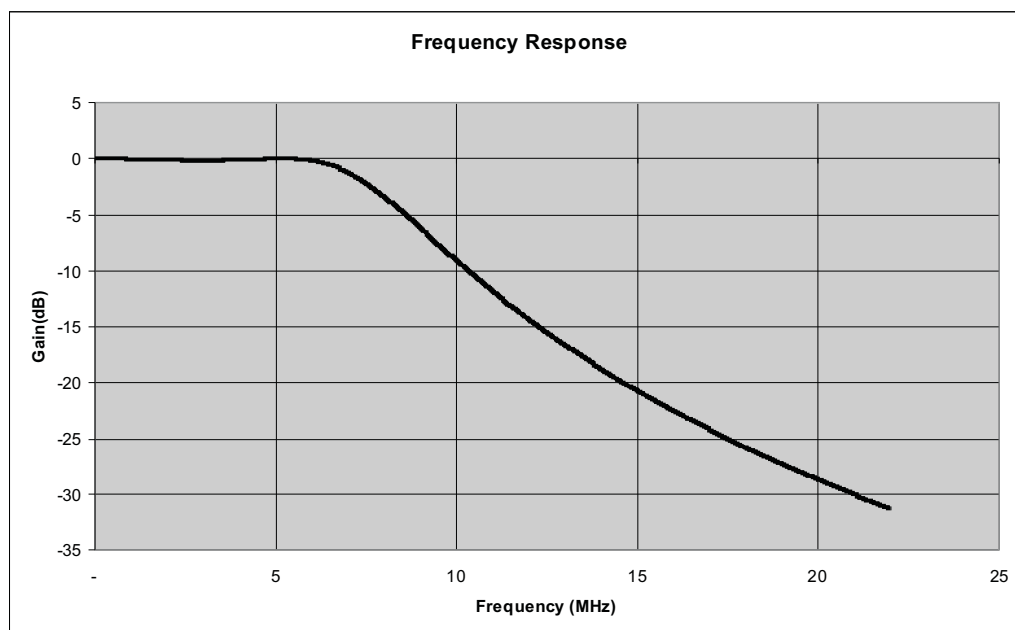
Figure 3-2. Anti-Aliasing Filter Frequency Response

3.1.2 Analog Video Input Clamping

An internal clamping circuit provides dc restoration for all four analog composite video inputs. The dc restoration circuit (sync-tip clamp) restores sync-tip level of the ac-coupled composite video signal to a fixed dc level near the bottom of the A/D converter range.

3.1.3 Analog Audio Input Clamping

An internal clamping circuit provides mid-level clamping of all four analog audio inputs to a dc level of approximately 0.625 V.

3.1.4 A/D Converter

All ADCs have a resolution of 10 bits and can operate at 27 MSPS. Each A/D channel receives a clock from the on-chip phase-locked loop (PLL) at a frequency 27 MHz. All ADC reference voltages are generated internally.

3.2 Digital Video Processing

Digital Video Processing block receives digitized video signals from the ADCs and performs composite processing and YCbCr signal enhancements. The digital data output can be programmed to two formats: ITU-R BT.656 8-bit 4:2:2 with embedded syncs or 16-bit 4:2:2 with embedded syncs. The circuit also detects pseudo-sync pulses, AGC pulses, and color striping in Macrovision-encoded copy-protected material.

3.2.1 2x Decimation Filter

All input signals are over-sampled by a factor of 2 (by 27-MHz clock). The A/D outputs initially pass through decimation filters that reduce the data rate to 1x the pixel rate. The decimation filter is a half-band filter. Over-sampling and decimation filtering can effectively increase the overall signal-to-noise ratio by 3 dB.

3.2.2 Automatic Gain Control

The automatic gain control (AGC) can be enabled and can adjust the signal amplitude controlled by 14-bit digital gain stage after the ADC. The AGC algorithms can use up to four amplitude references: sync height, color burst amplitude, composite peak, and luma peak.

The specific amplitude references being used by the AGC algorithms can be controlled using the AGC white peak processing register located at sub-address 2Dh. The gain increment speed and gain increment delay can be controlled using the AGC increment speed register located at sub-address 29h and the AGC increment delay register located at sub-address 2Ah. The gain decrement speed and gain decrement delay can be controlled using the AGC decrement speed register located at sub-address 2Bh and the AGC decrement delay register located at sub-address 2Ch.

3.2.3 Composite Processor

This Composite Processor circuit receives a digitized composite signal from the ADCs and performs sync and Y/C separation, chroma demodulation for PAL/NTSC, and YUV signal enhancements. The slice levels of the sync separator are adaptive. The slice levels continually adapt to changes in the back-porch and sync-tip levels. The 10-bit composite video is multiplied by the sub carrier signals in the quadrature demodulator to generate U and V color difference signals. The U and V signals are then sent to low-pass filters to achieve the desired bandwidth. An adaptive 5-line comb filter separates UV from Y based on the unique property of color phase shifts from line to line. The chroma is re-modulated through a quadrature modulator and subtracted from line-delayed composite video to generate luma. This form of Y/C

separation is completely complementary, thus there is no loss of information. However, in some applications, it is desirable to limit the U/V bandwidth to avoid crosstalk. In that case, notch filters can be turned on. To accommodate some viewing preferences, a peaking filter is also available in the luma path. Contrast, brightness, sharpness, hue, and saturation controls are programmable through the I^{2}C host port. Figure 3-3 shows the block diagram of Composite Processor.
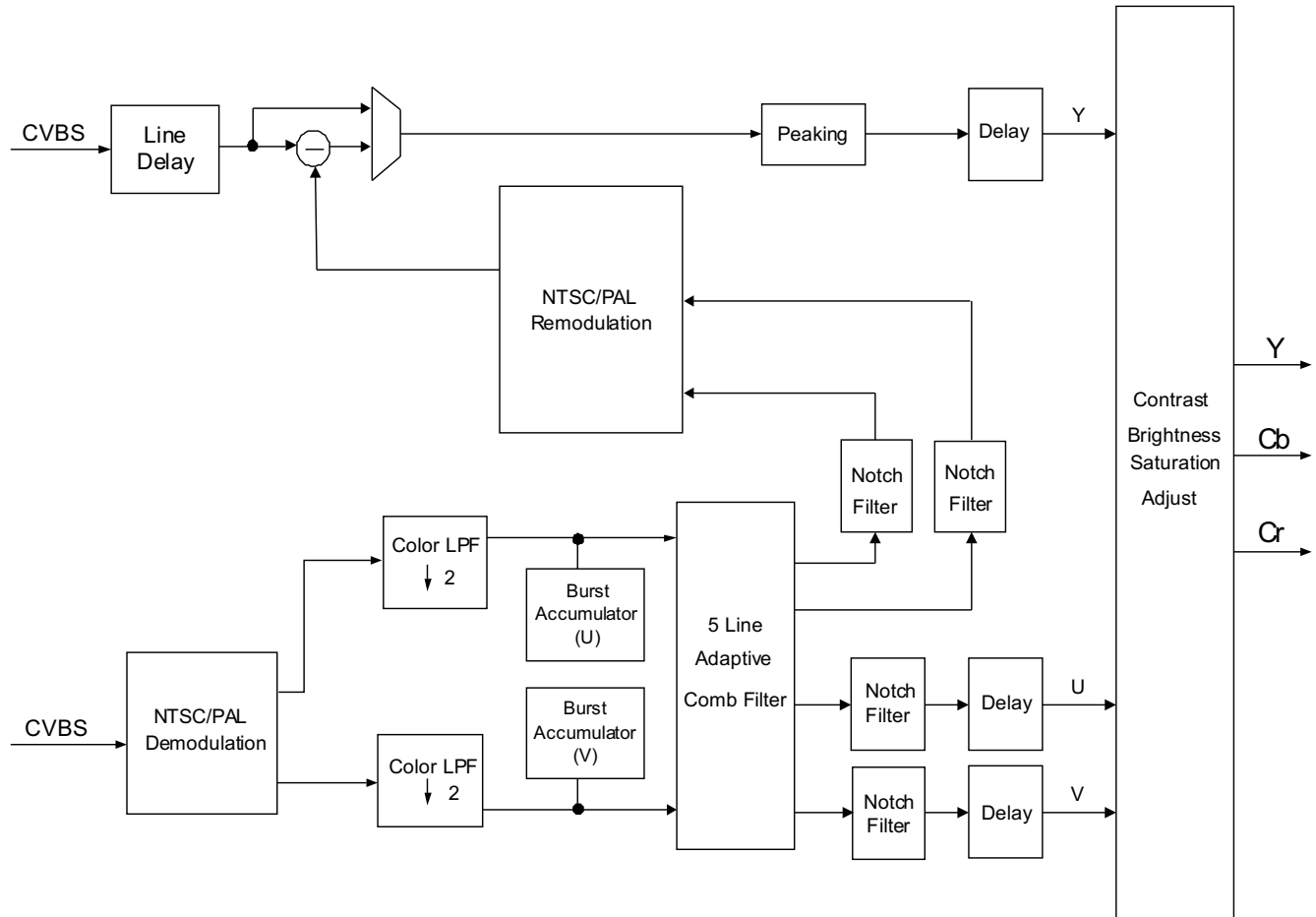
Figure 3-3. Composite Processor Block Diagram

3.2.3.1 Color Low-Pass Filter

High filter bandwidth preserves sharp color transitions and produces crisp color boundaries. However, for nonstandard video sources that have asymmetrical U and V side bands, it is desirable to limit the filter bandwidth to avoid UV crosstalk. The color low-pass filter bandwidth is programmable to enable one of the three notch filters. Figure 3-4 and Figure 3-5 represent the frequency responses of the wideband color low-pass filters.
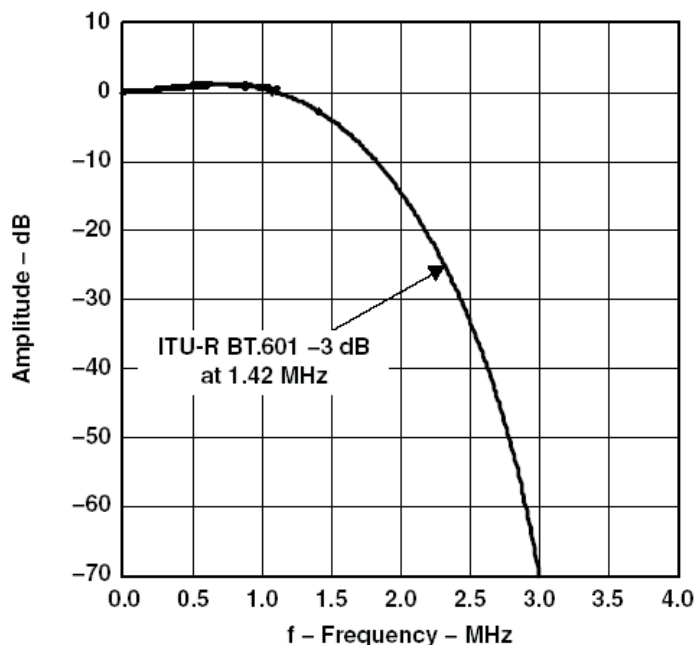
Figure 3-4. Color Low-Pass Filter Frequency Response
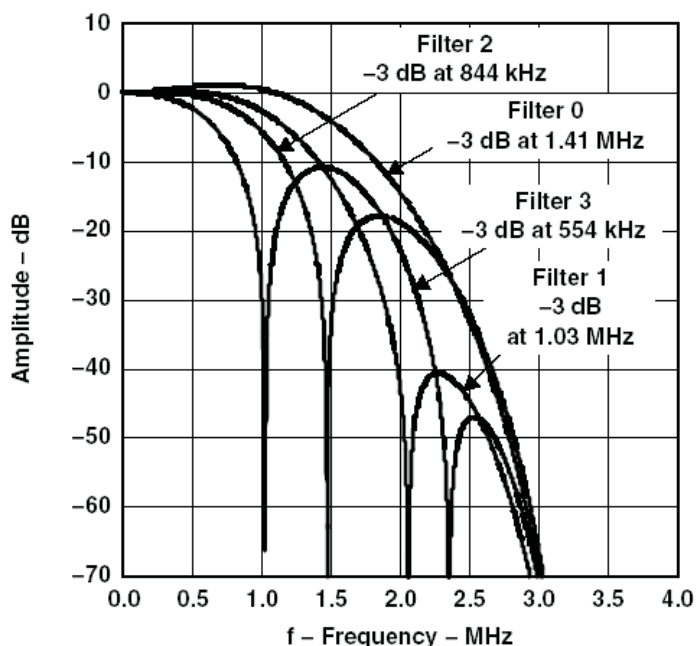
Figure 3-5. Color Low-Pass Filter with Filter Characteristics, NTSC/PAL ITU-R BT.601 Sampling

3.2.3.2 Y/C Separation

Y/C separation can be done using adaptive 5-line (5-H delay) comb filters or a chroma trap filter. The comb filter can be selectively bypassed in the luma or chroma path. If the comb filter is bypassed in the luma path, then chroma trap filters are used which are shown in Figure 3-6 and Figure 3-7. The TI patented adaptive comb filter algorithm reduces artifacts such as hanging dots at color boundaries. It detects and properly handles false colors in high-frequency luminance images such as a multiburst pattern or circle pattern.
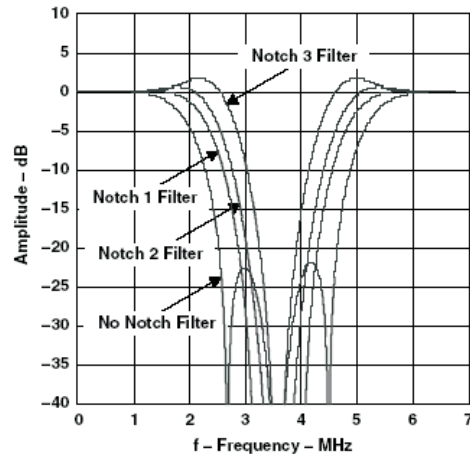
Figure 3-6. Chroma Trap Filter Frequency Response, NTSC ITU-R BT.601 Sampling
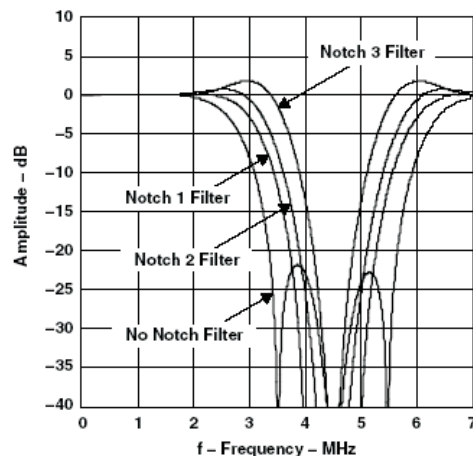
Figure 3-7. Chroma Trap Filter Frequency Response, PAL ITU-R BT.601 Sampling

3.2.4 Luminance Processing

The digitized composite video signal passes through either a luminance comb filter or a chroma trap filter, either of which removes chrominance information from the composite signal to generate a luminance signal. The luminance signal is then fed into the input of a peaking circuit. Figure 3-8 shows the basic functions of the luminance data path. A peaking filter (edge enhancer) amplifies high-frequency components of the luminance signal. Figure 3-9 shows the characteristics of the peaking filter at four different gain settings that are user-programmable via the I^{2}C interface.
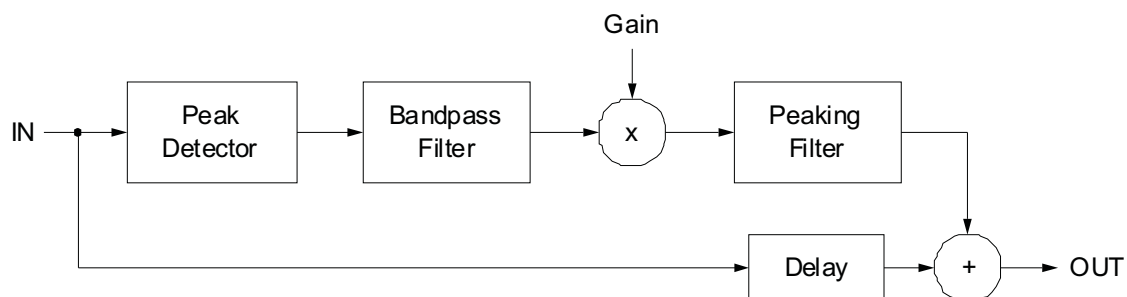
Figure 3-8. Luminance Edge-Enhancer Peaking Block Diagram
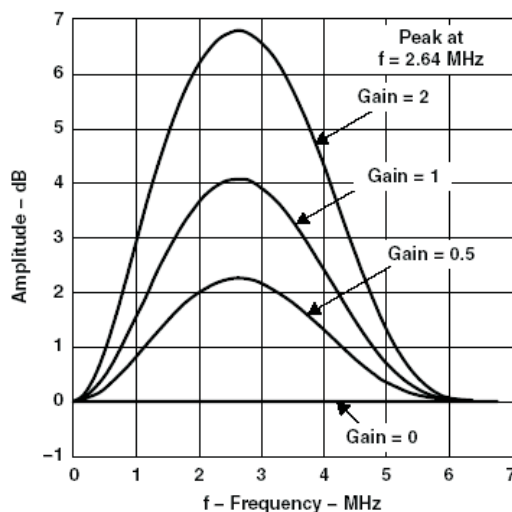
Figure 3-9. Peaking Filter Response, NTSC/PAL ITU-R BT.601 Sampling

3.3 AVID Cropping

AVID or active video cropping provides a means to decrease the amount of video data output. This is accomplished by horizontally blanking a number of AVID pulses and by vertically blanking a number of lines per frame. Horizontal cropping can be enabled/disabled using bit-6 of address B1h. When line cropping is enabled, active video will be reduced from 720 to 704 pixels for unscaled video and from 360 to 352 pixels for down-scaled video.

When line cropping is enabled, the TVP5158 crops an equal amount from both the start and end of active video. Register 8Ch can be used to delay both the start and end of active video. It allows selecting which 704 pixels out of 720 are actually being used for active video when line cropping is enabled.

3.4 Embedded Syncs

Standards with embedded syncs insert SAV and EAV codes into the data stream at the beginning and end of horizontal blanking. These codes contain the V and F bits which also define vertical timing. F and V change on EAV. Table 3-1 gives the format of the SAV and EAV codes.

H equals 1 always indicates EAV. H equals 0 always indicates SAV. The alignment of V and F to the line and field counter varies depending on the standard. Please refer to ITU-R BT.656 for more information on embedded syncs.

The P bits are protection bits:

P3 = V xor H
P2 = F xor H
P1 = F xor V
P0 = F xor V xor H

Table 3-1. EAV and SAV Sequence

	8-BIT DATA							
	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
Preamble	1	1	1	1	1	1	1	1
Preamble	0	0	0	0	0	0	0	0
Preamble	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0

3.5 Scaler

Each video decoder has an independent horizontal and vertical scaler, which supports D1 to half-D1 or CIF conversion. Table 3-2 gives the details of video resolution including un-cropped and cropped. Table 3-3 shows the video resolutions converted by the scaler.

Table 3-2. Standard Video Resolutions

Format	Uncropped		Cropped	
	NTSC	PAL	NTSC	PAL
D1	720 x 480	720 x 576	704 x 480	704 x 576
Half-D1	360 x 480	360 x 576	352 x 480	352 x 576
CIF	360 x 240	360 x 288	352 x 240	352 x 288

Table 3-3. Video Resolutions Converted by the Scaler

Scaling Ratio	Format	Horizontal Scaling	Vertical Scaling	Total Pixel	Active Output Resolution
D1	NTSC	1:1	1:1	858 x 525	720 x 480
	PAL	1:1	1:1	864 x 625	720 x 576
D1 to Half-D1	NTSC	2:1	1:1	429 x 525	360 x 480
	PAL	2:1	1:1	432 x 625	360 x 576
D1 to CIF	NTSC	2:1	2:1	429 x 262	360 x 240
	PAL	2:1	2:1	432 x 312	360 x 288

3.6 Noise Reduction

A video sequence shot under low light condition, which is typical of video surveillance applications, can contain lots of noise. Human eyes are very sensitive to oscillating signals, the visual quality degenerates significantly even when the noise level is small.

Each video decoder uses a TI proprietary spatial filter to reduce video noise. For each frame of image, the video noise filter (VNF) produces an estimate of the Y/U/V noise. Based on the noise estimates, the firmware adjusts the threshold for Y/U/V filtering. The filtered video shows improved video quality and lower compression bit-rate. The firmware can also utilize the Y/U/V noise estimates to make decisions to disable color if the video noise is determined to be too high. This "color killer" decision bit can be used to control another module that implements the color killing function.

The Noise Reduction can be controlled using I^2C registers from 50h to 5Fh. This module can also be set to bypass mode by I^2C register 5Dh (Bit 0).

3.7 Auto Contrast

The Auto Contrast (AC) module can adjust the picture brightness automatically or manually (user programmable) for better image quality. The goal of AC processing is to make the dark area brighter and high-light area dimmer. This makes it possible for the viewer to see details hidden in the shadows. It also prevents loss of details in the washed-out high light area. The AC processing is mostly for video surveillance applications.

For each frame of image, the auto contrast module collects the statistics of its Y (luminance) values. The AC algorithm implemented in the firmware processes the statistics and generates a look-up table (LUT). This LUT is used to map each incoming pixel Y value to an output pixel Y value for the next frame of image. The LUT is updated during the blanking period between two frames.

The Auto Contrast Mode can be controlled by using I^2C registers 0Fh. This module can also be set to disable mode by I^2C register 0Fh (Bit 1:0).

3.8 Output Formatter

The output formatter is responsible for generating the output digital video stream. Table 3-4 provides a summary of line frequencies, data rates, and pixel counts for different input standards. TVP5158 supports non-interleaved output mode, pixel-interleaved output mode and line-interleaved output mode. The non-interleaved mode is similar to the TVP5154A device, except that a single fixed clock output is used. In the interleaved modes, the video output data from multiple decoder channels are multiplexed together and then output to a single 8-bit or 16-bit port. The video output data from selected channels can be interleaved on a pixel or line basis.

Table 3-4. Summary of Line Frequencies, Data Rates and Pixel Counts for Different Standards

STANDARDS (ITU-R BT.601)	PIXELS PER LINE	ACTIVE PIXELS PER LINE	LINES PER FRAME	PIXEL FREQUENCY (MHz)	COLOR SUB-CARRIER FREQUENCY (MHz)	HORIZONTAL LINE RATE (kHz)
NTSC-J, M	858	720	525	13.5	3.579545	15.73426
NTSC-4.43	858	720	525	13.5	4.43361875	15.73426
PAL-M	858	720	525	13.5	3.57561149	15.73426
PAL-60	858	720	525	13.5	4.43361875	15.73426
PAL-B, D, G, H, I	864	720	625	13.5	4.43361875	15.625
PAL-N	864	720	625	13.5	4.43361875	15.625
PAL-Nc	864	720	625	13.5	3.58205625	15.625

3.8.1 Non-Interleaved Mode

In the non-interleaved mode, the YCbCr digital output is programmed as 8-bit ITU-R BT.656 parallel interface standard. Depending on which output mode is selected, the output for each channel can be un-scaled data or scaled data. Also each video output port can be selected to output the video data from any 1 of 4 video decoders. Table 3-5 shows the detailed information about non-interleaved mode.

Table 3-5. Output Ports Configuration for Non-Interleave Mode

VIDEO OUTPUT FORMATS	DATA CLOCK RATE (MHz)	INTERFACE TYPE	DVO_A	DVO_B	DVO_C	DVO_D
1-Ch D1	27	Quad BT.656	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch
1-Ch Half-D1	27	Quad BT.656	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch
1-Ch CIF	27	Quad BT.656	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch	Any 1 of 4 Ch

3.8.2 Pixel-Interleaved Mode

Each video decoder supports multiplexing two or four channels ITU-R BT.656 format data together on a pixel basis. The output from each video decoder channel is still ITU-R BT.656 format. After the processing in output formatter, two or four channels video data has been interleaved together by strictly one pixel from each channel.

The pixel-interleaved mode is dedicated for the backend chip which has limited video input ports. Table 3-6 gives the output port configuration for pixel-interleaved mode.

Table 3-6. Output Ports Configuration for Pixel-Interleaved Mode

VIDEO OUTPUT FORMATS	DATA CLOCK RATE (MHz)	INTERFACE TYPE	INTERLEAVE MODE	DVO_A	DVO_B	DVO_C	DVO_D
2-Ch D1	54	Dual BT.656	Pixel Based	Any 2 of 4 Ch	Any 2 of 4 Ch	Hi-Z	Hi-Z
4-Ch D1	108	Single BT.656	Pixel Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch Half-D1	54	Single BT.656	Pixel Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch CIF	54	Single BT.656	Pixel Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z

3.8.2.1 2-Ch Pixel-Interleaved Mode

In 2-Ch pixel-interleaved mode, the video output data with D1 resolution from two video channels is multiplexed pixel by pixel at 54 MHz. The output ports DVO_A and DVO_B are used in this mode. The output clocks OCLK_P and OCLK_N are synchronized with each channel so that the backend chip can de-multiplexed each video channel data easily. The video output from each channel is compatible with ITU-R BT.656 format. Figure 3-10 shows the timing diagram for 2-Ch pixel-interleaved mode.
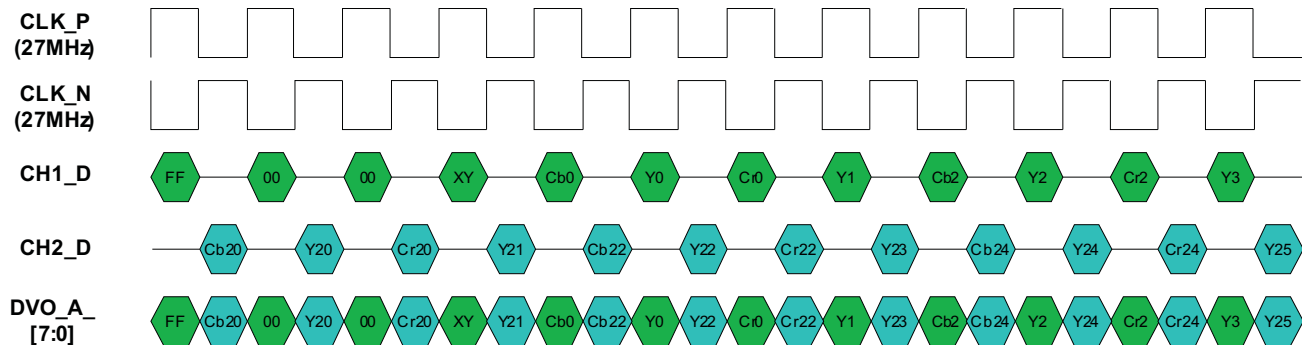
Figure 3-10. 2-Ch Pixel-Interleaved Mode Timing Diagram

3.8.2.2 4-Ch Pixel-Interleaved Mode

In 4-Ch pixel-interleaved mode, the video output data with D1 resolution from four video channels is multiplexed pixel by pixel at 108 MHz. The output DVO_A is used in this mode. The output clock OCLK_P is synchronized with all four channels data. Each channel video data is compatible with ITU-R BT.656 format. Figure 3-11 shows the timing diagram for 4-Ch pixel-interleaved mode.
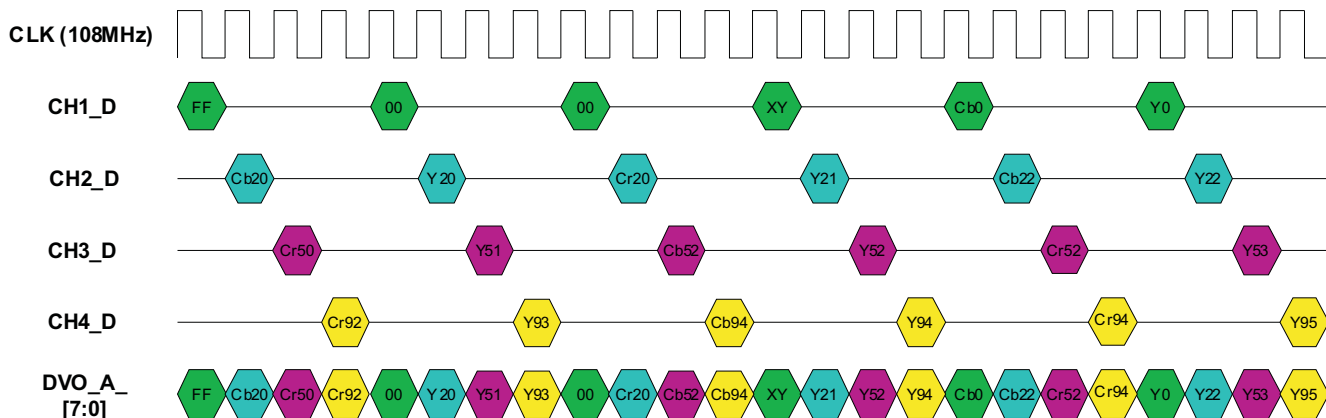
Figure 3-11. 4-Ch Pixel-Interleaved Mode Timing Diagram

In 4-Ch pixel-interleaved mode, TVP5158 also supports Half-D1 and CIF format data multiplexed at 54 MHz. The output DVO_A is used in this mode. The output clock OCLK_P is synchronized with all four channels data.

3.8.2.3 Metadata Insertion for Non-Interleave Mode and Pixel-Interleaved Mode

In non-interleaved mode and pixel-interleaved mode, the video detection status (VDET) has also been inserted in MSB of SAV/EAV control byte. Table 3-7 shows VDET status insertion in SAV/EAV codes.

Table 3-7. VDET Statues Insertion in SAV/EAV Codes

CONDITION			FVH VALUE			SAV/EAV CODE SEQUENCE				
FIELD	V TIME	H TIME	F	V	H	1st	2nd	3rd	4th	
									VDET = 1	VDET = 0
1	Active	SAV	0	0	0	FFh	00h	00h	80h	00h
1	Active	EAV	0	0	1	FFh	00h	00h	9Dh	1Dh
1	Blank	SAV	0	1	0	FFh	00h	00h	ABh	2Bh
1	Blank	EAV	0	1	1	FFh	00h	00h	B6h	36h
2	Active	SAV	1	0	0	FFh	00h	00h	C7h	47h
2	Active	EAV	1	0	1	FFh	00h	00h	DAh	5Ah
2	Blank	SAV	1	1	0	FFh	00h	00h	ECh	6Ch
2	Blank	EAV	1	1	1	FFh	00h	00h	F1h	71h

In the pixel-interleaved mode, Channel ID is inserted in the horizontal blanking code as Table 3-8. The backend chip can easily identify the video data from which video decoder channel by inserted Channel ID.

Table 3-8. Channel ID Insertion in Horizontal Blanking Code

CHANNEL	H BLANKING CODE WITH CHANNEL ID		
	Y	Cb	Cr
Ch1	10h	80h	80h
Ch2	11h	81h	81h
Ch3	12h	82h	82h
Ch4	13h	83h	83h

In the pixel-interleaved mode, Channel ID can also be inserted in 4 LSBs of SAV/EAV control byte replacing protection bits as Table 3-9.

Table 3-9. Channel ID Insertion in SAV/EAV Code Sequence

CONDITION			FVH VALUE			SAV/EAV CODE SEQUENCE						
FIELD	V TIME	H TIME	F	V	H	1st	2nd	3rd	4th			
									Ch1	Ch2	Ch3	Ch4
1	Active	SAV	0	0	0	FFh	00h	00h	80h	81h	82h	83h
1	Active	EAV	0	0	1	FFh	00h	00h	90h	91h	92h	93h
1	Blank	SAV	0	1	0	FFh	00h	00h	A0h	A1h	A2h	A3h
1	Blank	EAV	0	1	1	FFh	00h	00h	B0h	B1h	B2h	B3h
2	Active	SAV	1	0	0	FFh	00h	00h	C0h	C1h	C2h	C3h
2	Active	EAV	1	0	1	FFh	00h	00h	D0h	D1h	D2h	D3h
2	Blank	SAV	1	1	0	FFh	00h	00h	E0h	E1h	E2h	E3h
2	Blank	EAV	1	1	1	FFh	00h	00h	F0h	F1h	F2h	F3h

3.8.3 Line-Interleaved Mode Support (TVP5158 only)

TVP5158 supports line-interleaved modes to multiplex 2 or 4 video channels outputs together line by line. Compared to pixel-interleaved mode, the line-interleaved mode significantly reduces the code complexity and MIPS consumption of the backend DSP.

TVP5158 supports 2-Ch and 4-Ch line-interleaved modes. Each mode supports different resolutions including D1, Half-D1 and CIF. Table 3-10 includes all line-interleaved modes supported by a single TVP5158 device.

Table 3-10. Line-Interleaved Modes

VIDEO OUTPUT FORMATS	DATA CLOCK RATE (MHz)	INTERFACE TYPE	INTERLEAVE MODE	DVO_A	DVO_B	DVO_C	DVO_D
2-Ch D1	54	Dual BT.656	Line Based	Any 2 of 4 Ch	Any 2 of 4 Ch	Hi-Z	Hi-Z
4-Ch D1	108	Single BT.656	Line Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch Half-D1	54	Single BT.656	Line Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch CIF	27	Single BT.656	Line Based	All 4 Ch	Hi-Z	Hi-Z	Hi-Z
4-Ch D1	54	16-bit BT.601	Line Based	All 4 Ch (Y data)	All 4 Ch (C data)	Hi-Z	Hi-Z
4-Ch Half-D1	27	16-bit BT.601	Line Based	All 4 Ch (Y data)	All 4 Ch (C data)	Hi-Z	Hi-Z
4-Ch CIF + 1-Ch D1	54	Single BT.656	Line Based	All 4 Ch CIF + Any 1 of 4 D1	Hi-Z	Hi-Z	Hi-Z
4-Ch Half-D1 + 1-Ch D1	108	Single BT.656	Line Based	All 4 Ch Half-D1 + Any 1 of 4 D1	Hi-Z	Hi-Z	Hi-Z

3.8.3.1   2-Ch Line-Interleaved Mode

TVP5158 supports 2-Ch line-interleaved mode at 54 MHz. The video output data with D1 resolution from any two video channels is multiplexed together on a line basis. The output ports DVO_A and DVO_B are used in this mode. The output clock OCLK_P is synchronized with both output ports.

3.8.3.2   4-Ch Line-Interleaved Mode

In 4-Ch line-interleaved mode, the video output data from all 4 channels is multiplexed together on a line basis. The output resolution of video data can be D1, Half-D1 or CIF. For D1 and Half-D1 output resolutions, the video output port can be configured to support 8-bit BT.656 or 16-Bit YCbCr 4:2:2 data with embedded sync. Port DVO_A is used for 8-bit output. Ports DVO_A and DVO_B are used for 16-Bit output. The output clock OCLK_P is synchronized with all four output ports.

TVP5158 supports multiplexing 4-Ch CIF and 1-Ch D1 data together and then output through DVO_A at 54 MHz. 1-Ch D1 can be from any one of 4 video channels. In typical surveillance applications, CIF resolution is used for recording and D1 resolution is used for video preview.

TVP5158 also supports multiplexing 4-Ch Half-D1 and 1-Ch D1 data together and then output through DVO_A at 108 MHz. The backend chip can use Half-D1 to generate CIF format by dropped one field.

Pleas note that the line-interleaved mode does NOT strictly output one line from each decoder channel sequentially. The order of multiplexed the video line data is based on the availability of video output data from each decoder channel. Therefore, it is possible to output two consecutive lines from the same decoder channel or to skip one decoder channel output.

3.8.3.3   Video Cascade Mode

Two TVP5158 devices can be cascade connected and work as single 8-Ch video decoder. In cascade mode, the port DVO_C and DVO_D of master TVP5158 (first stage) can be configured as the video input interface. The DVO_A and DVO_B of master TVP5158 are configured as the output interface for two devices. This mode is dedicated for the backend chip with extremely limited input ports. Table 3-11 includes all cascade modes in TVP5158.

For the modes of 4-Ch CIF + 1 - Ch D1 at 54 MHz and 8-Ch CIF + 1 - Ch D1 at 108 MHz modes, the D1 line is broken into two equal-length half lines and then multiplex with other CIF lines. Therefore, all video data is actually multiplexed by CIF line length. Additionally, in these two modes, both the scaled and un-scaled data streams must use the same line cropping setting. The cropping setting can be controlled by I^{2}C register B1h (Bit 6).

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Table 3-11. TVP5158 Video Cascade Modes

VIDEO OUTPUT FORMATS	CASCADE STAGE	DATA CLOCK RATE (MHz)	INTERFACE TYPE	INTERLEAVE MODE	DVO_A	DVO_B	DVO_C	DVO_D
8-Ch CIF	1st Stage	54	Single BT.656	Line Based	All 8 Ch CIF	Hi-Z	Hi-Z	4-Ch CIF Input
	2nd Stage	27	Single BT.656	Line Based	All 4 Ch CIF	Hi-Z	Hi-Z	Hi-Z
8-Ch Half-D1	1st Stage	108	Single BT.656	Line Based	All 8 Ch Half-D1	Hi-Z	Hi-Z	4-Ch Half-D1 Input
	2nd Stage	54	Single BT.656	Line Based	All 4 Ch Half-D1	Hi-Z	Hi-Z	Hi-Z
8-Ch CIF + 1-Ch D1	1st Stage	108	Single BT.656	Line Based	All 8 Ch CIF + Any 1 of 8 D1	Hi-Z	1-Ch D1 Input	4-Ch CIF Input
	2nd Stage	27/27	Dual BT.656	Line Based	All 4 Ch CIF	Any 1 of 4 Ch D1	Hi-Z	Hi-Z

Typical applications with cascade mode show on next several pages.

shows the Cascade Connection for 16-Ch CIF Recoding and Multi-Ch CIF Preview.

shows the Cascade Connection for 16-Ch CIF Recoding and Multi-Ch Half-D1 Preview.

shows the Cascade Connection for 16-Ch CIF Recoding and 2-Ch D1/Multi-Ch CIF Preview.

Figure 3-12. Cascade Connection for 16-Ch CIF Recoding and Multi-Ch CIF Preview
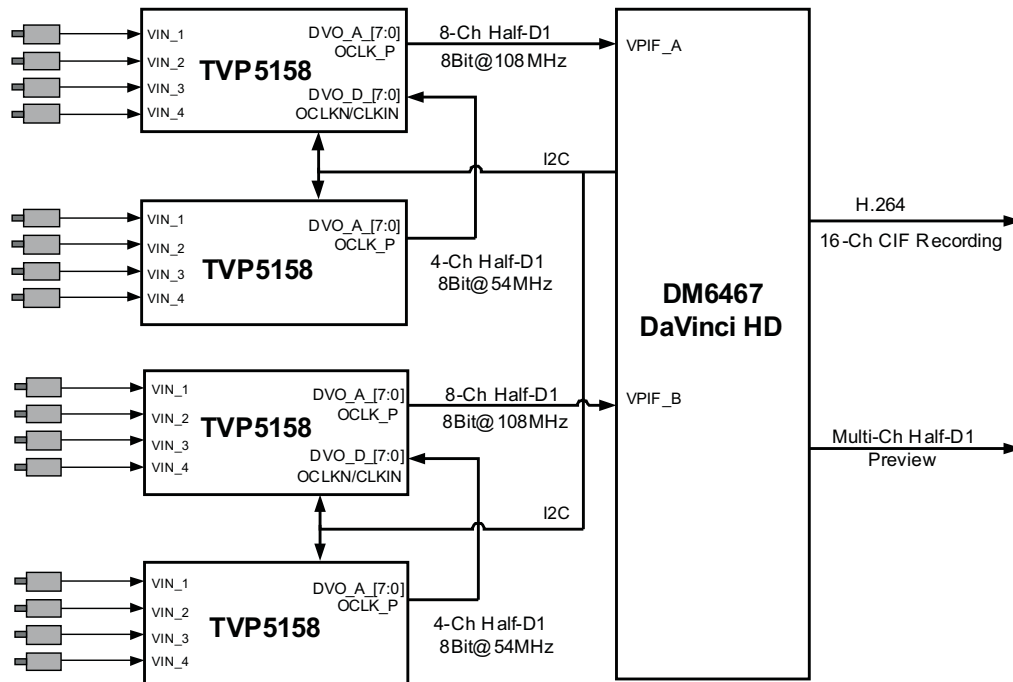
Figure 3-13. Cascade Connection for 16-Ch CIF Recoding and Multi-Ch Half-D1 Preview
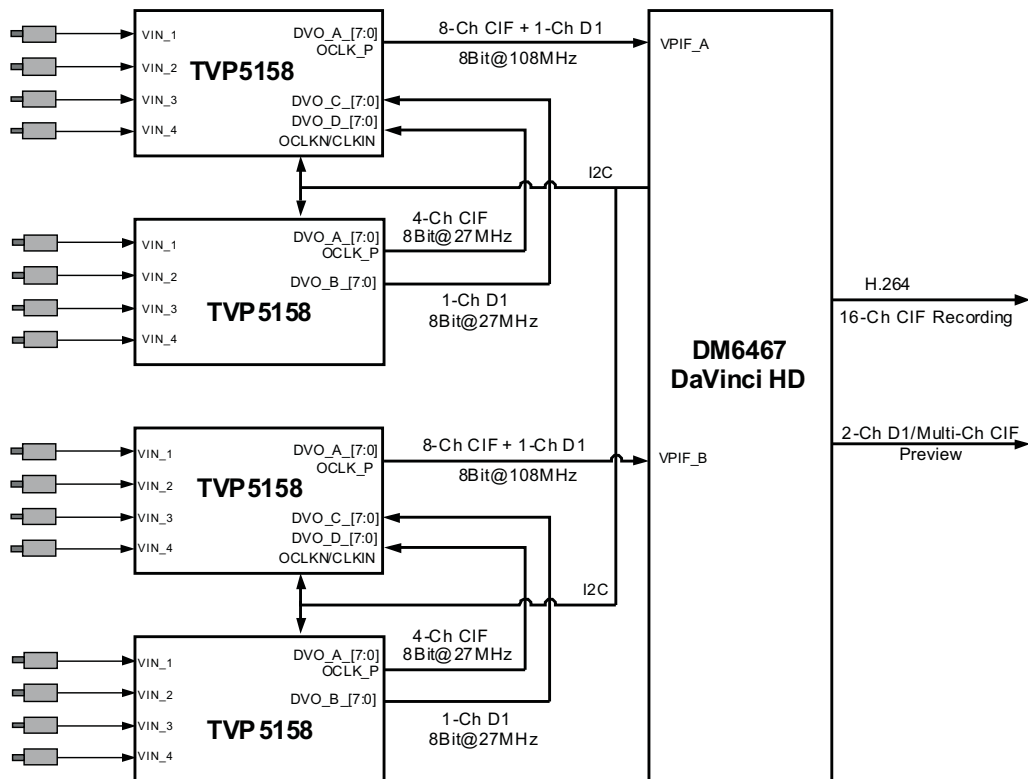
Figure 3-14. Cascade Connection for 16-Ch CIF Recoding and 2-Ch D1/Multi-Ch CIF Preview

3.8.3.4 Metadata Insertion for Line-Interleaved Mode

In the line-interleaved mode, the video data is rearranged on a line-by-line basis. There can be no guaranteed output line order since all analog video inputs are not synchronized. In order to be compatible with general backend BT.656 decoder, the video data is encapsulated on TVP5158 output so that all input data is preserved and output data is understandable to a BT.656 decoder.

To prevent confusion over image line count and vertical blanking appearing haphazardly, SAV/EAV codes will have FID and V data stripped and replaced with FID=V=0. Since vertical blanking in the input is being masked out, artificial vertical sync will be inserted every encapsulated frame (a.k.a. super frame). Thus to the unaware BT.656 decoder, the stream will appear to be progressive data with 2 lines of vertical blanking.

4-Byte Start Code (SC3:SC0) is inserted immediately after SAV code for encapsulated frame. Figure 3-15 and Figure 3-16 show the start code details.
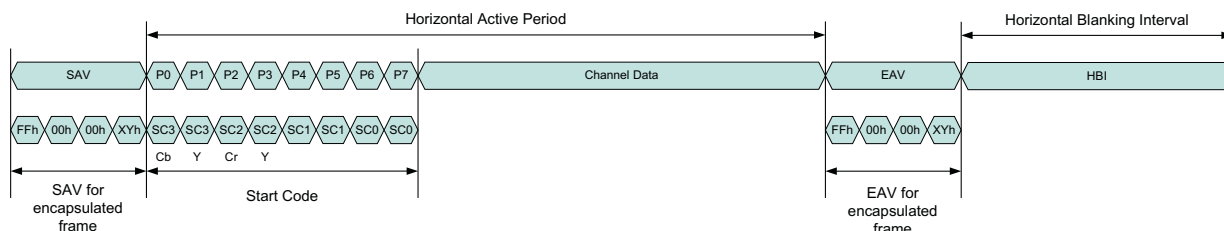
Figure 3-15. Start Code in 8-Bit BT.656 Interface
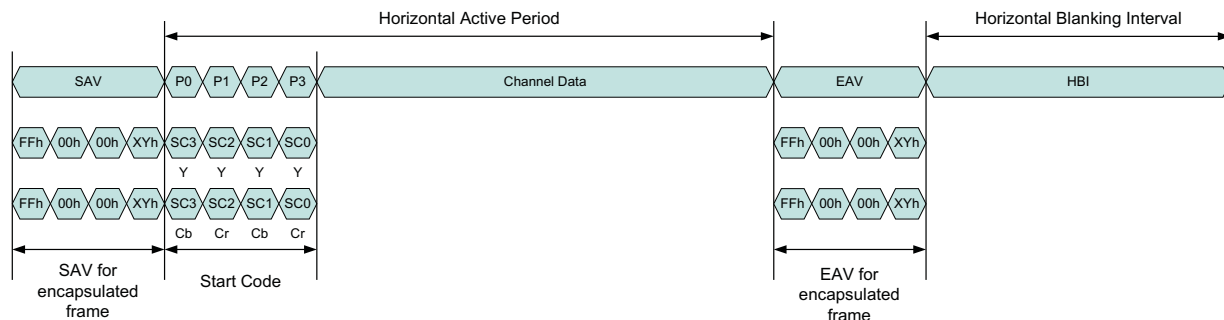
Figure 3-16. Start Code in 16-Bit YCbCr 4:2:2 Interface

Table 3-12 and Table 3-13 show the bit assignment and field definition of 4-Byte start code for Active Video Line.

Table 3-12. Bit Assignment of 4-Byte Start Code for Active Video Line

BYTE	7	6	5	4	3	2	1	0
SC[3]	1	RSVD	RSVD	RSVD		VCS_ID	CH_ID[1:0]	
SC[2]	0	BOL	EOL	VDET	RSVD		LN_ID[8:7]	
SC[1]	~LD_ID[6]	LN_ID[6:0]						
SC[0]	1	F	V	H	P3	P2	P1	P0

Functional Description   29

Table 3-13. Bit Field Definition of 4-Byte Start Code for Active Video Line

BIT	NAME	FUNCTION
31	1	Reserved. Must be set to 1.
30	RSVD	Reserved.
29	RSVD	Reserved.
[28:27]	RSVD	Reserved (to support up to 32 video channels)
26	VCS_ID	Video cascade stage ID. Set to 0 for normal operation. In cascade mode, the back-end device (e.g., TMS320DM6467) interfaces to the first stage. 0: First stage (channels 1 to 4) 1: Second stage (channels 5 to 8)
[25:24]	CH_ID[1:0]	2-bit Channel ID. Video decoder channel number. 00: Channel 1 01: Channel 2 10: Channel 3 11: Channel 4
23	0	Reserved. Must be set to 0.
22	BOL	Active-high beginning of line flag. Used in split-line mode which may be required for hybrid formats (e.g. 1-Ch D1 + 8-Ch CIF). Set high when the current encapsulated line of channel data includes the beginning of a video line. 0: BOL not included (2nd half of split line) 1: BOL included (1st half of split line or full line)
21	EOL	Active-high end of line flag. Used in split-line mode which may be required for hybrid formats (e.g. 1-Ch D1 + 8-Ch CIF). Set high when the current line of channel data includes the end of a video line. 0: EOL not included (1st half of split line) 1: EOL included (2nd half of split line or full line)
20	VDET	Active-high video detection status 0: Video not detected 1: Video detected
[19:18]	RSVD	Reserved.
[17:16]	LN_ID[8:7]	Two MSBs of 9-bit Line ID, active video line number. Line counter resets to 000h at beginning of active video (i.e., resets once per field). During the vertical blanking interval, the line counter may either continue counting or hold the terminal count determined at the end of active video.
15	~LN_ID[6]	Reserved. Must be set to the complement of bit 14 (LN_ID[6]).
[14:8]	LN_ID[6:0]	Seven LSBs of 9-bit Line ID, active video line number. Line counter resets to 000h at beginning of active video (i.e., resets once per field). During the vertical blanking interval, the line counter may either continue counting or hold the terminal count determined at the end of active video.
7	1	Reserved. Must be set to 1.
6	F	F-bit 0: First field of frame 1: Second field of frame
5	V	V-bit 0: when not in vertical blanking 1: during vertical blanking
4	H	H-bit. Always set to 0. 0: SAV 1: EAV (never used)
3	P3	P3 = V XOR H, Protection bits used for error detection/correction
2	P2	P2 = F XOR H, Protection bits used for error detection/correction
1	P1	P1 = F XOR V, Protection bits used for error detection/correction
0	P0	P0 = F XOR V XOR H, Protection bits used for error detection/correction

NOTE

For line-interleaved output mode, if none of video decoder channels has the data ready at a given time, TVP5158 outputs the dummy line until any one of video decoder channels is ready to output a line. The backend chip needs to keep only the active video line and ignore the dummy line.

The start code of the dummy line is different with active video line. Table 3-14 shows the bit assignment and field definition of 4-Byte start code for the Dummy Line.

Table 3-14. Bit Assignment of 4-Byte Start Code for the Dummy Line

BYTE	7	6	5	4	3	2	1	0
SC[3]	0	0	0	0	0	0	0	1
SC[2]	0	0	0	0	0	0	0	1
SC[1]	0	0	0	0	0	0	0	1
SC[0]	0	0	0	0	0	0	0	1

NOTE

The Dummy Line can be easily distinguished from active video line by simply looking at the MSB of byte SC[0].

3.9 Audio Sub-System (TVP5157 and TVP5158 Only)

The audio sub-system integrates 4-Ch audio analog-to-digital converters, digital processing and I^{2}S encoder. TVP5158 audio sub-system supports 4-Ch mono analog audio input and standard/multiple I^{2}S output. TVP5158 also supports audio cascade connection up to four devices cascade connected for 16-Ch audio input.

3.9.1 Features

- Four mono analog audio input channels
  - Requires external passive attenuator to support 2.828-Vpp analog audio input
- Programmable Gain Amplifier (PGA)
  - Gain range: -12 ~ 0 dB, Gain Step: 1.5 dB
- Integrated Anti-Aliasing Filter (AAF)
- 10-Bit Analog-to-Digital Converter
- Integrates Audio High-pass filter to eliminate low frequency hum
- Digital serial audio interface
  - 16-Bit Linear PCM, 8-Bit A-Law and 8-Bit µ-Law Data
  - I^{2}S or DSP Format
  - Master and Slave mode operation
  - Up to 16 slots TDM output
  - 64 f_s or 256 f_s system clock
- Sampling Rate : 16 kHz , 8 kHz
- Audio Cascade connection
  - Up to 4 cascaded devices
  - I^{2}S format
  - 256 f_s system clock
- Audio Mixing Output
  - Audio ADC has one register to set mix ratio
  - The Mixing output pin SD_M can also be used for recording. Combined with the recording output pin SD_R, two I^{2}S bit-streams can be output simultaneously.

3.9.2 Audio Sub-System Functional Diagram
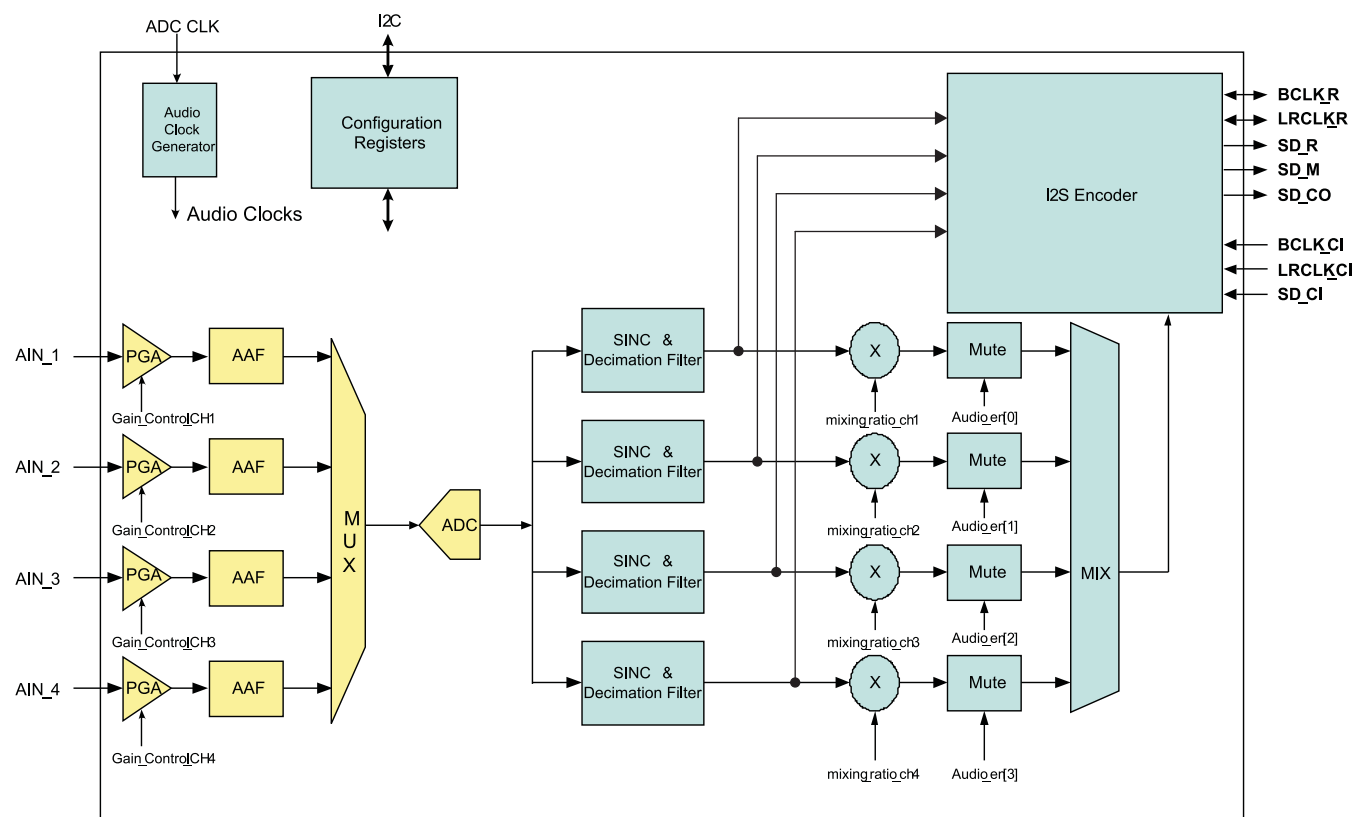
Figure 3-17. Audio Sub-System Functional Diagram

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3.9.3 Audio Cascade Connection
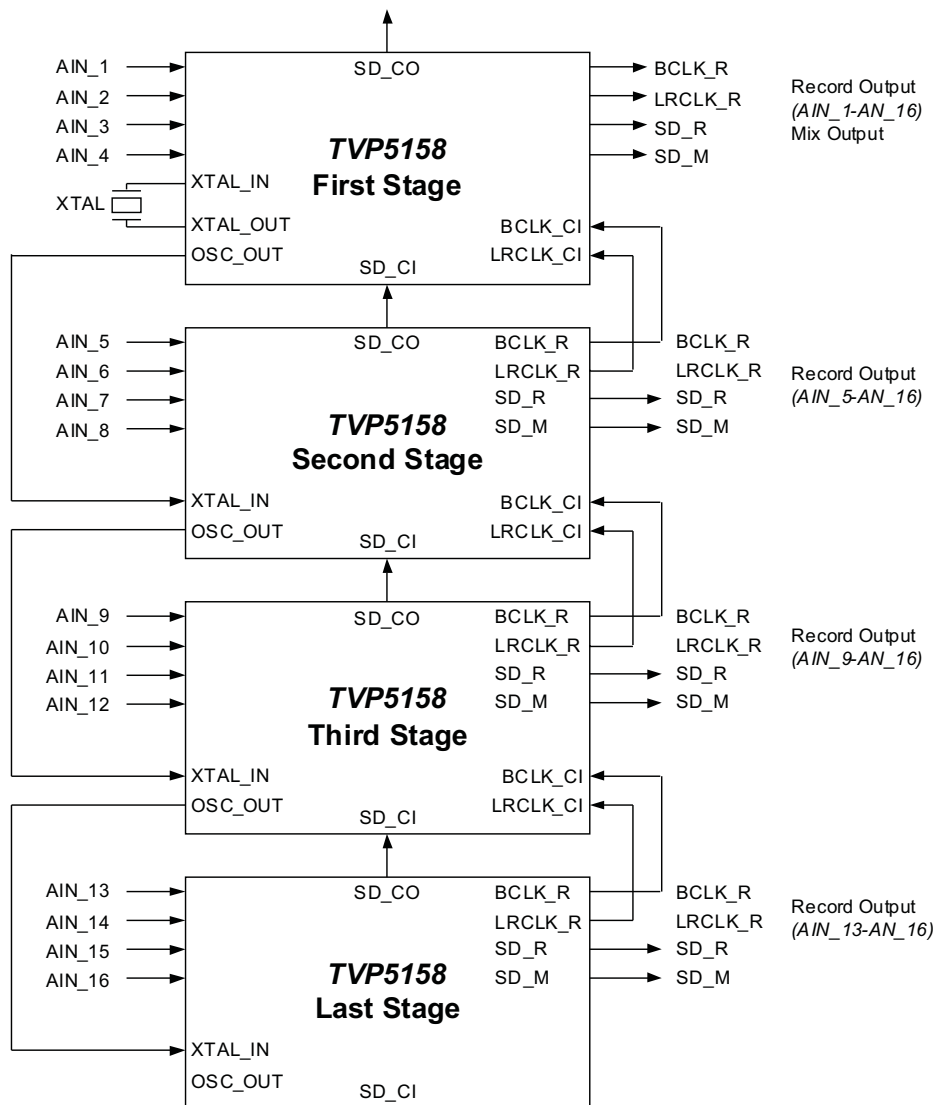
Figure 3-18. Audio Cascade Connection

TVP5158 supports up to 4 devices cascaded together for audio cascade connection. The I^{2}S output of master TVP5158 (1st stage) combines all audio channel data from cascaded TVP5158 devices.

Key Features of Audio Cascade Connection

- 16-Bit linear PCM data
- I^{2}S format
- Bit Clock: 256 f_s
- All cascade inputs are always in slave mode
- Second to fourth stage serial audio outputs are always in master mode
- First stage serial audio output can be in either master or slave mode
- Common clock source for all cascaded devices is required

The Serial Audio Output Channel Assignment shown on Table 3-15.

Table 3-15. Serial Audio Output Channel Assignment

I²S

tdm_ch	tdm_out_pin		Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8	Slot 9	Slot 10	Slot 11	Slot 12	Slot 13	Slot 14	Slot 15	Slot 16
						LRCLK_R Left								**LRCLK_R Right**				
0 (2 channel)	0	SD_R	AIN_1								AIN_2							
		SD_M																
	1	SD_R	AIN_1															
		SD_M	AIN_2															
1 (4 channel)	0	SD_R	AIN_1	AIN_3							AIN_2	AIN_4						
		SD_M																
	1	SD_R	AIN_1								AIN_2							
		SD_M	AIN_3								AIN_4							
2 (8 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7					AIN_2	AIN_4	AIN_6	AIN_8				
		SD_M																
	1	SD_R	AIN_1	AIN_5							AIN_2	AIN_6						
		SD_M	AIN_3	AIN_7							AIN_4	AIN_8						
3 (12 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_9	AIN_11			AIN_2	AIN_4	AIN_6	AIN_8	AIN_10	AIN_12		
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_9						AIN_2	AIN_6	AIN_10					
		SD_M	AIN_3	AIN_7	AIN_11						AIN_4	AIN_8	AIN_12					
4 (16 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_9	AIN_11	AIN_13	AIN_15	AIN_2	AIN_4	AIN_6	AIN_8	AIN_10	AIN_12	AIN_14	AIN_16
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_9	AIN_13					AIN_2	AIN_6	AIN_10	AIN_14				
		SD_M	AIN_3	AIN_7	AIN_11	AIN_15					AIN_4	AIN_8	AIN_12	AIN_16				

DSP Format

tdm_ch	tdm_out_pin		Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7	Slot 8	Slot 9	Slot 10	Slot 11	Slot 12	Slot 13	Slot 14	Slot 15	Slot 16
0 (2 channel)	0	SD_R	AIN_1	AIN_2														
		SD_M																
	1	SD_R	AIN_1															
		SD_M	AIN_2															
1 (4 channel)	0	SD_R	AIN_1	AIN_3	AIN_2	AIN_4												
		SD_M																
	1	SD_R	AIN_1	AIN_2														
		SD_M	AIN_3	AIN_4														
2 (8 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_2	AIN_4	AIN_6	AIN_8								
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_2	AIN_6												
		SD_M	AIN_3	AIN_7	AIN_4	AIN_8												
3 (12 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_9	AIN_11	AIN_2	AIN_4	AIN_6	AIN_8	AIN_10	AIN_12				
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_9	AIN_2	AIN_6	AIN_10										
		SD_M	AIN_3	AIN_7	AIN_11	AIN_4	AIN_8	AIN_12										
4 (16 channel)	0	SD_R	AIN_1	AIN_3	AIN_5	AIN_7	AIN_9	AIN_11	AIN_13	AIN_15	AIN_2	AIN_4	AIN_6	AIN_8	AIN_10	AIN_12	AIN_14	AIN_16
		SD_M																
	1	SD_R	AIN_1	AIN_5	AIN_9	AIN_13	AIN_2	AIN_6	AIN_10	AIN_14								
		SD_M	AIN_3	AIN_7	AIN_11	AIN_15	AIN_4	AIN_8	AIN_12	AIN_16								

3.10 I²C Host Interface

The I²C standard consists of two signals, serial input/output data line (SDA) and input/output clock line (SCL), which carry information between the devices connected to the bus. The input pins I2CA0, I2CA1 and I2CA2 are used to select the slave address to which the device responds. Although the I²C system can be multi-mastered, the TVP5158 decoder functions as a slave device only.

Both SDA and SCL must be connected to IOVDD via pullup resistors. When the bus is free, both lines are high. The slave address select terminals (I2CA0, I2CA1 and I2CA2) enable the use of up to eight devices on the same I^{2}C bus. At the trailing edge of reset, the status of the I2CA0, I2CA1 and I2CA2 lines are sampled to determine the device address used. Table 3-16 summarizes the terminal functions of the I^{2}C host interface. Table 3-17 shows the device address selection options.

Table 3-16. I^{2}C Terminal Description

SIGNAL	TYPE	DESCRIPTION
I2CA0	I	Slave address selection
I2CA1	I	Slave address selection
I2CA2	I	Slave address selection
SCL	I/O (open drain)	Input/output clock line
SDA	I/O (open drain)	Input/output data line

Table 3-17. I^{2}C Host Interface Device Addresses

A6	A5	A4	A3	A2(I2CA2)	A1(I2CA1)	A0 (I2CA0)	R/W	HEX
1	0	1	1	0	0	0	1/0	B1/B0
1	0	1	1	0	0	1	1/0	B3/B2
1	0	1	1	0	1	0	1/0	B5/B4
1	0	1	1	0	1	1	1/0	B7/B6
1	0	1	1	1	0	0	1/0	B9/B8
1	0	1	1	1	0	1	1/0	BB/BA
1	0	1	1	1	1	0	1/0	BD/BC
1	0	1	1	1	1	1	1/0	BF/BE

Data transfer rate on the bus is up to 400 Kbit/s. The number of devices connected to the bus is dependent on the bus capacitance limit of 400 pF. The data on the SDA line must be stable during the high period of the SCL except for start and stop conditions. The high or low state of the data line can only change with the clock signal on the SCL line being low. A high-to-low transition on the SDA line while the SCL is high indicates an I^{2}C start condition. A low-to-high transition on the SDA line while the SCL is high indicates an I^{2}C stop condition.

Every byte placed on the SDA must be 8 bits long. The number of bytes which can be transferred is unrestricted. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the I^{2}C master.

To simplify programming of each of the 4 decoder channels a single I^{2}C write transaction can be transmitted to any one or more of the 4 cores in parallel. This reduces the time required to download firmware or to configure the device when all channels are to be configured in the same manner. It also enables the addresses for all registers to be common across all decoders.

I^{2}C sub-address FEh contains 4 bits with each bit corresponding to one of the decoder cores. If a decoder write enable bit is set, then I^{2}C write transactions will be sent to the corresponding decoder core. For multi-byte I^{2}C write transactions there are options to auto-increment the sub-address or to auto-increment through the selected decoders or both.

I^{2}C sub-address FFh contains 4 bits with each bit corresponding to one of the decoder cores. If a decoder read enable bit is set, then I^{2}C read transactions will be sent to the corresponding decoder core.

If more than one decoder is enabled for reads then the lowest numbered decoder that is enabled will respond to the read transaction. For multi-byte I^{2}C read transactions there are options to auto-increment the sub-address or to auto-increment through the selected decoders or both.

3.10.1 I^2C Write Operation

Data transfers occur utilizing the following formats.

An I^2C master initiates a write operation to the decoder by generating a start condition (S) followed by the decoder I^2C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the decoder, the master presents the sub-address of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The decoder acknowledges each byte after completion of each transfer. The I^2C master terminates the write operation by generating a stop condition (P).

Step 1	0							
I^2C Start (master)	S							

Step 2	7	6	5	4	3	2	1	0
I^2C General address (master)	1	0	1	1	1	0	X	0

Step 3	9							
I^2C Acknowledge (slave)	A							

Step 4	7	6	5	4	3	2	1	0
I^2C Write register address (master)	Addr	Addr	Addr	Addr	Addr	Addr	Addr	Addr

Step 5	9							
I^2C Acknowledge (slave)	A							

Step 6[1]	7	6	5	4	3	2	1	0
I^2C Write data (master)	Data	Data	Data	Data	Data	Data	Data	Data

Step 7[1]	9							
I^2C Acknowledge (slave)	A							

Step 8	0							
I^2C Stop (master)	P							

(1)   Repeat steps 6 and 7 until all data have been written.

3.10.2 I^2C Read Operation

The read operation consists of two phases. The first phase is the address phase. In this phase, an I^2C master initiates a write operation to the decoder by generating a start condition (S) followed by the decoder slave address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledge from the decoder, the master presents the sub-address of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master has the option of generating a stop condition or not.

In the data phase, an I^2C master initiates a read operation to the decoder by generating a start condition followed by the decoder I^2C slave address (as shown below for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the decoder, the I^2C master receives one or more bytes of data from the decoder. The I^2C master acknowledges the transfer at the end of each byte. After the last data byte has been transferred from the decoder, the master generates a not acknowledge followed by a stop.

Read Phase 1

Step 1	0
I²C Start (master)	S

Step 2	7	6	5	4	3	2	1	0
I²C General address (master)	1	0	1	1	X	X	X	0

Step 3	9
I²C Acknowledge (slave)	A

Step 4	7	6	5	4	3	2	1	0
I²C Read register address (master)	Addr	Addr	Addr	Addr	Addr	Addr	Addr	Addr

Step 5	9
I²C Acknowledge (slave)	A

Step 6[1]	0
I²C Stop (master)	P

(1)   Step 6 is optional.

Read Phase 2

Step 7	0
I²C Start (master)	S

Step 8	7	6	5	4	3	2	1	0
I²C General address (master)	1	0	1	1	X	X	X	1

Step 9	9
I²C Acknowledge (slave)	A

Step 10[1]	7	6	5	4	3	2	1	0
I²C Read data (slave)	Data	Data	Data	Data	Data	Data	Data	Data

Step 11[1]	9
I²C Not Acknowledge (master)	$\overline{A}$

Step 12	0
I²C Stop (master)	P

(1)   Repeat steps 10 and 11 for all bytes read. Master does not acknowledge the last read data received.

3.11 Clock Circuits

An analog clock multiplier PLL is used to generate a system clock from an external 27-MHz crystal (fundamental resonant frequency) or external clock reference input. A crystal can be connected across terminals 99 (XTAL_IN) and 101 (XTAL_OUT), or a 1.8-V external clock input can be connected to terminal 99. Four horizontal PLLs generate the line-locked sample clock for each video decoder core from the system clock. Four color PLLs generate the color subcarrier frequency for each video decoder core from the corresponding line-locked clock. Four vertical PLLs generate the field/frame sync for each video decoder core. A frequency synthesizer generates the 32.768-MHz audio oversampling clock for each analog audio input from the system clock.
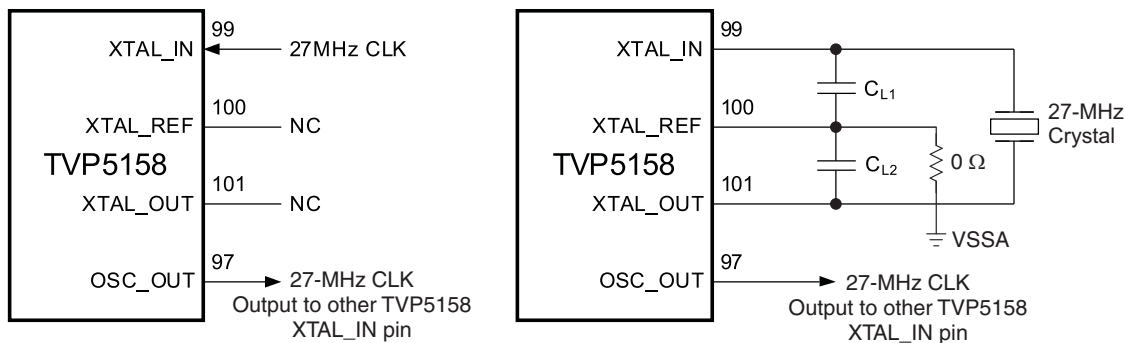
Figure 3-19. Clock and Crystal Connectivity

3.12 Reset Mode

Terminals 3 (RESETB) is active low signal to hold the decoder into reset. Table 3-18 shows the configuration of reset mode. Table 3-19 describes the status of the decoder signals during and immediately after reset. Figure 3-20 shows the reset timing.

After power-up, the device will be in an unknown state until properly reset. An active low reset, Reset B, of greater than or equal to 20 ms is required following active and stable supply ramp-up. To avoid potential I^2C issues, keep SCL and SDA inactive (high) for at least 260 µs after reset goes high. There are no power sequencing requirements except that all power supplies should become active and stable within 500 ms of each other.

Table 3-18. Reset Mode

RESETB	CONFIGURATION
0	Resets the decoder
1	Normal operation

Table 3-19. Reset Sequence

SIGNAL NAME	DURING RESET	RESET COMPLETED
DVO_A_[7:0], DVO_B_[7:0], DVO_C_[7:0], DVO_D_[7:0], OCLK_P, OCLK_N, INTREQ, I2CA[2:0], BCLK_R, LRCLK_R, SD_R, SD_M, SD_CO	Input	High-impedance
RESETB, SDA, SCL, LRCLK_CI, BCLK_CI, SD_CI, XTAL_IN	Input	Input
XTAL_OUT, OSC_OUT	Output	Output
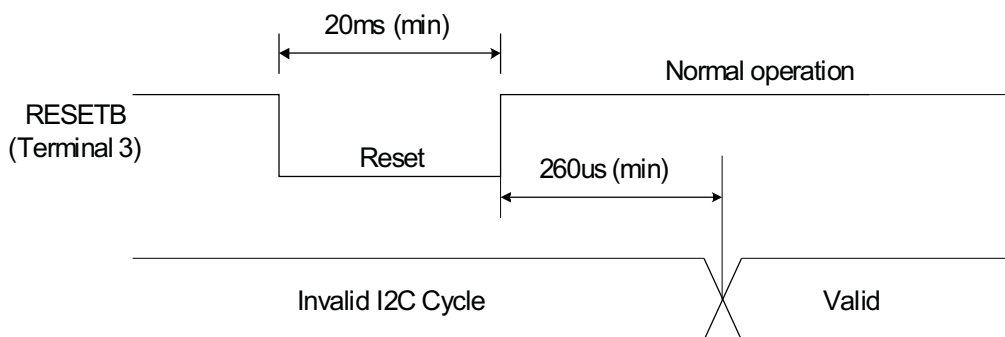
Figure 3-20. Reset Timing

4   Internal Control Registers

4.1   Overview

The decoder is initialized and controlled by a set of internal registers which set all device operating parameters. Communication between the external controller and the decoder is through I^2C. Table 4-1 shows the summary of these registers. The reserved registers must not be written. Reserved bits in the defined registers must be written with 0s, unless otherwise noted. The detailed programming information of each register is described in the following sections.

I^2C register FEh controls which of the four decoders will receive I^2C commands. I^2C register FFh controls which decoder core responds to I^2C reads. Note, for a read operation it is necessary to perform a write first in order to set the desired sub-address for reading.

Compared to previous video decoder, TVP5154A, the TVP5156, TVP5157, and TVP5158 add decoder auto increment and address auto increment bits control. If decoder auto increment bit is set, the next read/write is from/to the next decoder that is enabled. If address auto increment bit is set, the address will increment after all the decoders enabled read/writes are completed. The detail of I^2C registers FEh and FFh is shown in their register section.

Table 4-1. Registers Summary

REGISTER NAME	I^2C SUBADDRESS	DEFAULT	R/W [(1)]
Status 1	00h		R
Status 2	01h		R
Color Subcarrier Phase Status	02h		R
Reserved	03h		
ROM Version	04h		R
Reserved	05h - 07h		
Chip ID MSB	08h	51h	R
Chip ID LSB	09h	58h	R
Reserved	0Ah - 0Bh		
Video Standard Status	0Ch		R
Video Standard Select	0Dh	00h	R/W
CVBS Autoswitch Mask	0Eh	03h	R/W
Auto Contrast Mode	0Fh	03h	R/W
Luminance Brightness	10h	80h	R/W
Luminance Contrast	11h	80h	R/W
Reserved	12h	00h	R/W
Chrominance Saturation	13h	80h	R/W
Chrominance Hue	14h	00h	R/W
Reserved	15h		
Color Killer	16h	10h	R/W
Reserved	17h		
Luminance Processing Control 1	18h	40h	R/W
Luminance Processing Control 2	19h	00h	R/W
Power Control	1Ah	00h	R/W
Chrominance Processing Control 1	1Bh	00h	R/W
Chrominance Processing Control 2	1Ch	0Ch	R/W
Reserved	1Dh - 1Fh		
AGC Gain Status 1	20h		R
AGC Gain Status 2	21h		R

(1)   R = Read only, W = Write only, R/W = Read and write

Table 4-1. Registers Summary (continued)

REGISTER NAME	I²C SUBADDRESS	DEFAULT	R/W [1]
Reserved	22h		
Back-End AGC Status	23h		R
Status Request	24h	00h	R/W
AFE Gain Control	25h	F5h	R/W
Luma ALC Freeze Upper Threshold	26h	00h	R/W
Chroma ALC Freeze Upper Threshold	27h	00h	R/W
Reserved	28h		
AGC Increment Speed	29h	06h	R/W
AGC Increment Delay	2Ah	1Eh	R/W
AGC Decrement Speed	2Bh	04h	R/W
AGC Decrement Delay	2Ch	00h	R/W
AGC White Peak Processing	2Dh	F2h	R/W
Back-End AGC Control	2Eh	08h	R/W
Reserved	2Fh - 33h		
AFE Fine Gain	34h - 35h	086Ah	R/W
Reserved	36h - 47h		
AVID Start Pixel LSBs	48h	7Ah/84h	R/W
AVID Start Pixel MSBs	49h	00h/00h	R/W
AVID Pixel Width	4Ah - 4Bh	02D0h/02D0h	R/W
Reserved	4Ch - 5Bh		
NR_Max_Noise	5Ch	28h	R/W
NR_Control	5Dh	09h	R/W
NR_Noise_Filter	5Eh - 5Fh	0330h	R/W
Operation Mode Control	60h	00h	R/W
Color PLL Speed Control	61h	09h	R/W
Reserved	62h - 7Bh		
Sync Height Low Threshold	7Ch	02h	R/W
Sync Height High Threshold	7Dh	08h	R/W
Reserved	7Eh - 80h	03h	R/W
Clear Lost Lock Detect	81h	00h	R/W
Reserved	82h - 84h		
V-Sync Filter Shift	85h	03h	R/W
Reserved	86h		
656 Version/F Bit Control	87h	00h	R/W
F- and V-Bit Decode Control	88h	00h	R/W
F- and V-Bit Control	89h	16h	R/W
Reserved	8Ah - 8Bh		
Output Timing Delay	8Ch	00h	R/W
Reserved	8Dh - 8Fh		
Auto Contrast User Table Index	8Fh	04h	R/W
Blue Screen Y Control	90h	10h	R/W
Blue Screen Cb Control	91h	80h	R/W
Blue Screen Cr Control	92h	80h	R/W
Blue Screen LSB Control	93h	00h	R/W
Noise Measurement LSB	94h		R
Noise Measurement MSB	95h		R
Weak Signal High Threshold	96h	60h	R/W

Table 4-1. Registers Summary (continued)

REGISTER NAME	I²C SUBADDRESS	DEFAULT	R/W [1]
Weak Signal Low Threshold	97h	50h	R/W
Reserved	98h - 9Dh		
NR_Y_T0	9Eh	0Ah	R/W
NR_U_T0	9Fh	BCh	R/W
NR_V_T0	A0h	BCh	R/W
Reserved	A1h		
Vertical Line Count Status	A2h - A3h		R
Reserved	A4h - A7H		
Output Formatter Control 1 (write to all four decoder cores)	A8h	44h	R/W
Output Formatter Control 2 (write to all four decoder cores)	A9h	40h	R/W
Reserved	AAh - ADh		
Embedded Sync Offset Control 1 (write to all four decoder cores)	AEh	00h	R/W
Embedded Sync Offset Control 2 (write to all four decoder cores)	AFh	00h	R/W
AVD Output Control 1	B0h	00h	R/W
AVD Output Control 2	B1h	10h	R/W
OFM Mode Control	B2h	20h	R/W
OFM Channel Select 1	B3h	E4h	R/W
OFM Channel Select 2	B4h	E4h	R/W
OFM Channel Select 3	B5h	00h	R/W
OFM Super-Frame Size LSBs	B6h	1Bh	R/W
OFM Super-Frame Size MSBs	B7h	04h	R/W
OFM H-Blank Duration LSBs	B8h	40h	R/W
OFM H-Blank Duration MSBs	B9h	00h	R/W
Misc Ofm Control	BAh	00h	R/W
Reserved	BBh - BFh	00h	R/W
Audio Sample Rate Control	C0h	00h	R/W
Analog Audio Gain Control 1	C1h	88h	R/W
Analog Audio Gain Control 2	C2h	88h	R/W
Audio Mode Control	C3h	C9h	R/W
Audio Mixer Select	C4h	01h	R/W
Audio Mute Control	C5h	00h	R/W
Audio Mixing Ratio Control 1	C6h	00h	R/W
Audio Mixing Ratio Control 2	C7h	00h	R/W
Audio Cascade Mode Control	C8h	00h	R/W
Reserved	C9h	A5h	R/W
Reserved	CAh	FFh	R/W
Reserved	CBh	7Eh	R/W
Reserved	CCh	01h	R/W
Reserved	CDh - F1h		
Interrupt Status	F2h		R
Reserved	F3h		
Interrupt Mask	F4h	00h	R/W
Reserved	F5h		
Interrupt Clear	F6h	00h	R/W
Decoder Write Enable	FEh	0Fh	R/W
Decoder Read Enable	FFh	01h	R/W

Internal Control Registers   41

4.2 Register Definitions

Table 4-2. Status 1

Subaddress   00h
Default   Read only

7	6	5	4	3	2	1	0
Reserved	Line-alternating status	Field rate status	Lost lock detect	Color subcarrier lock status	Vertical sync lock status	Horizontal sync lock status	TV/VCR status

Line-alternating status

    0   Non line alternating
    1   Line alternating

Field rate status

    0   60 Hz
    1   50 Hz

Lost lock detect

    0   No lost lock since this bit was last cleared
    1   Lost lock since this bit was last cleared

Color subcarrier lock status

    0   Color subcarrier is not locked
    1   Color subcarrier is locked

Vertical sync lock status

    0   Vertical sync is not locked
    1   Vertical sync is locked

Horizontal sync lock status

    0   Horizontal sync is not locked
    1   Horizontal sync is locked

TV/VCR status

    0   TV
    1   VCR

Table 4-3. Status 2

Subaddress   01h
Default   Read only

7	6	5	4	3	2	1	0
Signal present	Weak signal detection	PAL switch polarity	Field sequence status	Color killed	Macrovision detection [2:0]		

Signal present
        0   Signal is not present
        1   Signal is present
Weak signal detection
        0   No weak signal
        1   Weak signal mode
PAL switch polarity
        0   PAL switch is zero
        1   PAL switch is one
Field sequence status
        0   Even field
        1   Odd field
Color killed
        0   Color killer is not active
        1   Color killer is active
Macrovision detection [2:0]
        000   No copy protection
        001   AGC pulses/pseudo syncs present (Type 1)
        010   2-line colorstripe only present
        011   AGC pulses/pseudo syncs and 2-line colorstripe present (Type 2)
        100   Reserved
        101   Reserved
        110   4-line colorstripe only present
        111   AGC pulses/pseudo syncs and 4-line colorstripe present (Type 3)

Table 4-4. Color Subcarrier Phase Status

Subaddress   02h
Default   Read only

7	6	5	4	3	2	1	0
Color subcarrier phase [7:0]							

This register shows the color subcarrier phase.

Table 4-5. ROM Version

Subaddress   04h
Default   Read only

7	6	5	4	3	2	1	0
ROM version [7:0]							

ROM Version [7:0]
        ROM revision number = 02h for PG 1.1

Table 4-6. Chip ID MSB

Subaddress 08h
Default Read only

7	6	5	4	3	2	1	0
Chip ID MSB [7:0]							

Chip ID MSB[7:0]

    This register identifies the MSB of device ID. Value = 51h

Table 4-7. Chip ID LSB

Subaddress 09h
Default Read only

7	6	5	4	3	2	1	0
Chip ID LSB [7:0]							

Chip ID LSB [7:0]

    This register identifies the LSB of device ID. Value = 58h

Table 4-8. Video Standard Status

Subaddress 0Ch
Default Read only

7	6	5	4	3	2	1	0
Autoswitch	Reserved				Video standard [2:0]		

This register contains information about the detected video standard that the device is currently operating. When in autoswitch mode, this register can be tested to determine which video standard as has been detected. See subaddress: 0Dh.

Autoswitch Mode

    0   Single standard set
    1   Autoswitch mode enabled

Video Standard [2:0]

    00h   Reserved
    01h   (M, J) NTSC
    02h   (B, D, G, H, I, N) PAL
    03h   (M) PAL
    04h   (Combination-N) PAL
    05h   NTSC 4.43
    06h   Reserved
    07h   PAL 60

Table 4-9. Video Standard Select

Subaddress   0Dh
Default   00h

7	6	5	4	3	2	1	0
Reserved					CVBS Standard [2:0]		

The user can force the device to operate in a particular video standard mode by writing the appropriate value into this register. Changing these bits will cause some register settings to be reset to their defaults. See subaddress: 0Ch.

CVBS Standard [2:0]

00h	CVBS Autoswitch mode (default)
01h	(M, J) NTSC
02h	(B, D, G, H, I, N) PAL
03h	(M) PAL
04h	(Combination-N) PAL
05h	NTSC 4.43
06h	Reserved
07h	PAL 60

Table 4-10. CVBS Autoswitch Mask

Subaddress   0Eh
Default   03h

7	6	5	4	3	2	1	0
Reserved	PAL 60	Reserved	NTSC 4.43	(Nc) PAL	(M) PAL	PAL	(M, J) NTSC

Autoswitch mode mask

Limits the video formats between which autoswitch is possible.

PAL 60	0	Autoswitch does not include PAL 60 (default)
	1	Autoswitch includes PAL 60
NTSC 4.43	0	Autoswitch does not include NTSC 4.43 (default)
	1	Autoswitch includes NTSC 4.43
(Nc) PAL	0	Autoswitch does not include (Nc) PAL (default)
	1	Autoswitch includes (Nc) PAL
(M) PAL	0	Autoswitch does not include (M) PAL (default)
	1	Autoswitch includes (M) PAL
PAL	0	Reserved
	1	Autoswitch includes (B, D, G, H, I, N) PAL (default)
(M, J) NTSC	0	Reserved
	1	Autoswitch includes (M, J) NTSC (default)

Table 4-11. Auto Contrast Mode

Subaddress   0Fh
Default   03h

7	6	5	4	3	2	1	0
Reserved						Auto Contrast Mode [1:0]	

Auto Contrast Mode [1:0]

00h	Enabled
01h	Reserved
02h	User Mode
03h	Disabled (default)

Table 4-12. Luminance Brightness

| **Subaddress** | 10h |
| **Default** | 80h |

7	6	5	4	3	2	1	0
Brightness [7:0]							

Brightness [7:0]

 This register works for the luminance.

 0000 0000 0 (dark)

 1000 0000 128 (default)

 1111 1111 255 (bright)

Table 4-13. Luminance Contrast

| **Subaddress** | 11h |
| **Default** | 80h |

7	6	5	4	3	2	1	0
Contrast [7:0]							

Contrast [7:0]

 This register works for the luminance.

 0000 0000 0 (minimum contrast)

 1000 0000 128 (default)

 1111 1111 255 (maximum contrast)

Table 4-14. Chrominance Saturation

| **Subaddress** | 13h |
| **Default** | 80h |

7	6	5	4	3	2	1	0
Saturation [7:0]							

Saturation [7:0]

 This register works for the chrominance.

 0000 0000 0 (no color)

 1000 0000 128 (default)

 1111 1111 255 (maximum)

Table 4-15. Chrominance Hue

| **Subaddress** | 14h |
| **Default** | 80h |

7	6	5	4	3	2	1	0
Hue [7:0]							

Saturation [7:0]

 This register works for the chrominance.

 0000 0000 -180°

 1000 0000 0° (default)

 1111 1111 +180°

Table 4-16. Color Killer

| **Subaddress** | 16h |
| **Default** | 10h |

7	6	5	4	3	2	1	0
Reserved	Automatic color killer		Color killer threshold [4:0]				

Automatic color killer

00	Automatic mode (default)
01	Reserved
10	Color killer enabled, The UV terminals are forced to a zero color state.
11	Color killer disabled

Color killer threshold [4:0]

0 0000	0 (minimum)
1 0000	16 (default)
1 1111	31 (maximum)

Table 4-17. Luminance Processing Control 1

| **Subaddress** | 18h |
| **Default** | 40h |

7	6	5	4	3	2	1	0
NTSC_Ped	Reserved				Luminance signal delay [2:0]		

NTSC_Ped

Specifies whether NTSC composite video inputs are compliant with NTSC-M or NTSC-J.

| 0 | NTSC-M (714/286 ratio, w/ pedestal) - default |
| 1 | NTSC-J (714/286 ratio, w/o pedestal) |

Luminance signal delay [2:0]

Luminance signal delays respect to chroma signal in 1x pixel clock increments.

011	3 pixel clocks delay
010	2 pixel clocks delay
001	1 pixel clocks delay
000	0 pixel clocks delay (default)
111	-1 pixel clocks delay
110	-2 pixel clocks delay
101	-3 pixel clocks delay
100	0 pixel clocks delay

Table 4-18. Luminance Processing Control 2

Subaddress   19h
Default   00h

7	6	5	4	3	2	1	0
Luma filter select [1:0]		Reserved		Peaking gain [1:0]		Reserved	

Luma filter selected [1:0]

    00   Luminance adaptive comb enable (default)

    01   Luminance adaptive comb disable (trap filter selected)

    10   Luma comb/trap filter bypassed

    11   Reserved

Peaking gain [1:0]

    00   0 (default)

    01   0.5

    10   1

    11   2

Table 4-19. Power Control

Subaddress   1Ah
Default   00h

7	6	5	4	3	2	1	0
Pwd_ach4	Pwd_ach3	Pwd_ach2	Pwd_ach1	Pwd_vpll	Pwd_ref	Pwd_ofm_clk	Pwd_video

Pwd_ach4

  Power down audio channel 4, active high

  0   Normal operation (default)

  1   Audio channel 4 power down

Pwd_ach3

  Power down audio channel 3, active high

  0   Normal operation (default)

  1   Audio channel 3 power down

Pwd_ach2

  Power down audio channel 2, active high

  0   Normal operation (default)

  1   Audio channel 2 power down

Pwd_ach1

  Power down audio channel 1, active high

  0   Normal operation (default)

  1   Audio channel 1 power down

Pwd_vpll

  Power down video PLL, active high

  0   Normal operation (default)

  1   Video PLL power down

Pwd_ref

  Power down bandgap reference, active high

  0   Normal operation (default)

  1   Bandgap reference power down

Pwd_ofm_clk

  Power down OFM clock, active high

  0   Normal operation (default)

  1   OFM clock power down

Pwd_video

  Power down video channel corresponding to current decoder core, active high

  0   Normal operation (default)

  1   Power down video channel corresponding to current decoder core

Table 4-20. Chrominance Processing Control 1

Subaddress 1Bh
Default 00h

7	6	5	4	3	2	1	0
Reserved	TBC		Color PLL reset	Chroma adaptive comb enable	Reserved	Automatic color gain control [1:0]	

TBC

Line based time correction corrects for horizontal phase errors encountered during video decoding up to ±80 pixels of error. TBC does not require external memory.

00 Disabled (default)

01 Enabled

10 Automatic selection. On when TV/VCR = VCR, off when TV/VCR = TV.

11 Automatic selection. On when TV/VCR = VCR, off when TV/VCR = TV.

Color PLL reset

0 Color subcarrier PLL not reset (default)

1 Color subcarrier PLL reset

Chrominance adaptive comb enable

This bit is effective on composite video only.

0 Enabled (default)

1 Disabled

Automatic color gain control (ACGC) [1:0]

00 ACGC enabled (default)

01 Reserved

10 ACGC disabled, ACGC set to the nominal value

11 ACGC frozen to the previously set value

Table 4-21. Chrominance Processing Control 2

Subaddress 1Ch
Default 0Ch

7	6	5	4	3	2	1	0
Reserved				PAL compensation	WCF	Chrominance filter select [1:0]	

PAL compensation

This bit is not effective to NTSC mode.

0 Disabled

1 Enabled (default)

Wideband chroma LPF filter (WCF)

0 Disabled

1 Enabled (default)

Chrominance filter select [1:0]

This register trades chroma bandwidth for less false color.

00 Disabled (default)

01 Notch 1

10 Notch 2

11 Notch 3

Table 4-22. AGC Gain Status

Subaddress   20h-21h
Default   Read Only

Subaddress	7	6	5	4	3	2	1	0
20h				Fine Gain [7:0]				
21h		Reserved			Fine Gain [13:8]			

These AGC gain status registers are updated automatically when the AGC is enabled; in manual gain control mode these register values are not updated.

Since this register is a multi byte register it is necessary to "capture" the setting into the register to ensure that the value is not updated between reading the lower and upper bytes. In order to cause this register to "capture" the current settings bit 0 of I^{2}C register 24h (Status Request) should be set to a 1. Once the internal processor has updated this register bit 0 of register 24h will be cleared, indicating that both bytes of the AGC gain status register have been updated and can be read. Either byte may be read first since no further update will occur until bit 0 of 24h is set to 1 again.

Table 4-23. Back-End AGC Status

Subaddress   23h
Default   Read Only

7	6	5	4	3	2	1	0
			Gain [7:0]				

Current back-end AGC ratio = Gain/128.

Table 4-24. Status Request

Subaddress   24h
Default   00h

7	6	5	4	3	2	1	0
			Reserved				Capture

Capture

  Setting a 1 in this register causes the inter processor to capture the current settings of the AGC status, noise measurement, and the vertical line count registers. Since this capture is not immediate it is necessary to check for completion of the capture by reading the "capture" bit repeatedly after setting it and waiting for it to be cleared by the internal processor. Once the "capture" bit is 0 the AGC status, noise measurement and vertical line counters (20h/21h, 94h/95h and A2h/A3h) will have been updated, and can be safely read in any order.

Table 4-25. AFE Gain Control

Subaddress   25h
Default   F5h

7	6	5	4	3	2	1	0
			Reserved		ALC	Reserved	AGC

Reserved

  For future compatibility, all reserved bits must be set to logic 1.

ALC

  Active-high automatic level control (ALC) enable

  0   ALC disabled (manual level control)

  1   ALC enabled (default)

AGC

  Active-high automatic gain control (AGC) enable

  0   AGC disabled (manual gain control)

  1   AGC enabled (default)

Table 4-26. Luma ALC Freeze Upper Threshold

Subaddress	26h
Default	00h

7	6	5	4	3	2	1	0
Luma ALC freeze [7:0]							

Upper hysteresis threshold for luma ALC freeze function. The lower hysteresis threshold for the ALC freeze function is fixed at 1 count out of 4096. Setting the upper threshold to 00h (default condition) disables the ALC freeze function.

Table 4-27. Chroma ALC Freeze Upper Threshold

Subaddress	27h
Default	00h

7	6	5	4	3	2	1	0
Chroma ALC freeze [7:0]							

Upper hysteresis threshold for chroma ALC freeze function. The lower hysteresis threshold for the ALC freeze function is fixed at 1 count out of 4096. Setting the upper threshold to 00h (default condition) disables the ALC freeze function. Recommend a setting of 02h or greater when enabled.

Table 4-28. AGC Increment Speed

Subaddress	29h
Default	06h

7	6	5	4	3	2	1	0
Reserved					AGC increment speed [3:0]		

AGC increment speed

    Controls the filter coefficient of the first-order, recursive automatic gain control (AGC) algorithm whenever incrementing the gain.

    000   0 (fastest)

    110   6 (default)

    111   7 (slowest)

Table 4-29. AGC Increment Delay

Subaddress	2Ah
Default	1Eh

7	6	5	4	3	2	1	0
AGC increment delay [7:0]							

AGC increment delay [7:0]

    Number of frames to delay gain increments. Also see AGC decrement delay at subaddress 2Ch.

    00000000   0

    00011110   30 frames (default)

    11111111   255 frames

Table 4-30. AGC Decrement Speed

Subaddress   2Bh
Default   04h

7	6	5	4	3	2	1	0
Reserved					AGC decrement speed [2:0]		

AGC decrement speed

> Controls the filter coefficient of the first-order recursive automatic gain control (AGC) algorithm when decrementing the gain.
> NOTE: This register affects the decrement speed only when the amplitude reference used by the AGC is either the composite peak or the luma peak.
> Also see AGC increment speed at subaddress 29h.
>
> 111   7 (slowest)
>
> 110   6 (default)
>
> 000   0 (fastest)

Table 4-31. AGC Decrement Delay

Subaddress   2Ch
Default   00h

7	6	5	4	3	2	1	0
AGC decrement delay [7:0]							

AGC decrement delay [7:0]

> Number of frames to delay gain decrements.
> NOTE: This register affects the decrement delay only when the amplitude reference used by the AGC is either the composite peak or the luma peak.
> Also see AGC increment delay at subaddress 2Ah.
>
> 111   0
>
> 110   30 (default)
>
> 000   255

Table 4-32. AGC White Peak Processing

Subaddress	2Dh
Default	F2h

7	6	5	4	3	2	1	0
Luma peak A	Reserved	Color burst A	Sync height A	Luma peak B	Composite peak	Color burst B	Sync height B

If all four bits of the lower nibble are set to logic 1 (that is, no amplitude reference selected), then the front-end analog and digital gains are automatically set to nominal values.

If all four bits of the upper nibble are set to logic 1 (that is, no amplitude reference selected), then the back-end gain is set automatically to unity. If the input sync height is greater than 100% and the AGC-adjusted output video amplitude becomes less than 100%, then the back-end scale factor attempts to increase the contrast in the back-end to restore the video amplitude to 100%.

Luma peak A

    Use of the luma peak as a video amplitude reference for the back-end feed-forward type AGC algorithm

    0   Enabled (default)

    1   Disabled

Color burst A

    Use of the color burst amplitude as a video amplitude reference for the back-end

    0   Enabled (default)

    1   Disabled

Sync height A

    Use of the sync-height as a video amplitude reference for the back-end feed-forward type AGC algorithm

    0   Enabled (default)

    1   Disabled

Luma peak B

    Use of the luma peak as a video amplitude reference for front-end feedback type AGC algorithm

    0   Enabled (default)

    1   Disabled

Composite peak

    Use of the composite peak as a video amplitude reference for front-end feedback type AGC algorithm

    0   Enabled (default)

    1   Disabled

Color burst B

    Use of the color burst amplitude as a video amplitude reference for front-end feedback type AGC algorithm

    0   Enabled (default)

    1   Disabled

Sync height B

    Use of the sync-height as a video amplitude reference for front-end feedback type AGC algorithm

    0   Enabled (default)

    1   Disabled

Table 4-33. Back-End AGC Control

Subaddress   2Eh
Default   08h

7	6	5	4	3	2	1	0
Reserved				1	Peak	Color	Sync

This register allows disabling the back-end AGC when the front-end AGC uses specific amplitude references (sync-height, color burst or composite peak) to decrement the front-end gain. For example, writing 09h to this register disables the back-end AGC whenever the front-end AGC uses the sync-height to decrement the front-end gain.

Peak

     Disables back-end AGC when the front-end AGC uses the composite peak as an amplitude reference.

     0   Enabled (default)

     1   Disabled

Color

     Disables back-end AGC when the front-end AGC uses the color burst as an amplitude reference.

     0   Enabled (default)

     1   Disabled

Sync

     Disables back-end AGC when the front-end AGC uses the sync height as an amplitude reference.

     0   Enabled (default)

     1   Disabled

Table 4-34. AFE Fine Gain

Subaddress   34h-35h
Default   086Ah

Subaddress	7	6	5	4	3	2	1	0
34h	FGAIN [7:0]							
35h	Reserved		FGAIN [13:8]					

FGAIN [13:0]

     This fine gain applies to CVBS. Fine Gain = $(1/2048) \times$ FGAIN where $0 \leq$ FGAIN ≤ 16383. This register works only in manual gain control mode. When AGC is active, writing to any value is ignored.

00 0000 0000 0000 to 00 0011 1111 1111	Reserved
00 0100 0000 0000	0.5
00 1000 0000 0000	1
00 1000 0110 1010	1.052 (default)
00 1100 0000 0000	1.5
11 1111 1111 1111	7.9995

Table 4-35. AVID Start Pixel

Subaddress   48h-49h
Default   007Ah/0084h

Subaddress	7	6	5	4	3	2	1	0
48h	AVID start [7:0]							
49h	Reserved			AVID active	Reserved		AVID start [9:8]	

AVID start [9:0]

   AVID start pixel number, this is a absolute pixel location from HS start pixel 0.

   The TVP5158 updates the AVID start only when the AVID start MSB byte is written to. AVID start pixel register also controls the position of SAV code. If these registers are modified, then the TVP5158 will retain the values for each video standard until the device is reset. The values for a particular video standard should be set by forcing the TVP5158 to the desired video standard first using register 0Dh then setting this register. This should be repeated for each video standard where the default values need to be changed.

AVID active

   0   AVID out active in VBLK (default)

   1   AVID out inactive in VBLK

Table 4-36. AVID Pixel Width

Subaddress   4Ah-4Bh
Default   02D0h

Subaddress	7	6	5	4	3	2	1	0
4Ah	AVID Width [7:0]							
4Bh	Reserved						AVID Width [9:8]	

AVID Width [9:0]

   AVID pixel width. The number of pixels width of active video must be an even number. This is an absolute pixel location from HS start pixel 0.

   The TVP5158 updates the AVID pixel width only when the AVID pixel width MSB byte is written to. AVID pixel width register also controls the position of EAV code. If these registers are modified, then the TVP5158 will retain the values for each video standard until the device is reset. The values for a particular video standard should be set by forcing the TVP5158 to the desired video standard first using register 0Dh then setting this register. This should be repeated for each video standard where the default values need to be changed.

Table 4-37. Noise Reduction Max Noise

Subaddress   5Ch
Default   28h

7	6	5	4	3	2	1	0
Reserved	NR_Max_Noise [6:0]						

NR_Max_Noise [6:0]

   User-defined maximum noise level

   0010 1000   40 (default)

Table 4-38. Noise Reduction Control

Subaddress   5Dh
Default   09h

7	6	5	4	3	2	1	0
Reserved			NR_Color_ Killer_En	Block_Width_ UV	Block_Width_Y	Test_ Bypass	NR_ Bypass

NR_Color_Killer_En

    Noise reduction color killer enabled

    0   Disabled (default)

    1   Enabled

Block_Width_UV

    Number of UV pixel values which the algorithm will use to generate the noise average.

    0   128 pixels

    1   256 pixels (default)

Block_Width_Y

    Number of Y pixel values which the algorithm will use to generate the noise average.

    0   256 pixels (default)

    1   512 pixels

Test_Bypass

    Test mode bypass. This test bypass mode bypasses the Noise Reduction module completely via hard wires and has zero delay for processing.

    0   Bypass disabled (default)

    1   Bypass enabled

NR_Bypass

    Noise reduction module bypass. The noise reduction module has a bypass capability which enables it to pass through the incoming data during the output active video period, while matching the delay in operation mode.

    0   Bypass disabled

    1   Bypass enabled (default)

Table 4-39. Noise Reduction Noise Filter Beta

Subaddress   5Eh-5Fh
Default   0330h

Subaddress	7	6	5	4	3	2	1	0
5Eh	NR_NoiseFilter [7:0]							
5Fh	Reserved						NR_NoiseFilter [9:8]	

NR_NoiseFilter [9:0]

    Noise reduction noise filter setting

    0000 0011 0011 0000   816 (default)

Table 4-40. Operation Mode Control

Subaddress   60h
Default   00h

7	6	5	4	3	2	1	0
Reserved		TV/VCR mode		Reserved	Freeze CPLL	Mode_CTL [1:0]	

TV/VCR mode

When in TV mode the horizontal PLL responds slower, improving noise immunity and producing a more stable line frequency, hence more stable output image.

When in VCR mode the PLL responds more quickly in order to be able to respond to larger variations in the horizontal timing of the video signal, reducing tearing, particularly at VCR head switching intervals.

When in automatic mode the horizontal phase error is used to automatically determine if the input signal is behaving like a TV type signal, or a VCR type signal, configuring the horizontal PLL accordingly.

00   Automatic detection (default)

01   Reserved

10   Force VCR mode

11   Force TV mode

Freeze CPLL

0   Normal operation (default)

1   Freeze color PLL

Mode_CTL [1:0]

Stable Vsync output when no input.

00   Disabled (default)

01   Force Stable Vsync out

10   Automatic

11   Reserved

Table 4-41. Color PLL Speed Control

Subaddress   61h
Default   09h

7	6	5	4	3	2	1	0
Reserved				CPLL speed [3:0]			

CPLL speed [3:0]

Color PLL speed control

0000
to   Reserved
1000

1001   9: Faster (default)

1010   10

1011   11: Slower

1100
to   Reserved
1111

Table 4-42. Sync Height Low Threshold

Subaddress   7Ch
Default   02h

7	6	5	4	3	2	1	0
VSync upper thres [7:0]							

Lower hysteresis threshold for vertical sync-height detection (value/32×target sync height).

Table 4-43. Sync Height High Threshold

| **Subaddress** | 7Dh |
| **Default** | 08h |

7	6	5	4	3	2	1	0
VSync upper thres [7:0]							

Upper hysteresis threshold for vertical sync-height detection (value/32×target sync height).

Table 4-44. Clear Lost Lock Detect

| **Subaddress** | 81h |
| **Default** | 00h |

7	6	5	4	3	2	1	0
Reserved							Clear lost lock detect

Clear lost lock detect

      Clear bit 4 (lost lock detect) in the status 1 register at subaddress 00h

      0   No effect (default)

      1   Clears bit 4 in the status 1 register (00h)

Table 4-45. VSYNC Filter Shift

| **Subaddress** | 85h |
| **Default** | 03h |

7	6	5	4	3	2	1	0
Reserved						VSYNC filter shift [1:0]	

VSYNC filter shift [1:0]

      Used for adaptation of VPLL time constant

      00   0 (fast)

      01   1

      10   2

      11   3 (slow)

Table 4-46. 656 Version/F-bit Control

| **Subaddress** | 87h |
| **Default** | 00h |

7	6	5	4	3	2	1	0
Reserved						656 version	F-control

656 version

      0   Timing confirms to ITU-R BT.656-4 specifications (default)

      1   Timing confirms to ITU-R BT.656-3 specifications

F-control

      0   Odd field causes 0 → 1 transition in F-bit when in TVP5146 F/V mode (see register 88h)

      1   Even field causes 0 → 1 transition in F-bit when in TVP5146 F/V mode (see register 88h)

Table 4-47. F-Bit and V-Bit Decode Control

Subaddress   88h

Default   00h

7	6	5	4	3	2	1	0
Reserved			VPLL	Adaptive	Reserved	F-Mode [1:0]	

VPLL

    VPLL time constant control

    0   VPLL adapts time constants to input signal

    1   VPLL time constants fixed

Adaptive

    0   Enable F and V bit adaptation to detected lines per frame

    1   Disable F and V bit adaptation to detected lines per frame

F-Mode [1:0]

    F-bit control mode

    00   Auto: If lines per frame is standard decode F and V bits as per 656 standard from line count else decode F bit from VSYNC input and set V bit = 0

    01   Decode F and V from input syncs

    10   Reserved

    11   Always decode F and V bits from line count (TVP5146 compatible)

This register is used in conjunction with register 89h as shown:

Reg 88h		Reg 89h		Mode	Standard LPF		Non-standard LPF	
Bit 1	Bit 0	Bit 1	Bit 0		F	V	F	V
0	0	0	0	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	0	1	TVP5158	656	656	Toggle	Switch9
0	0	1	0	TVP5158	656	656	Pulse	0
0	0	1	1	Reserved	Reserved	Reserved	Reserved	Reserved
0	1	0	0	Reserved	Reserved	Reserved	Reserved	Reserved
0	1	0	1		656	656	Toggle	Switch9
0	1	1	0		656	656	Pulse	0
0	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved
1	0	0	0	Reserved	Reserved	Reserved	Reserved	Reserved
1	0	0	1	Reserved	Reserved	Reserved	Reserved	Reserved
1	0	1	0	Reserved	Reserved	Reserved	Reserved	Reserved
1	0	1	1	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	0	TVP5146	656	656	Even = 1 Odd = toggle	Switch
1	1	0	1	TVP5146	656	656	Toggle	Switch
1	1	1	0	TVP5146	656	656	Pulse	Switch
1	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved

656   ITU-R BT.656 standard

Toggle   Toggles from field to field

Pulse   Pulses low for 1 line prior to field transition

Switch   V bit switches high before the F bit transition and low after the F bit transition

Switch9   V bit switches high 1 line prior to F bit transition, then low after 9 lines

Reserved   Not used

Table 4-48. F-Bit and V-Bit Control

Subaddress   89h
Default   16h

7	6	5	4	3	2	1	0
Rabbit	Reserved		Fast lock	F and V [1:0]		Phase Det	HPLL

Rabbit

    Enable "rabbit ear"

    0   Disabled (default)

    1   Enabled

Fast lock

    Enable fast lock where vertical PLL is reset and a 2 sec timer is initialized when vertical lock is lost; during timeout the detected input VS is output.

    0   Disabled

    1   Enabled (default)

F and V [1:0]

    F and V control bits are only enabled for F-bit control mode 01 and 10 (see register 88h)

F and V	Lines Per Frame	F Bit	V Bit
00	Standard	ITU-R BT.656	ITU-R BT.656
	Non standard-even	Forced to 1	Switch at field boundary
	Non standard-odd	Toggles	Switch at field boundary
01 (default)	Standard	ITU-R BT.656	ITU-R BT.656
	Non standard	Toggles	Switch at field boundary
10	Standard	ITU-R BT.656	ITU-R BT.656
	Non standard	Pulsed mode	Switch at field boundary
11	Reserved		

Phase Det

    Enable integral-window phase detector

    0   Disabled

    1   Enabled (default)

HPLL

    Enable horizontal PLL to free run

    0   Disabled (default)

    1   Enabled

Table 4-49. Output Timing Delay

Subaddress   8Ch
Default   00h

7	6	5	4	3	2	1	0
Reserved	Output timing delay [6:0]						

Output timing delay [6:0]

    Adjusts delay for AVID start and stop.

    000 1111   +15 pixel delay

    000 0001   +1 pixel delay

    000 0000   0 pixel delay (default)

    111 1111   -1 pixel delay

    111 0000   -16 pixel delay

Table 4-50. Auto Contrast User Table Index

Subaddress	8Fh
Default	04h

7	6	5	4	3	2	1	0
Reserved	AC_User_Mode_Table [2:0]			Reserved			

AC_User_Mode_Table [2:0]

    User table selection for auto contrast user mode when the register 0Fh sets to 02h.

000	Brighter 1
001	Brighter 2
010	Brighter 3 (Brightest)
011	Darker 1
100	Darker 2
101	Darker 3 (Darkest)
110 to 111	Reserved

Table 4-51. Blue Screen Y Control

Subaddress	90h
Default	10h

7	6	5	4	3	2	1	0
Y value [9:2]							

The Y value of the color screen output when enabled by bit 2 or 3 of the output formatter 2 register is programmable using a 10-bit value. The 8 MSBs, bits[9:2], are represented in this register. The remaining two LSB are found in the Blue screen LSB register. The default color screen output is black.

Table 4-52. Blue Screen Cb Control

Subaddress	91h
Default	80h

7	6	5	4	3	2	1	0
Cb value [9:2]							

The Cb value of the color screen output when enabled by bit 2 or 3 of the output formatter 2 register is programmable using a 10-bit value. The 8 MSBs, bits[9:2], are represented in this register. The remaining two LSB are found in the Blue screen LSB register. The default color screen output is black.

Table 4-53. Blue Screen Cr Control

Subaddress	92h
Default	80h

7	6	5	4	3	2	1	0
Cr value [9:2]							

The Cr value of the color screen output when enabled by bit 2 or 3 of the output formatter 2 register is programmable using a 10-bit value. The 8 MSBs, bits[9:2], are represented in this register. The remaining two LSB are found in the Blue Screen LSB register. The default color screen output is black.

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Table 4-54. Blue Screen LSB Control

Subaddress	93h
Default	00h

7	6	5	4	3	2	1	0
Reserved		Y value LSB [1:0]		Cb value LSB [1:0]		Cr value LSB [1:0]	

The two LSBs for the Blue screen Y, Cb, and Cr values are represented in this register.

Table 4-55. Noise Measurement

Subaddress	94h-95h
Default	Read Only

Subaddress	7	6	5	4	3	2	1	0
94h	Noise Measurement [7:0]							
95h	Noise Measurement [15:8]							

Noise measurement[15:0]

Used by the weak signal detection algorithm.

Since this register is a double byte register it is necessary to "capture" the setting into the register to ensure that the value is not updated between reading the lower and upper bytes. In order to cause this register to "capture" the current settings bit 0 of I^{2}C register 24h (status request) should be set to a 1. Once the internal processor has updated this register bit 0 of register 24h will be cleared, indicating that both bytes of the noise measurement register have been updated and can be read. Either byte may be read first since no further update will occur until bit 0 of 24h is set to 1 again.

Table 4-56. Weak Signal High Threshold

Subaddress	96h
Default	60h

7	6	5	4	3	2	1	0
Level [7:0]							

This register controls the upper threshold of the noise measurement used to determine whether the input signal should be considered a weak signal.

Table 4-57. Weak Signal Low Threshold

Subaddress	97h
Default	50h

7	6	5	4	3	2	1	0
Level [7:0]							

This register controls the lower threshold of the noise measurement used to determine whether the input signal should be considered a weak signal.

Table 4-58. Noise Reduction Y/U/V T0

Subaddress	9Eh	9Fh	A0h
Default	0Ah	BCh	BCh

Subaddress	7	6	5	4	3	2	1	0
9Eh	Noise Reduction Y T0 [7:0]							
9Fh	Noise Reduction U T0 [7:0]							
A0h	Noise Reduction V T0 [7:0]							

These registers control how much noise filtering is done for Y/U/V channels. The bigger the value is, the more noise filtering at the expense of video details.

Table 4-59. Vertical Line Count Status

Subaddress	A2h-A3h
Default	Read Only

Subaddress	7	6	5	4	3	2	1	0
A2h	Vertical line [7:0]							
A3h	Reserved						Vertical line [9:8]	

This status register is only updated when a status request is initiated via bit 0 of subaddress 24h.

Vertical line [9:0] represent the detected a total number of lines from the previous frame. This can be used with nonstandard video signals such as a VCR in trick mode to synchronize downstream video circuitry.

NOTE: This register is not double buffered.

Since this register is a double byte register it is necessary to "capture" the setting into the register to ensure that the value is not updated between reading the lower and upper bytes. In order to cause this register to "capture" the current settings bit 0 of I^{2}C register 24h (Status Request) should be set to a 1. Once the internal processor has updated this register bit 0 of register 24h will be cleared, indicating that both bytes of the vertical line count register have been updated and can be read. Either byte may be read first since no further update will occur until bit 0 of 24h is set to 1 again.

Table 4-60. Output Formatter Control 1

Subaddress	A8h
Default	44h

7	6	5	4	3	2	1	0
Reserved	YCbCr code range	CbCr range	Reserved				

This register writes to all four decoder cores.

YCbCr output code range

0	ITU-R BT.601 coding range (Y ranges from 64 to 940. Cb and Cr range from 64 to 960.)
1	Extended coding range (Y, Cb and Cr range from 4 to 1016.) (default)

CbCr range format

0	Offset binary code (2's complement + 512) (default)
1	Straight binary code (2's complement)

Table 4-61. Output Formatter Control 2

Subaddress   A9h
Default   40h

7	6	5	4	3	2	1	0
Reserved				Blue screen output [1:0]		Reserved	

This register writes to all four decoder cores.

Blue screen output [1:0] (internal use only)

> Fully programmable color of "blue screen" to support clean input/channel switching. When enabled, in case of lost lock, or when forced, the TVP5158 waits until the end of the current frame, then switches the output data to a programmable color. Once displaying the "blue screen", the inputs can be switched without causing snow or noise to be displayed on the digital output data. Once the inputs have settled the "blue screen" can be disabled, where the TVP5158 then waits until the end of the current video frame before re-enabling the video stream data to the output ports.

> 00   Normal operation (default)
> 01   Blue screen out when TVP5158 detects lost lock
> 10   Force Blue screen out
> 11   Reserved

Table 4-62. Embedded Sync Offset Control 1

Subaddress   AEh
Default   00h

7	6	5	4	3	2	1	0
Offset [7:0]							

Offset [7:0]

> This register allows the line position of the embedded F and V bit signals to be offset from the 656 standard positions. This register is only applicable to input video signals with standard number of lines.

> 01111111   +127 lines
> ⋮
> 00000001   +1 line
> 00000000   0 line
> 11111111   -1 line
> ⋮
> 10000000   -128 lines

Table 4-63. Embedded Sync Offset Control 2

Subaddress   AFh
Default   00h

7	6	5	4	3	2	1	0
Offset [7:0]							

Offset [7:0]

> This register allows the line relationship between the embedded F and V bit signals to be offset from the 656 standard positions, and moves F relative to V. This register is only applicable to input video signals with standard number of lines.

> 01111111   +127 lines
> ⋮
> 00000001   +1 line
> 00000000   0 line
> 11111111   -1 line
> ⋮
> 10000000   -128 lines

Table 4-64. AVD Output Control 1

Subaddress	B0h
Default	00h

7	6	5	4	3	2	1	0
Interleave_mode		Channel_Mux_Number		Output_ type	VCS_ID	Video_Res_Sel	

This register writes to all four decoder cores.

Interleave_mode

Interleave mode for multi-channel formats

00   Non-interleaved (a.k.a. 1-Ch mode) – (default)

01   Pixel-interleaved mode (2-Ch and 4-Ch only)

10   Line-interleaved mode

11   Line-interleaved, hybrid mode (adds 1-Ch D1 to selected 4-Ch Half-D1, 4-Ch CIF or 8-Ch CIF format)

Channel_Mux_Number

Number of time-multiplexed channels

00   1-Ch (reserved)

01   2-Ch

10   4-Ch (or 4-Ch Half-D1 or CIF + 1-Ch D1 for line-interleaved, hybrid mode)

   8-Ch cascade (format depends on VCS_ID, line-interleaved mode only)

   •   ✕ Line-interleaved mode
      –   1st stage: 8-Ch Half-D1 or 8-Ch CIF (video port A)

11   –   2nd stage: 4-Ch Half-D1 or 4-Ch CIF (video port A)

   •   ✕ Line-interleaved, hybrid mode
      –   1st stage: 8-Ch CIF + 1-Ch D1 (video port A)
      –   2nd stage: 4-Ch CIF (video port A) and 1-Ch D1 (video port B)

Output_type

Output interface type

0   8-bit ITU-R BT.656 interface (default)

1   16-bit ITU-R BT.601 interface (4-Ch D1 and 4-Ch Half-D1 line-interleaved modes only)

VCS_ID

Video cascade stage ID. Set to 0 for normal operation. For line-interleaved mode only.

0   1st stage (channels 1 to 4) (default)

1   2nd stage (channels 5 to 8)

Video_Res_Sel

Video resolution select. Effects multi-channel OFM only.

00   D1 (default)

01   Reserved

10   Half-D1

11   CIF

Table 4-65. AVD Output Control 2

Subaddress   B1h
Default   10h

7	6	5	4	3	2	1	0
LLC_En	Line_Crop_En	Quan_Ctrl		Line_ID_Ctrl	Chan_ID_SAVEAV_En	Chan_ID_Blank_En	Video_Det_SAVEAV_En

This register writes to all four decoder cores.

LLC_En

    Line-locked clock enable, active high. For non-interleaved mode only. For use with Port A only.

    0   Line-locked clock disabled (default)

    1   Line-locked clock enabled

Line_ Crop_En

    AVD line cropping enable, active high. Effects both scaled and unscaled AVD outputs.

    0   Cropping disabled (unscaled: 720 pixels/line, down-scaled: 360 pixels/line) – (default)

    1   Cropping enabled (unscaled: 704 pixels/line, down-scaled: 352 pixels/line)

Quan_Ctrl

    10-bit to 8-bit quantization control. Dithering algorithm based on truncation error from previous pixel.

    00   Enable simple truncation

    01   Enable dithering (default)

    10   Enable simple rounding

    11   Reserved

Line_ID_Ctrl

    Line ID control. For line-interleaved mode only.

    0   Line ID continues counting through the vertical blanking interval - (default)

    1   Line ID holds the terminal count from the end of active video through the vertical blanking interval

Chan_ID_SAVEAV_En

    Channel ID inserted in SAV/EAV codes enable, active high. For pixel-interleaved mode only. Always disabled for
    non-interleaved and line-interleaved modes.

    0   Disabled (default)

    1   Enabled

Chan_ID_Blank_En

    Channel ID inserted in blanking level enable, active high. For pixel-interleaved mode only. Always disabled for non-interleaved and
    line-interleaved modes.

    0   Disabled (default)

    1   Enabled

Video_Det_SAVEAV_En

    Video detection status inserted in SAV/EAV codes enable, active high. For non-interleaved and pixel-interleaved
    modes. Always enabled for line-interleaved mode.

    0   VDET insertion disabled (default)

    1   VDET insertion enabled

Table 4-66. OFM Mode Control

Subaddress	B2h
Default	20h

7	6	5	4	3	2	1	0
Reserved	Out_CLK_Freq_Ctl	OSC_OUT_En	Out_CLK_Pol_Sel	Out_CLK_Freq_Sel	Out_CLK_P_En	Out_CLK_N_En	Video_Port_En

This register writes to decoder core 0 only.

Out_CLK_Freq_Ctl

> Output clock frequency control for 4-Ch Half-D1 + 1-Ch D1 and 8-Ch CIF + 1-Ch D1 line-interleaved, hybrid output formats only. Affects both OCLK_P and OCLK_N.
>
> 0   108 MHz (default)
>
> 1   81 MHz

OSC_OUT_En

> Oscillator output enable, active high
>
> 0   OSC_OUT disabled
>
> 1   OSC_OUT enabled (default)

Out_CLK_Pol_Sel

> Output clock polarity select. Affects both OCLK_P and OCLK_N.
>
> 0   Non-inverted (default)
>
> 1   Inverted

Out_CLK_Freq_Sel

> Output clock frequency select for 2-ch pixel-interleaved mode only. Affects both OCLK_P and OCLK_N.
>
> 0   54 MHz (default)
>
> 1   27 MHz

Out_CLK_P_En

> Output data clock+ (OCLK_P) enable, active high
>
> 0   OCLK_P disabled (default)
>
> 1   OCLK_P enabled

Out_CLK_N_En

> Output data clock- (OCLK_N) enable, active high
>
> 0   OCLK_N disabled (default)
>
> 1   OCLK_N enabled (for 2-Ch mode only)

Video_Port_En

> Video port output enable, active high
>
> 0   All four video ports disabled (default)
>
> 1   All video ports required for selected output format enabled

Table 4-67. OFM Channel Select 1

Subaddress   B3h
Default   E4h

7	6	5	4	3	2	1	0
Chan_Sel_Port_D		Chan_Sel_Port_C		Chan_Sel_Port_B		Chan_Sel_Port_A	

This register writes to decoder core 0 only. OFM channel select by video port in 1-Ch mode.

Chan_Sel_Port_D
      Channel select for port D
      00   Ch 1
      01   Ch 2
      10   Ch 3
      11   Ch 4 (default)
Chan_Sel_Port_C
      Channel select for port C
      00   Ch 1
      01   Ch 2
      10   Ch 3 (default)
      11   Ch 4
Chan_Sel_Port_B
      Channel select for port B
      00   Ch 1
      01   Ch 2 (default)
      10   Ch 3
      11   Ch 4
Chan_Sel_Port_A
      Channel select for port A
      00   Ch 1 (default)
      01   Ch 2
      10   Ch 3
      11   Ch 4

NOTE: Each video port must be set to a different channel.

Table 4-68. OFM Channel Select 2

Subaddress	B4h
Default	E4h

7	6	5	4	3	2	1	0
2nd_Chan_Sel_Port_B		1st_Chan_Sel_Port_B		2nd_Chan_Sel_Port_A		1st_Chan_Sel_Port_A	

This register writes to decoder core 0 only. OFM channel select by video port in 2-Ch mode.

2nd_Chan_Sel_Port_B
    Second channel select for port B
    00   Ch 1
    01   Ch 2
    10   Ch 3
    11   Ch 4 (default)
1st_Chan_Sel_Port_B
    First channel select for port B
    00   Ch 1
    01   Ch 2
    10   Ch 3 (default)
    11   Ch 4
2nd_Chan_Sel_Port_A
    Second channel select for port A
    00   Ch 1
    01   Ch 2 (default)
    10   Ch 3
    11   Ch 4
1st_Chan_Sel_Port_A
    First channel select for port A
    00   Ch 1 (default)
    01   Ch 2
    10   Ch 3
    11   Ch 4

NOTE: Each video port must be set to a different channel.

Table 4-69. OFM Channel Select 3

Subaddress	B5h
Default	00h

7	6	5	4	3	2	1	0
Reserved					Hybrid_Chan_Sel [2:0]		

This register writes to decoder core 0 only.
Hybrid_Chan_Sel [2:0]
    OFM channel select for 1-Ch D1 channel in video cascade mode and hybrid format mode.
    000   Ch 1 (default)
    001   Ch 2
    010   Ch 3
    011   Ch 4
    100   Cascade input from Port C (for video cascade 1st stage only)
    101   Reserved
    110   Reserved
    111   Reserved

Table 4-70. OFM Super-Frame Size

Subaddress   B6h-B7h
Default   041Bh

Subaddress	7	6	5	4	3	2	1	0
B6h	Super_Frame_Size [7:0]							
B7h	Reserved		Ctrl_Mode [1:0]		Super_Frame_Size [11:8]			

These registers write to decoder core 0 only.

Ctrl_Mode [1:0]

      Super-frame size control mode

      00   Super-frame size based on 525-line standard (default)

      01   Super-frame size based on 625-line standard

      10   Reserved

      11   Super-frame size based on manual setting (see subaddress B6h/B7h)

Super_Frame_Size [11:0]

      Total number of lines per super-frame. For line-interleaved mode only.

      0100 0001 1011   1051 (default)

NOTE: Has no effect on port B in the video cascade interface.

Table 4-71. OFM H-Blank Duration

Subaddress   B8h-B9h
Default   0040h

Subaddress	7	6	5	4	3	2	1	0
B8h	OFM_HBlank_Duration [7:0]							
B9h	Reserved			HBlank_ Duration_ Mode	Reserved		OFM_HBlank_ Duration [9:8]	

These registers write to decoder core 0 only.

HBlank_Duration_Mode

      H-blank duration control mode.

      0   H-blank duration automatically controlled (8-bit output mode: 40h, 16-bit output mode: 80h)

      1   H-blank duration based on manual setting (see subaddress B8h/B9h)

OFM_HBlank_Duration [9:0]

      Horizontal blanking duration in OCLK_P clock cycles. For non-interleaved and line-interleaved modes.

      00 0100 0000   64 (default)

Table 4-72. Misc OFM Control

Subaddress	BAh
Default	00h

7	6	5	4	3	2	1	0
Reserved							OFM_Soft_Reset

OFM_Soft_Reset

Soft reset for OFM logic.

Note: This bit is automatically cleared by firmware when the reset is completed.

0   Normal operation (default)

1   Reset output formatter logic

NOTE: In cascade mode, the OFM reset of the 1st stage should be asserted after the OCLK_N output of the 2nd stage is enabled.

Table 4-73. Audio Sample Rate Control

Subaddress	C0h
Default	00h

7	6	5	4	3	2	1	0
Reserved						Aud_SamRate_Set [1:0]	

Aud_SamRate_Set [1:0]

Audio sample rate control bits.

00   16 kHz (default)

01   Reserved

10   8 kHz

11   Reserved

Table 4-74. Analog Audio Gain Control 1

Subaddress   C1h
Default   88h

7	6	5	4	3	2	1	0
Audio_Gain_Ctrl_CH2				Audio_Gain_Ctrl_CH1			

Audio_Gain_Ctrl_CH2

    Analog audio gain control for audio Ch 2. See values below.

Audio_Gain_Ctrl_CH1

    Analog audio gain control for audio Ch 1

    0000   -12.0 dB
    0001   -10.5 dB
    0010   -9 dB
    0011   -7.5 dB
    0100   -6 dB
    0101   -4.5 dB
    0110   -3 dB
    0111   -1.5 dB
    1000   0 dB (default)
    1001   Reserved
    1010   Reserved
    1011   Reserved
    1100   Reserved
    1101   Reserved
    1110   Reserved
    1111   Reserved

Table 4-75. Analog Audio Gain Control 2

| **Subaddress** | C2h |
| **Default** | 88h |

7	6	5	4	3	2	1	0
Audio_Gain_Ctrl_CH4				Audio_Gain_Ctrl_CH3			

Audio_Gain_Ctrl_CH4

    Analog audio gain control for audio Ch 4. See values below.

Audio_Gain_Ctrl_CH3

    Analog audio gain control for audio Ch 3

    0000   -12.0 dB
    0001   -10.5 dB
    0010   -9 dB
    0011   -7.5 dB
    0100   -6 dB
    0101   -4.5 dB
    0110   -3 dB
    0111   -1.5 dB
    1000   0 dB (default)
    1001   Reserved
    1010   Reserved
    1011   Reserved
    1100   Reserved
    1101   Reserved
    1110   Reserved
    1111   Reserved

Table 4-76. Audio Mode Control

Subaddress   C3h
Default   C9h

7	6	5	4	3	2	1	0
SD_M_En	SD_R_En	I2S_Mode	Serial_IF_Format	BCLK_R_Freq	Audio_Data_Format		TDM_Pin_Sel

SD_M_En

    SD_M output enable, active high

    0   SD_M output disabled

    1   SD_M output enabled (default)

SD_R_En

    SD_R output enable, active high.

    0   SD_R output disabled

    1   SD_R output enabled (default)

I2S_Mode

    Audio serial I^2S interface mode

    0   Slave mode (default)

    1   Master mode

Serial_IF_Format

    Audio serial interface format

    0   I^2S justified mode (default)

    1   DSP justified mode

BCLK_R_Freq

    Audio serial interface BCLK_R clock frequency

    0   256 f_s

    1   64 f_s (stand alone operation only) (default)

Audio_Data_Format

    Audio serial interface data format

    00   16-bit PCM (default)

    01   8-bit μ-Law

    10   8-bit A-Law

    11   Reserved

TDM_Pin_Sel

    TDM output pin select

    0   SD_R only

    1   SD_R and SD_M (default)

Table 4-77. Audio Mixer Select

Subaddress   C4h
Default   01h

7	6	5	4	3	2	1	0
Audio_Mixer_Sel [4:0]					TDM_Chan_Number [2:0]		

Audio_Mixer_Sel [4:0]

      Audio mixer output select

      00000   Mix channel (default)

      00001   Ch 1

      00010   Ch 2

      00011   Ch 3

      00100   Ch 4

      00101   Ch 5

      00110   Ch 6

      00111   Ch 7

      01000   Ch 8

      01001   Ch 9

      01010   Ch 10

      01011   Ch 11

      01100   Ch 12

      01101   Ch 13

      01110   Ch 14

      01111   Ch 15

      10000   Ch 16

      10001
      to   Reserved
      11111

TDM_Chan_Number [2:0]

      Number of Audio channels to TDM

      000   2 channels

      001   4 channels (default)

      010   8 channels

      011   12 channels

      100   16 channels

      101   Reserved

      110   Reserved

      111   Reserved

Table 4-78. Audio Mute Control

Subaddress   C5h
Default   00h

7	6	5	4	3	2	1	0
Reserved				Ch4_Mute	Ch3_Mute	Ch2_Mute	Ch1_Mute

Ch4_Mute

     Ch 4 Audio mute enable, active high

     0   Disabled (default)

     1   Enabled

Ch3_Mute

     Ch 3 Audio mute enable, active high

     0   Disabled (default)

     1   Enabled

Ch2_Mute

     Ch 2 Audio mute enable, active high

     0   Disabled (default)

     1   Enabled

Ch1_Mute

     Ch 1 Audio mute enable, active high

     0   Disabled (default)

     1   Enabled

Table 4-79. Analog Mixing Ratio Control 1

Subaddress   C6h
Default   00h

7	6	5	4	3	2	1	0
Audio_Mixing_Ratio_CH2				Audio_Mixing_Ratio_CH1			

Audio_Mixing_Ratio_CH2

     Audio mixing ratio for audio channel 2. See values below.

Audio_Mixing_Ratio_CH1

     Audio mixing ratio for audio channel 1

     0000   0.25 (default)

     0001   0.31

     0010   0.38

     0011   0.44

     0100   0.5

     0101   0.63

     0110   0.75

     0111   0.88

     1000   1.00

     1001   1.25

     1010   1.5

     1011   1.75

     1100   2.00

     1101   2.25

     1110   2.5

     1111   2.75

Table 4-80. Analog Mixing Ratio Control 2

Subaddress	C7h
Default	00h

7	6	5	4	3	2	1	0
Audio_Mixing_Ratio_CH4				Audio_Mixing_Ratio_CH3			

Audio_Mixing_Ratio_CH4

    Audio mixing ratio for audio channel 4. See values below.

Audio_Mixing_Ratio_CH3

    Audio mixing ratio for audio channel 3

0000	0.25 (default)
0001	0.31
0010	0.38
0011	0.44
0100	0.5
0101	0.63
0110	0.75
0111	0.88
1000	1.00
1001	1.25
1010	1.5
1011	1.75
1100	2.00
1101	2.25
1110	2.5
1111	2.75

Table 4-81. Audio Cascade Mode Control

Subaddress	C8h
Default	00h

7	6	5	4	3	2	1	0
Reserved						Audio_Cas_Mode_Ctrl	

Audio_Cas_Mode_Ctrl

    Audio Cascade Mode control which is cascade stage ID. Set to 00 for standalone operation.

00	First stage (channels 1 to 4) (default)
01	Second stage (channels 5 to 8)
10	Third stage (channels 9 to 12)
11	Fourth stage (channels 13 to 16)

Table 4-82. Interrupt Status

Subaddress   F2h
Default   Read Only

7	6	5	4	3	2	1	0
Reserved		Sig_Present	Weak_Sig	Vid_Lock	Macrovision	Vid_Std	Reserved

The Interrupt Status register represents the interrupt status after applying mask bits. Therefore, the status bits are the result of a logical AND between the raw status and mask bits. The external interrupt pin is derived from this register as an OR function of all non-masked interrupts in this register.

Reading data from the corresponding register does not clear the status flags automatically. These flags are reset using the corresponding bits in interrupt clear register.

Sig_Present

     Signal present detect interrupt

     0   Not available

     1   Available

Weak_Sig

     Weak signal detect interrupt

     0   Not available

     1   Available

Vid_Lock

     Video (HV) lock change interrupt

     0   Not available

     1   Available

Macrovision

     Macrovision change interrupt

     0   Not available

     1   Available

Vid_Std

     Video standard change interrupt

     0   Not available

     1   Available

Table 4-83. Interrupt Mask

Subaddress   F4h
Default   00h

7	6	5	4	3	2	1	0
Reserved		Sig_Present	Weak_Sig	Vid_Lock	Macrovision	Vid_Std	Reserved

The host interrupt mask register can be used by the external processor to mask unnecessary interrupt sources for Interrupt Status register bits, and for the external interrupt pin. The external interrupt is generated from all non-masked interrupt flags.

Sig_Present

    Signal present detect interrupt mask

    0   Interrupt disabled (default)

    1   Interrupt enabled

Weak_Sig

    Weak signal detect interrupt mask

    0   Interrupt disabled (default)

    1   Interrupt enabled

Vid_Lock

    Video (HV) lock change interrupt mask

    0   Interrupt disabled (default)

    1   Interrupt enabled

Macrovision

    Macrovision change interrupt mask

    0   Interrupt disabled (default)

    1   Interrupt enabled

Vid_Std

    Video standard change interrupt mask

    0   Interrupt disabled (default)

    1   Interrupt enabled

Table 4-84. Interrupt Clear

Subaddress   F6h
Default   00h

7	6	5	4	3	2	1	0
Reserved		Sig_Present	Weak_Sig	Vid_Lock	Macrovision	Vid_Std	Reserved

The host interrupt Clear register is used by the external processor to clear the interrupt status bits in the host interrupt status register. When no non-masked interrupts remain set in the register, the external interrupt pin also becomes inactive.

Sig_Present

    Signal present interrupt clear

    0   No effect (default)

    1   Clear interrupt bit

Weak_Sig

    Weak signal interrupt clear

    0   No effect (default)

    1   Clear interrupt bit

Vid_Lock

    Video (HV) lock change interrupt clear

    0   No effect (default)

    1   Clear interrupt bit

Macrovision

    Macrovision change interrupt clear

    0   No effect (default)

    1   Clear interrupt bit

Vid_Std

    Video standard change interrupt clear

    0   No effect (default)

    1   Clear interrupt bit

Table 4-85. Decoder Write Enable

Subaddress   FEh
Default   0Fh

7	6	5	4	3	2	1	0
Reserved		Addr Auto Incr	Decoder Auto Incr	Decoder 4	Decoder 3	Decoder 2	Decoder 1

This register controls which of the four decoder cores receives I^{2}C write transactions. A 1 in the corresponding Decoder bit will enable the decoder to receive write commands. Any combination of decoders can be configured to receive write commands, allowing all four decoders to be programmed concurrently.

The following table shows how the address auto-increment and decoder auto-increment functions operate when a multi-byte I^{2}C write transaction occurs. For this example, decoders 2, 3 and 4 are enabled for writes, the sub-address is 0xA0 and 8 bytes of data are written.

Decoder Auto Incr	0		0		1		1	
Addr Auto Incr	0		1		0		1	
Data	**Dec**	**Addr**	**Dec**	**Addr**	**Dec**	**Addr**	**Dec**	**Addr**
1st	2,3,4	A0	2,3,4	A0	2	A0	2	A0
2nd	2,3,4	A0	2,3,4	A1	3	A0	3	A0
3rd	2,3,4	A0	2,3,4	A2	4	A0	4	A0
4th	2,3,4	A0	2,3,4	A3	2	A0	2	A1
5th	2,3,4	A0	2,3,4	A4	3	A0	3	A1
6th	2,3,4	A0	2,3,4	A5	4	A0	4	A1
7th	2,3,4	A0	2,3,4	A6	2	A0	2	A2
8th	2,3,4	A0	2,3,4	A7	3	A0	3	A2

Table 4-86. Decoder Read Enable

Subaddress   FFh
Default   01h

7	6	5	4	3	2	1	0
Reserved		Addr Auto Incr	Decoder Auto Incr	Decoder 4	Decoder 3	Decoder 2	Decoder 1

This register controls which of the four decoder cores responds to I^{2}C read transactions. A 1in the corresponding bit position will enable the decoder to respond to read commands. A 1in Decoder Auto Increment will read the next byte from the next enabled decoder. If Decoder Auto Increment is 0 and more than one decoder is enabled for reading then only the lowest numbered decoder will respond. A 1in Address Auto Increment causes the sub-address to increment after read(s) of the current sub-address are completed.

The following table shows how the address auto-increment and decoder auto-increment functions operate when a multi-byte I^{2}C read transaction occurs. For this example, decoders 2, 3 and 4 are enabled for reads, the sub-address is 0xA0 and 8 bytes of data are read.

Decoder Auto Incr	0		0		1		1	
Addr Auto Incr	0		1		0		1	
Data	Dec	Addr	Dec	Addr	Dec	Addr	Dec	Addr
1st	2	A0	2	A0	2	A0	2	A0
2nd	2	A0	2	A1	3	A0	3	A0
3rd	2	A0	2	A2	4	A0	4	A0
4th	2	A0	2	A3	2	A0	2	A1
5th	2	A0	2	A4	3	A0	3	A1
6th	2	A0	2	A5	4	A0	4	A1
7th	2	A0	2	A6	2	A0	2	A2
8th	2	A0	2	A7	3	A0	3	A2

5   Electrical Specifications

5.1   Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage range	VDD_3_3 to VSS_3_3	0.5 V to 4.0 V
		VDD_1_1 to VSS_1_1	-0.2 V to 1.2 V
		VDDA_3_3 to VSSA_3_3	-0.3 V to 3.6 V
		VDDA_1_8 to VSSA_1_8	-0.2 V to 2.0 V
		VDDA_1_1 to VSSA_1_1	-0.2 V to 1.2 V
V_I	Digital input voltage range	V_I to DGND	-0.5 V to 4.5 V
V_O	Digital output voltage range	V_O to DGND	-0.5 V to 4.5 V
	Analog video input voltage range	A_{IN} to AGND	-0.2 V to 2.5 V
	Analog audio input voltage range	A_{IN} to AGND	-0.2 V to 2.0 V
T_A	Operating free-air temperature range	Commercial range	0°C to 70°C
		Industrial range	-40°C to 85°C
T_{stg}	Storage temperature range		-65°C to 150°C
V_{ESD}	ESD stress voltage[2]	Human-body model (HBM)[3] — OSC_OUT, VSSA, XTAL_IN, XTAL_OUT, VDDA_1_8, VDDA_1_1	500 V
		Human-body model (HBM)[3] — Other Pins	1000 V
		Charged-device model (CDM)[4] — OSC_OUT, VSSA, XTAL_IN, XTAL_OUT, VDDA_1_8, VDDA_1_1	250 V
		Charged-device model (CDM)[4] — Other Pins	500 V

(1)   Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2)   Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.
(3)   Tested per JEDEC JESD22-A114F
(4)   Tested per JEDEC JESD22-C101D

5.2   Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
VDD_3_3	Supply voltage, digital		3	3.3	3.6	V
VDD_1_1	Supply voltage, digital		1	1.1	1.2	V
VDDA_3_3	Supply voltage, analog		3	3.3	3.6	V
VDDA_1_8	Supply voltage, analog		1.65	1.8	1.95	V
VDDA_1_1	Supply voltage, analog		1	1.1	1.2	V
$V_{I(pp)}$	Analog video input voltage (ac-coupling necessary)[1]			1.2		V
$V_{I(pp)}$	Analog audio input voltage (ac-coupling necessary)			0.8		V
V_{IH}	Input voltage high, digital[2] [3]		0.7 VDD_3_3			V
V_{IL}	Input voltage low, digital[4] [3]				0.3 VDD_3_3	V
I_{OH}	Output current: DVO outputs/OCLK_N[3]	V_{OUT} = 2.4 V		-4		mA
I_{OL}	Output current: DVO outputs/OCLK_N[3]	V_{OUT} = 0.4 V		4		mA
I_{OH}	Output current, OCLK_P[3]	V_{OUT} = 2.4 V		-8		mA
I_{OL}	Output current, OCLK_P[3]	V_{OUT} = 0.4 V		8		mA
T_A	Operating free-air temperature	Commercial	0		70	°C
		Industrial	-40		85	°C

(1)   Specified based on a typical 100% Color Bar Signal
(2)   Exception: 0.7 VDDA_1_8 for XTAL_IN terminal
(3)   Specified by design
(4)   Exception: 0.3 VDDA_1_8 for XTAL_IN terminal

5.3   Reference Clock Specifications

	MIN	NOM	MAX	UNIT
Frequency		27		MHz
Frequency tolerance [1]	-50		50	ppm

(1)   This number is the required specification for the external crystal/oscillator and is not tested.

5.4   Electrical Characteristics

5.5   DC Electrical Characteristics

For minimum/maximum values: VDD_1_1 = 1.0 to 1.2 V, VDD_3_3 = 3.0 V to 3.6 V, VDDA_1_1 = 1.0 V to 1.2 V, VDDA_1_8 = 1.65 V to 1.95 V, VDDA_3_3 = 3.0 V to 3.6 V
For typical values (T_A = 25°C): VDD_1_1 = 1.1 V, VDD_3_3 = 3.3 V, VDDA_1_1 = 1.1 V, VDDA_1_8 = 1.8 V, VDDA_3_3 = 3.3 V[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(33D)}$	3.3-V I/O digital supply current	2-Ch D1 mode at 54 MHz		33		mA
		4-Ch D1 mode at 108 MHz		41		mA
$I_{DD(11D)}$	1.1-V core digital supply current	2-Ch D1 mode at 54 MHz		143		mA
		4-Ch D1 mode at 108 MHz		156		mA
$I_{DD(33A)}$	3.3-V analog supply current	2-Ch D1 mode at 54 MHz		4.5		mA
		4-Ch D1 mode at 108 MHz		4.5		mA
$I_{DD(18A)}$	1.8-V analog supply current	2-Ch D1 mode at 54 MHz		172		mA
		4-Ch D1 mode at 108 MHz		168		mA
$I_{DD(11A)}$	1.1-V analog supply current	2-Ch D1 mode at 54 MHz		14		mA
		4-Ch D1 mode at 108 MHz		17		mA
P_{TOT}	Total power dissipation, normal operation	2-Ch D1 mode at 54 MHz		606		mW
		4-Ch D1 mode at 108 MHz		643		mW
P_{APWD}	Power dissipation with audio powered down	4-Ch D1 mode at 108 MHz		619		mW
P_{DOWN}	Total power dissipation with power down (I^2C register 1Ah set to FFh)			90		mW
I_{lkg}	Input leakage current				20	µA
C_I	Input capacitance [2]				8	pF
V_{OH}	Output voltage high	I_{OH} = -4 mA	0.8 VDD_3_3			V
V_{OL}	Output voltage low	I_{OL} = 4 mA			0.2 VDD_3_3	V

(1)   Typical current measurements made with 4-Ch D1 video output at 108 MHz with 4-Ch audio.
(2)   Specified by design

5.6 Video A/D Converters Electrical Characteristics

ADC sample rate = 27 MSPS for video Ch 1, Ch 2, Ch 3, Ch 4

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Video ADC conversion rate			27		MHz
Z_i	Input impedance, analog video inputs[1]		200			kΩ
C_i	Input capacitance, analog video inputs[1]				10	pF
$V_{i(PP)}$	Full-scale input range of ADC[2]	$C_{coupling}$ = 0.1 μF	1.4			V
G	Nominal analog video gain[1]			-2.9		dB
DNL	Absolute differential non-linearity[3]	AFE only		0.75	1	LSB
INL	Absolute integral non-linearity	AFE only		1	2.5	LSB
FR	Frequency response	Multiburst (60 IRE)		-0.9		dB
XTALK	Input crosstalk[1]	1 MHz		-50		dB
SNR	Signal-to-noise ratio (all channels)[4]	Fin = 1 MHz, 1.0 Vpp		54		dB
NS	Noise spectrum	Luma ramp (100 kHz to full, tilt null)		-51		dB
DP	Differential phase	Modulated ramp		0.5		deg
DG	Differential gain	Modulated ramp		±1.5		%

(1) Specified by design
(2) Full range video
(3) No missing codes
(4) Based on 10-bit internal ADC test mode

5.7 Audio A/D Converters Electrical Characteristics

ADC sample rate = 32.768 MSPS for audio Ch 1, Ch 2, Ch 3, Ch 4

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Audio ADC conversion rate	f_S = 16 kHz		32.768		MHz
Z_i	Input impedance, analog audio inputs[1]	0-dB PGA gain	20			kΩ
C_i	Input capacitance, analog audio inputs[1]				10	pF
$V_{i(PP)}$	Full-scale input voltage range of ADC	$C_{coupling}$ = 2.2 μF, 0-dB PGA gain	1			V
DNL	Absolute differential non-linearity[2]	AFE only		0.75	1	LSB
INL	Absolute integral non-linearity	AFE only		1	2.5	LSB
XTALK	Crosstalk between any two channels			-50		dB
SNR	Signal-to-noise ratio (all channels)	f_S = 16 kHz, V_{IN} = -60 dB, 1 kHz		56		dB
	System clock frequency per channel			512 f_S		Hz

(1) Specified by design
(2) No missing codes

5.8 Video Output Clock and Data Timing

10-pF load for 27 MHz and 54 MHz, 6-pF load for 108 MHz

NO.	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Duty cycle, OCLK_P/OCLK_N	≤50%, OCLK_P/OCLK_N = 108 MHz	44	50	55	%
t3	Fall time, OCLK_P/OCLK_N	90% to 10%, OCLK_P/OCLK_N = 27 MHz			1.4	ns
		90% to 10%, OCLK_P/OCLK_N = 108 MHz			1.15	ns
t4	Rise time, OCLK_P/OCLK_N	10% to 90%, OCLK_P/OCLK_N = 27 MHz			1.4	ns
		10% to 90%, OCLK_P/OCLK_N = 108 MHz			1.15	ns
t1	Fall time, Data	90% to 10%, Data = 27 MHz			3.4	ns
		90% to 10%, Data = 108 MHz			2.9	
t2	Rise time, Data	10% to 90%, Data = 27 MHz			4.2	ns
		10% to 90%, Data = 108 MHz			3.4	
t5	Propagation delay from falling edge of OCLK_P/OCLK_N	50%, OCLK_P/OCLK_N = 27 MHz	1.9		4.86	ns
		50%, OCLK_P/OCLK_N = 108 MHz	0.22		1.5	ns
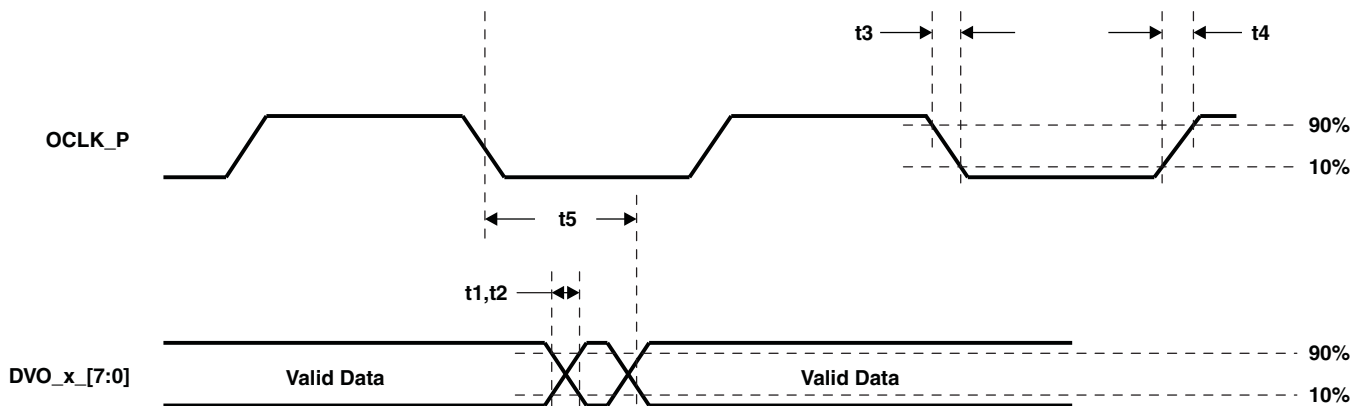
Figure 5-1. Video Output Clock and Data Timing

5.8.1 Video Input Clock and Data Timing

NOTE
Video Cascade Modes: Timing is ensured by design at 27/54MHz input frequency with input trace delays < 2 ns.

5.9 I²C Host Port Timing[1]

NO.	PARAMETER	MIN	TYP	MAX	UNIT
t1	Bus free time between STOP and START	1.3			µs
t2	Data Hold time	0		0.9	µs
t3	Data Setup time	100			ns
t4	Setup time for a (repeated) START condition	0.6			µs
t5	Setup time for a STOP condition	0.6			ns
t6	Hold time (repeated) START condition	0.6			µs
t7	Rise time SDA and SCL signal			250	ns
t8	Fall time SDA and SCL signal			250	ns
C_b	Capacitive load for each bus line			400	pF
f_{I2C}	I²C clock frequency			400	kHz

(1) Specified by design
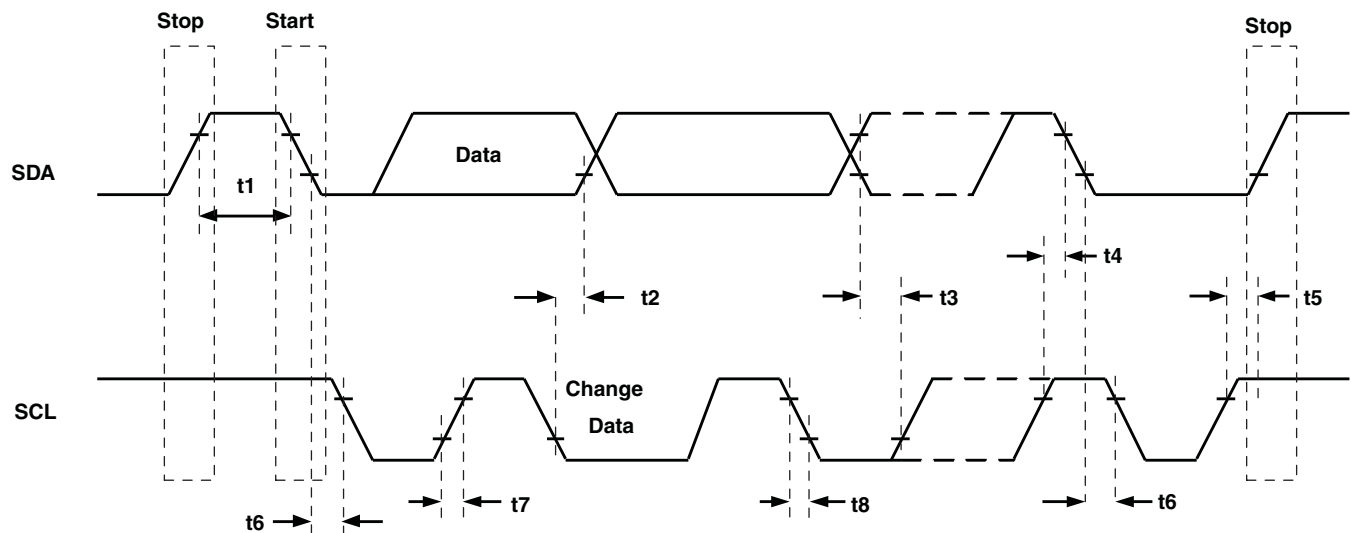
Figure 5-2. I²C Host Port Timing

5.9.1 I^2S Port Timing

NOTE
Philips I^2S bus compliant (specified by design) – See the Philips I2S bus specification

5.10 Miscellaneous Timings

PARAMETER		MIN	TYP	MAX	UNIT
t_{RESET}	RESETB Signal Low Time for valid reset	20			ms
t_{valid}	I^2C valid time, Initialization time after reset until I^2C ready	260			µs

5.11 Thermal Specification

Exposed thermal pad must be soldered to PCB (see Section 6.5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
θ_{JA}	Junction to ambient thermal resistance, still air (commercial)	4-layer PCB with solid ground plane		19.5	°C/W
θ_{JA}	Junction to ambient thermal resistance, still air (industrial)	4-layer PCB with solid ground plane		19.1	°C/W
T_J	Junction temperature (commercial)			90	°C
T_J	Junction temperature (industrial)			105	°C

6   Application Information

6.1   4-Ch D1 Applications
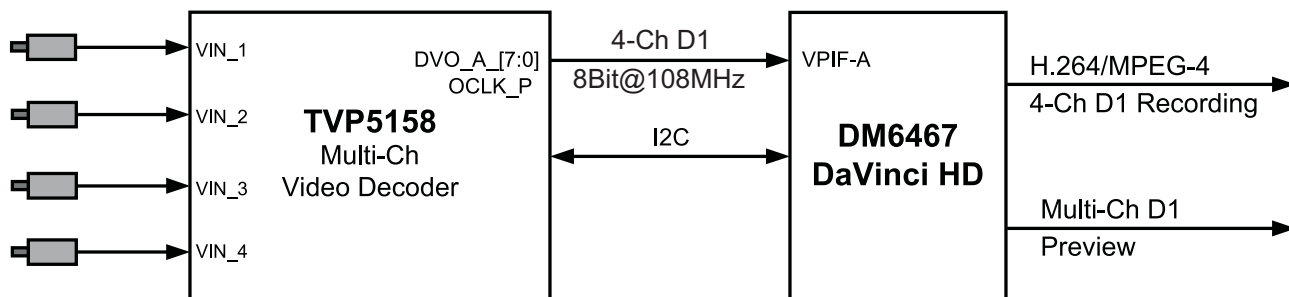
Figure 6-1. 4-Ch D1 Application (Single BT.656 Interface)
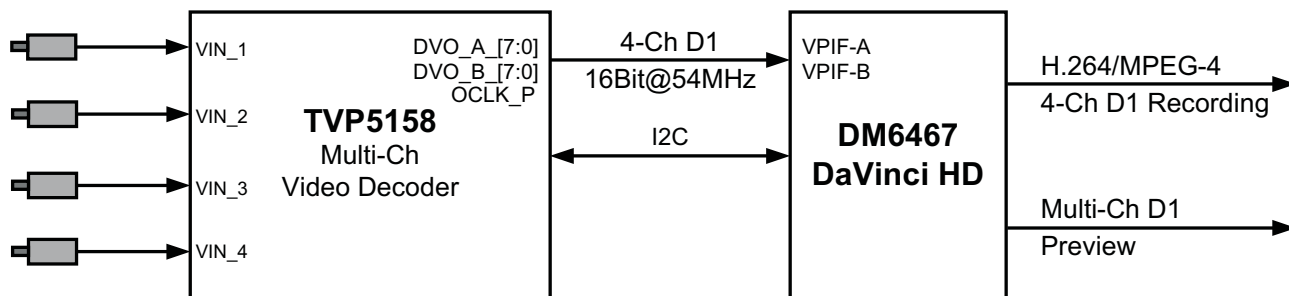
Figure 6-2. 4-Ch D1 Application (16-Bit YCbCr 4:2:2 Interface)
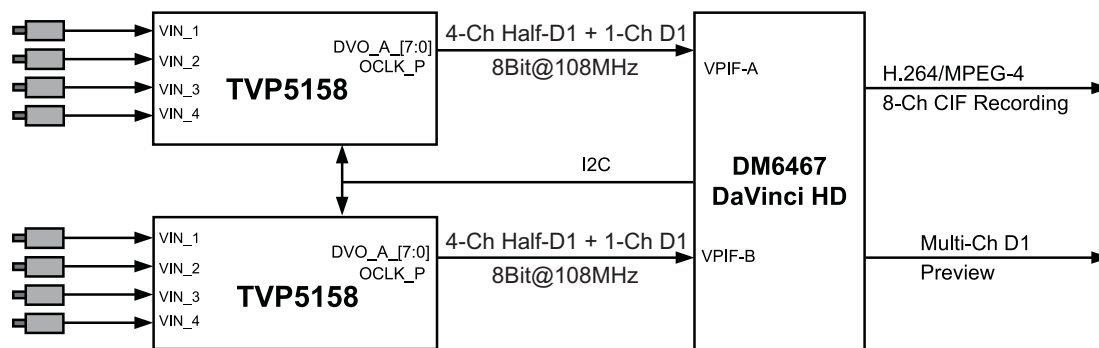
6.2   8-Ch CIF Applications
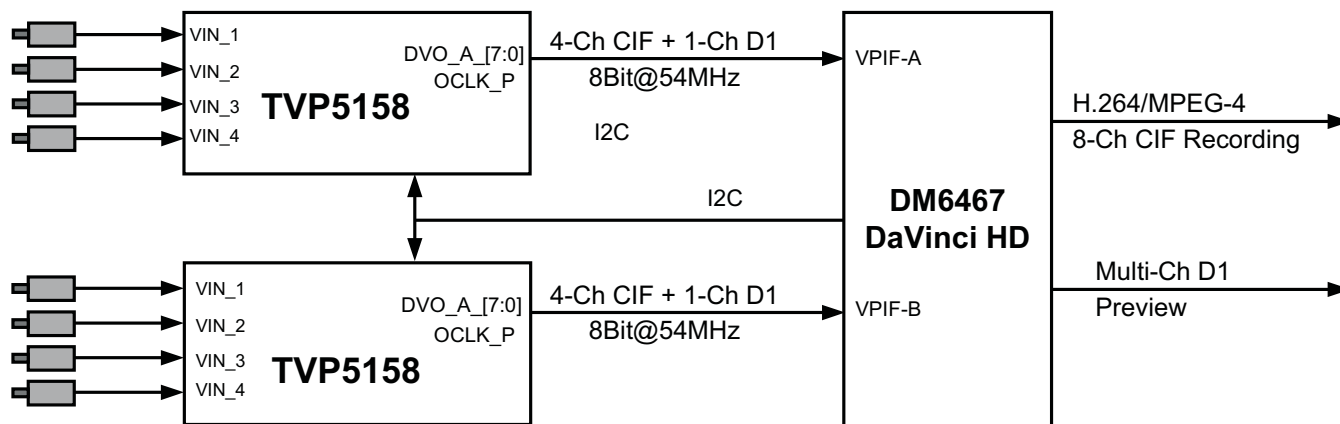
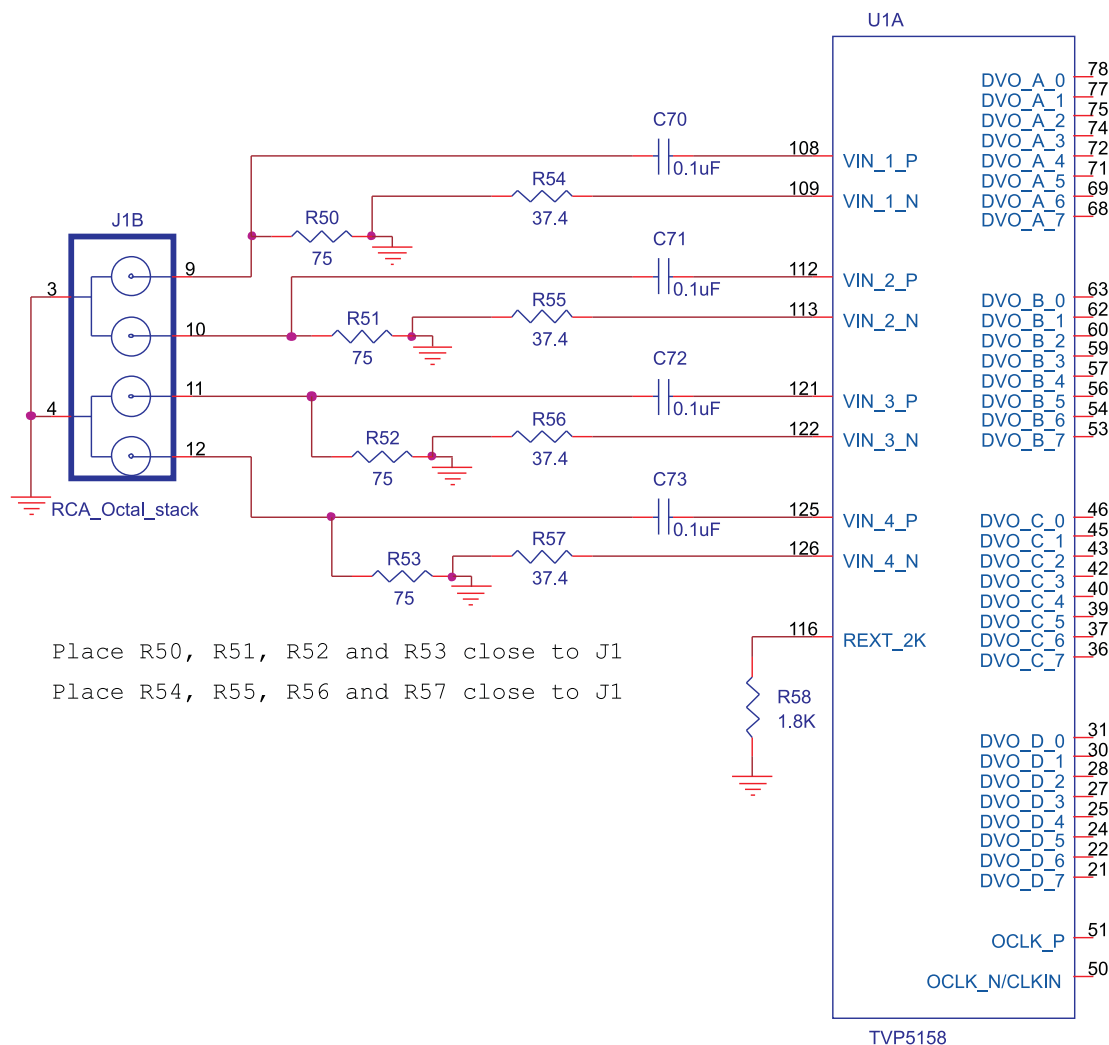**Figure 6-3. 8-Ch CIF Real Time Encoding and Multi-Ch D1 Preview Application**

NOTE: The backend DSP drops one field of Half-D1 to get CIF format video

**Figure 6-4. 8-Ch CIF Real Time Encoding and Multi-Ch D1 Preview Application**

6.3   16-Ch CIF Applications

See Section 3.8.3.3 for the details of 16-Ch CIF applications.

6.4   Application Circuit Examples

Place R50, R51, R52 and R53 close to J1
Place R54, R55, R56 and R57 close to J1

NOTE: System level ESD protection is not included in above application circuit but is recommended.

Figure 6-5. Video Input Connectivity
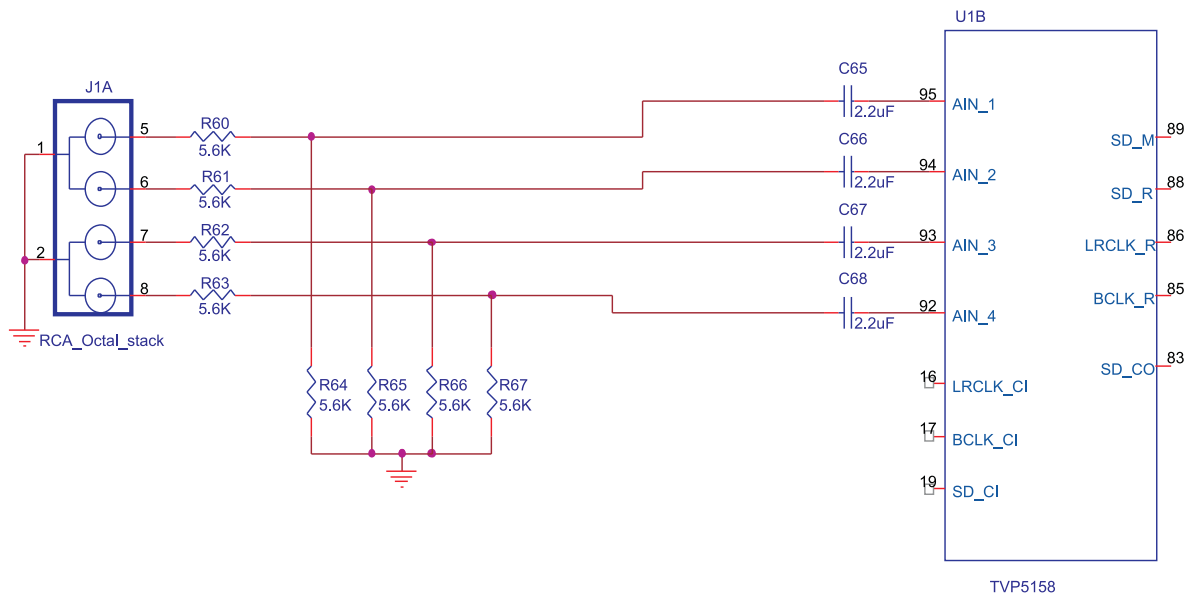
NOTE: System level ESD protection is not included in above application circuit but is recommended.

NOTE: Resistor divider may vary dependent on expected max input audio levels. Desired analog audio input levels should not exceed 1Vpp.

Figure 6-6. Audio Input Connectivity

6.5 Designing with PowerPAD Devices

The TVP5158 device is housed in a high-performance, thermally enhanced, 128-terminal PowerPAD package. Use of the PowerPAD package does not require any special considerations except to note that the thermal pad, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing the PowerPAD PCB features, the use of solder masks (or other assembly techniques) can be required to prevent any inadvertent shorting by the exposed thermal pad of connection etches or vias under the package. The recommended option, however, is not to run any etches or signal vias under the device, but to have only a grounded thermal land as in the following explanation. Although the actual size of the exposed die pad may vary, the minimum size required for the keep-out area for the 128-terminal PFP PowerPAD package is 9mm x 9mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD package. The thermal land varies in size, depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for using thermal lands and thermal vias are detailed in the TI application note *PowerPAD Thermally Enhanced Package* application report (SLMA002).

For the TVP5158 device, this thermal land must be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal terminals. The thermal land can be soldered to the exposed thermal pad using standard reflow soldering techniques.

While the thermal land can be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low-impedance ground plane for the device. More information can be obtained from the TI application note PHY Layout (SLLA020).

7   Revison History

Table 7-1. Revison History

REVISION	COMMENTS
SLES243	Initial release
SLES243A	Table 2-1, XTAL_REF description change. Figure 3-19, 0-ohm resistor added inline between XTAL_REF pin and VSSA.
SLES243B	YUV references changed to YCbCr. Section 1, Trademarks added. Table 2-1, XTAL_IN, XTAL_REF, and XTAL_OUT terminal descriptions moved to Analog Section. Section 3.1.2, Analog Video Input Clamping description changed. Section 3.1.3, Analog Audio Input Clamping description added. Section 3.11, Clock Circuit description changed.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TVP5156PNP	ACTIVE	HTQFP	PNP	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TVP5156PNPR	ACTIVE	HTQFP	PNP	128	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TVP5157PNP	ACTIVE	HTQFP	PNP	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TVP5157PNPR	ACTIVE	HTQFP	PNP	128	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TVP5158IPNP	ACTIVE	HTQFP	PNP	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TVP5158IPNPR	ACTIVE	HTQFP	PNP	128	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TVP5158PNP	ACTIVE	HTQFP	PNP	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TVP5158PNPR	ACTIVE	HTQFP	PNP	128	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
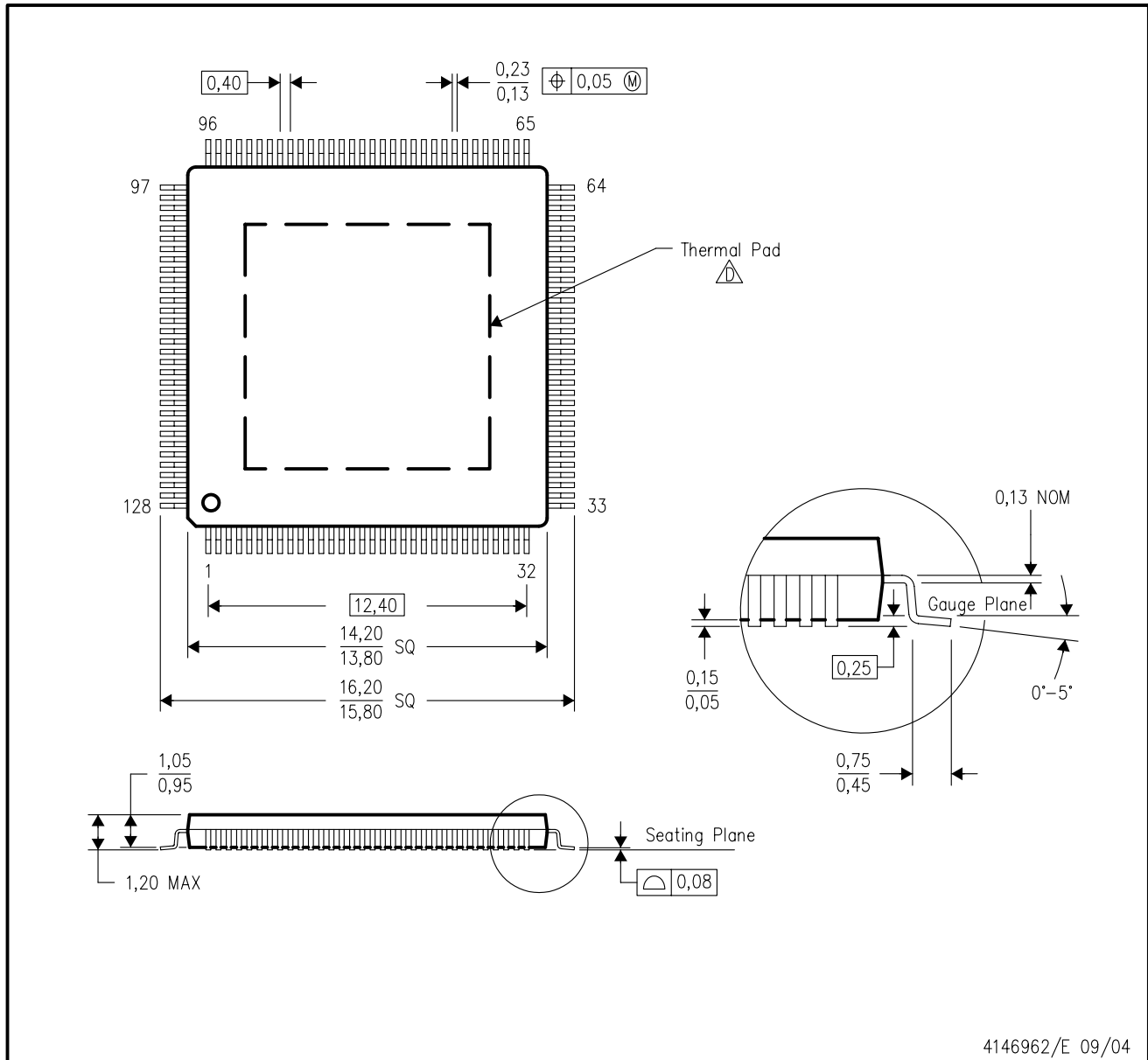
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PNP (S−PQFP−G128)   PowerPAD™ PLASTIC QUAD FLATPACK

0,40   0,23/0,13   ⊕ 0,05 Ⓜ

96   65

97   64

Thermal Pad
△D

128   33

1   32

12,40

14,20/13,80 SQ

16,20/15,80 SQ

0,13 NOM

Gauge Plane

0,15/0,05   0,25   0°−5°

0,75/0,45

1,05/0,95

1,20 MAX

Seating Plane

⌒ 0,08

4146962/E 09/04

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion
        △D   This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
   See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Top View
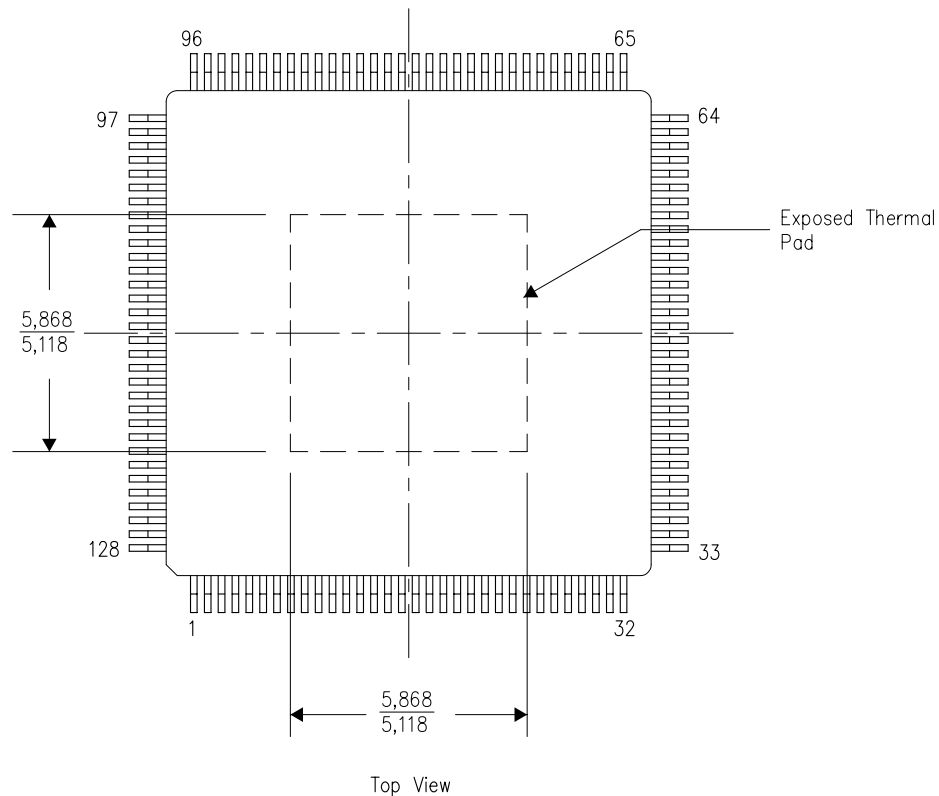
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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