FUJITSU

NMOS SINGLE-CHIP
4-BIT
MICROCOMPUTER

MB88400
SERIES

TM342-A871: January 1987

NMOS SINGLE-CHIP 4-BIT MICROCOMPUTER

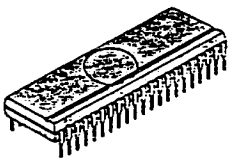
The Fujitsu MB88400H series NMOS single-chip 4-bit microcomputer family is a upgrade version of the conventional MB8840 series.

The currently available member of the MB88400 series is the MB88401 only. MB88401H contain a 4K by 8-bit mask ROM (program memory), a 192 by 4-bit static RAM (data memory), a 36 I/O lines (including a serial port), an 8-bit timer/counter, and a clock generator.

This device fabricated by the NMOS process, packaged in a 42-pin plastic standard, shrink DIP, or 48-pin plastic flat package. They operate with a single +5 V power supply and a 2 MHz clock without a prescaler (or 4.19 MHz clock with prescaler) over the temperature range of -30 °C to +70 °C.

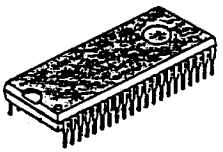
For user's development of the MB88400 series based system, Fujitsu provides the MB88400/500 cross-assembler and host-emulator which run on the CP/M-86 or PC-DOS machines (cross-assembler also run on the Intellec series III MDS), and the MB2115 series evaluation board system, and the MB88408U piggyback EPROM evaluation devices which have external 4K x 8-bit EPROM (MBM2732A). These development tools enables users to minimize their development time and cost.

MB88401-P



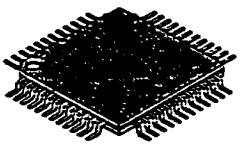
42-PIN PLASTIC STANDARD DIP
(DIP-42P-M01)

MB88401-PSH



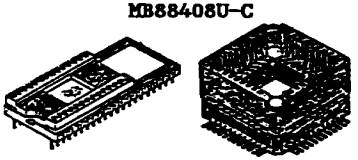
42-PIN PLASTIC SHRINK DIP
(DIP-42P-M02)

MB88401-PF



48-PIN PLASTIC FLAT PACK
(FPT-48P-M02)

MB88408U-C



42-PIN CERAMIC MODULE
(MDP-42C-P04)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FEATURES

- CMOS Single-chip 4-bit Microcomputer

- Program Memory:
  - o 4K x 8-bit mask ROM

- Data Memory:
  - o 192 x 4-bit static RAM

- 36 I/O Lines:
  - o K-Port: 4-bit parallel input only port
  - o P-Port: 4-bit parallel output only port
  - o O-Port: 8-bit parallel output only port
  - o R-Port: Three 4-bit and a 3-bit parallel or 15 individual input/output ports
  - o C-Port: Serial I/O, interrupt input, timer/counter input, and timing output

- Three Selectable Output Port Types for O-, P-, and R-Ports with Mask Option:
  - o Standard open-drain
  - o Standard pull-up
  - o High-current open-drain

- Two Selectable K-Port Input Level with Mask Option:
  - o Standard threshold level
  - o High threshold level

- On-chip Mask-programmable PLA (Programmable Logic Array) for Data Conversion at O-Port

- 8-bit Programmable Timer/Counter with Two Clock Modes:
  - o Internal clock (Timer)
  - o External clock (Counter)

- Software Selectable Serial I/O with 4-/8-bit Serial Buffer/Three Clock Modes:
  - o Internal clock
  - o External clock
  - o Software clock

- On-chip Clock Generator with 2 Mask Options:
  - o External crystal/ceramic resonator or external clock drive
  - o External RC-network or external clock drive

- Mask-option Divide-by-two Clock Prescaler for Expanding Clock Range

- Single Level Four Prior Source Maskable Interrupt:
  - o External
  - o Clock
  - o Timer/counter overflow
  - o Serial buffer full/empty

- 8-nesting Levels for Subroutine Call

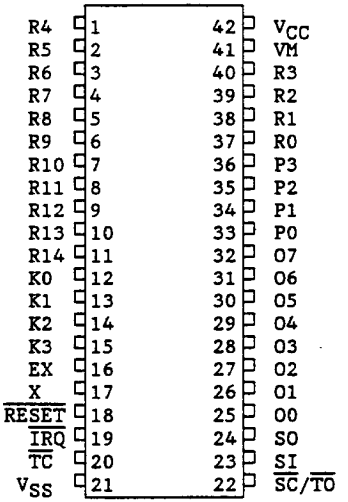
- Instruction Set:
  - o Number of instructions : 75
  - o Instruction length/cycle: 1 byte/1 cycle (82%), 2 bytes/2 cycles (17%), and 2 byte/3 cycle (1%)
  - o Execution time : 2.86µs min. using 4.19MHz clock with prescaler

FEATURES (Continued)

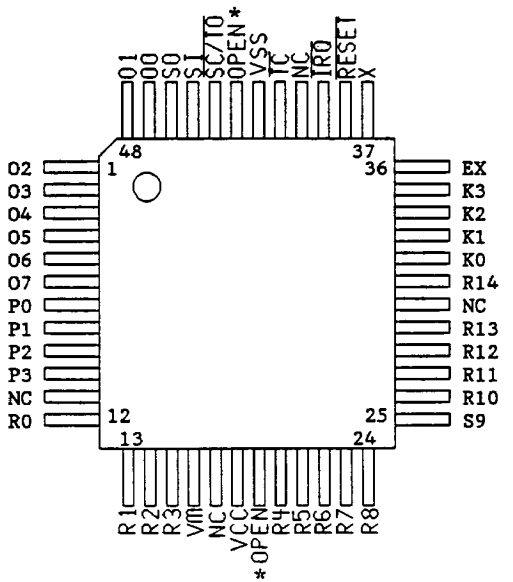
- On-chip Power-on Reset Circuit
- Watch-dog Timer Function with Mask Option
- Power Dissipation: o 75mA
- Power Supply:
  o Main power supply (VCC) : 4.5V to 5.5V
  o Memory back up supply (VM): o Active mode : 4.5V to 5.5V
  o Standby mode: 3.0V to 5.5V
- Operation Temperature Range:
  o T_A= -30 °C to +70 °C
- Silicon Gate NMOS Technology
- Three Package Types:
  o 42-pin plastic standard DIP: Suffix -P
  o 42-pin plastic shrink DIP: Suffix -PSH
  o 48-pin plastic flat package: Suffix -PF
- Powerful Development Support:
  o CP/M-86, PC-DOS, or Intellec series III MDS cross assemblers (SM07415-A012/SMXXXXX-XXXX/SM0525-A010)
  o CP/M-86 or PC-DOS host-emulator software for monitoring evaluation board and symbolic debugging (SM07415-G022/SMXXXX-XXXX)
  o MB2115 evaluation board for software debugging
  o MB88408U NMOS piggyback EPROM evaluation

Fig. 1: PIN ASSIGNMENT

Suffix -P and -PSH
(Top view)



Suffix -PF
(Top View)



Note: * This pin should not be connected must be left open.

Fig. 2: LOGIC SYMBOL

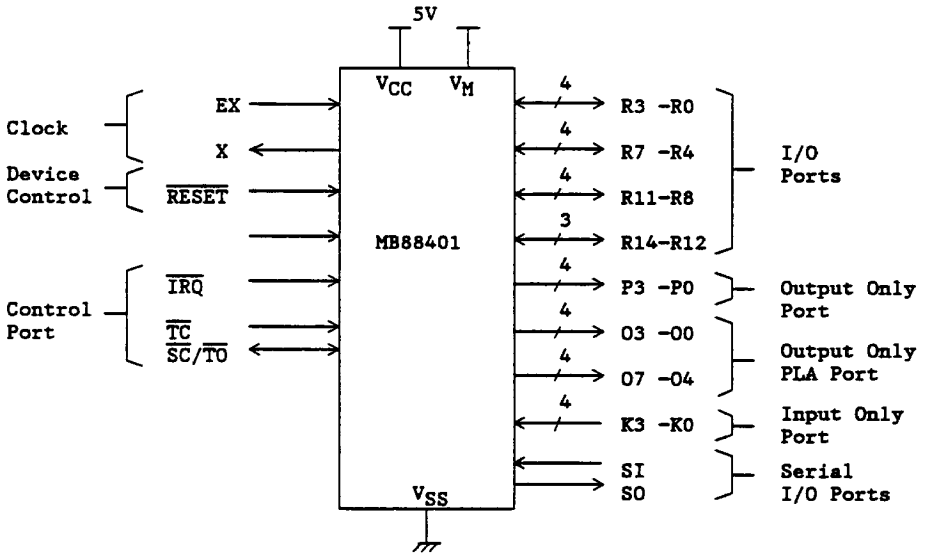
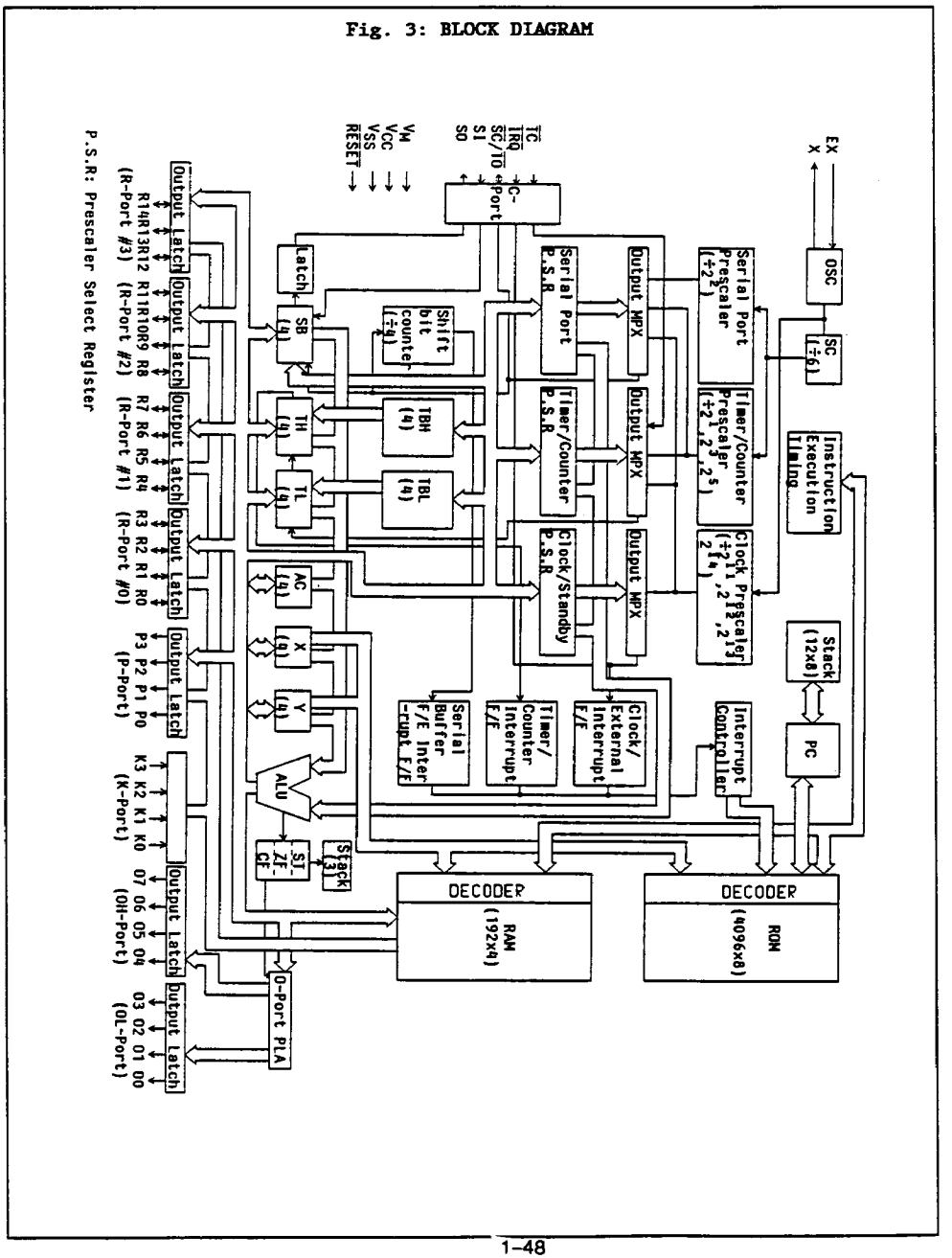


Fig. 3: BLOCK DIAGRAM



P.S.R: Prescaler Select Register

PIN DESCRIPTION

Fig. 1 and Table 1 show the pin assignment and pin description of the MB88400 series.

Table 1: PIN DESCRIPTION

Symbol	Pin No.	Type	Name & Function
• Power Supply			
V_{CC}	42 (18)	–	+5V DC main power supply pin.
V_M	41 (16)	–	Data memory backup power supply.
V_{SS}	21 (42)	–	Ground pin.
• Clock			
EX	16 (36)	I	**Oscillator Input**: Input to the inverting amplifier that forms the on-chip oscillator. An external crystal/ ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation types can be selected using mask option. When an external oscillator is used, the EX pin receives the external oscillator signal. This pin is a non-hysteresis input when the crystal/ ceramic oscillator is selected, and a hysteresis input when the RC-network oscillator is selected.
X	17 (37)	O	**Oscillator Output**: Output of the inverting amplifier that forms the on-chip oscillator, and input to the internal clock generator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillator types can be selected using mask option. When an external oscillator is used, the X pin should be left open.
• Device Control			
$\overline{\text{RESET}}$	18 (38)	I	**Reset**: This pin function as an external reset input or power-on reset output. External reset input: A reset input to the internal reset circuit. A low level on the $\overline{\text{RESET}}$ pin forcedely stops the MCU's operation, and initializes its internal state. After the $\overline{\text{RESET}}$ pin returns high, the MCU restarts execution of program from address #0. The $\overline{\text{RESET}}$ pulse must be low for at least two instruction cycles while the oscillator is stably running after power-on. This pin is a hysteresis input with an internal pullup resistor. An external capacitor from the $\overline{\text{RESET}}$ pin to the VSS pin (and the internal pull-up resistor), whose time constant should be greater than the reset time required (12 clock periods) composes the external reset circuit.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• Device Control (Continued)			
$\overline{RESET}$	18 (38)	I/O	Power on reset output: A reset output from the on-chip reset control circuit. Normally this output is high during the active operation except the reset mode. The rising of the VCC voltage after power on outputs a low level on the $\overline{RESET}$ pin, and them automatically returns high 2^{18} clock periods after the oscillator starts by power on. This pin is a hysteresis input with an internal pullup resistor.
• C-Port			
$\overline{IRQ}$	19 (39)	I	**Interrupt Request**: A maskable external interrupt input to the on-chip interrupt control circuit. The falling edge of the $\overline{IRQ}$ pulse sets the external interrupt request flag (IRF) in the interrupt flag register regardless of enabling or disabling the external interrupt. If the external interrupt is enabled in advance by EN instruction, the interrupt sequence starts at once. Otherwise, the IRF flag is internally held as an interrupt source. Also, the $\overline{IRQ}$ pin state (logical level), which is reflected in the external interrupt input flag (IF) regardless of enabling or disabling the external interrupt, is testable using TSTI instruction. (When $\overline{IRQ}$ = L, IF = 1; otherwise IF = 0.) This pin is a hysteresis input with an internal pullup resistor.
$\overline{TC}$	20 (40)	I	**Timer/Counter**: An external count clock input to the on-chip 8-bit timer/counter. The falling edge of the $\overline{TC}$ pulse increments the timer/counter by one bit, when the external count clock (counter) mode is enabled by EN instruction programming the timer/counter prescaler select register using OUT instruction (with Y = B). Also, the TC pin state (logical level), which is reflected in the timer/counter input flag (TCIF) in the timer/counter prescaler select register regardless of enabling or disabling the external count clock (counter mode, is testable by reading the prescaler select register using IN instruction (with Y = B). (When $\overline{TC}$ = L, TCIF = 1; otherwise TCIF = 0.) This pin is inactive as a count clock input when the external count clock mode is not selected or the timer/counter is disabled by DIS instruction or reset. This pin is a hysteresis input with an internal pullup resistor.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port (Continued)			
$\overline{SC}/\overline{TO}$	22 (44)	I/O	**Shift Clock/Timing Output:** One of the shift clock input ($\overline{SC}$), shift clock output ($\overline{SC}$), or synchronous timing output ($\overline{TO}$) is enabled using EN instruction.
		I	$\overline{SC}$: 1) Shift clock input to the on-chip serial port: When the external shift clock mode is enabled for the serial port, the falling edge of the external $\overline{SC}$ clock shifts the contents of the internal serial buffer one bit right (from MSB to LSB). This input is inactive when the external clock mode is not selected or the serial port disabled by DIS instruction or reset. This pin is a hysteresis input. 2) Shift clock output from the on-chip serial port: When the internal shift clock mode is enabled, the internal shift clock shifts the contents of the serial buffer one bit right. In this mode, the internal timing signal selected is output onto the $\overline{SC}$ pin for synchronization.
		O	$\overline{TO}$: Synchronous timing output: When the timing output is enabled, the internal timing signal (which is generated by the on-chip state counter outputs, $\phi 1$ and $\phi 2$) is output onto the $\overline{TO}$ pin. By DIS instruction or reset, the $\overline{TO}$ pin is disabled and stops issuing the timing output. This pin is a hysteresis input with an internal pullup resistor
SI	23 (45)	I	**Serial Data Input:** Data input to the on-chip serial port. The rising edge of the external ($\overline{SC}$) or internal shifts the data bit on the SI pin into the MSB of the serial buffer register when the serial port is enabled by EN instruction. Also, the SI pin state (logical level) is reflected in the serial data input flag (SIF) in the serial port prescaler select register regardless of enabling or disabling the serial port. Therefore, the SI pin can be sensed by reading the prescaler register using IN instruction (with Y = A).
SO	24 (46)	O	**Serial Data Output:** Data output with latch of the on-chip serial port. The falling edge of the external ($\overline{SC}$) or internal shift clock shifts the LSB data of the serial buffer register to the serial port output latch, regardless of enabling or disabling to serial port. The content of the output latch directly appears on the SO pin. This pin is a CMOS pullup output, and is set high by reset.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• I/O Ports			
K3-K0	15-12 (35-32)	I	K-Port: A 4-bit parallel non-latched input only port. K0 is LSB. 4-bit data on K-Port is input into the accumulator by INK instruction. These pins are internally pullup.
P3-P0	36-33 (10- 7)	O	P-Port: A 4-bit parallel latched output only port. P0 is LSB. 4-bit data in the accumulator is output to P-Port by OUTP instruction. Refer to Table 4 User mask options for available making option.
O3-O0, O7-O0	28-25 (2,1,48, 47) 32-39 (6-3)	O	O-Port: An 8-bit parallel latched output only port with the on-chip mask programmable PLA (Programmable Logic Array) for output data conversion. Depending on user's PLA pattern, this port functions as a dual 4-bit parallel output or an 8-bit parallel PLA output. Dual 4-bit parallel output: By OUTO instruction, 4-bit data in the accumulator is output, without conversion, onto the lower nibble (O3-O0) or upper nibble (O7-O4) of O-Port, depending on whether the carry flag (CF) is "0" or "1". 8-bit parallel PLA output : By OUTO instruction, 4-bit data in the accumulator and the carry flag (CF) bit are converted into 8-bit data through the PLA array, and the 8-bit data is output to O-Port. Depending on user's PLA pattern, 32 kinds of 8-bit data conversions are possible. For example, it can be encoded into 8-segment data for LED display. Refer to Table 4 User mask options for available making option.
R3 -R0, R7 -R4, R11-R8, R14-R12	40-37, (15-12) 4- 1, (23-20) 8- 5, (27-24) 11- 9 (31,29, 28)	I/O	R-Port: This port functions as three 4-bit parallel input and one 3-bit parallel input (non-latched)/output (latched) ports, or 15 individual input (non-latched)/ output (latched) lines, depending on instructions. Parallel I/O: Each 4-bit and 3-bit port is named R-Port #0 (R3-R0), R-Port #1 (R7-R4), R-Port #2 (R11-R8), and R-Port #3 (R14-R12), and is indirectly addressed by the Y-register (Port #). 4-bit data in the accumulator is output to an addressed port of R-Ports #0 to #3 by OUT instruction. 4-bit data on the addressed port is input into the accumulator by IN instruction. (Before IN instruction, the port to be addressed must be set up to "1" state (input) mode).)

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• I/O Port (Continued)			
R3 -R0, R7 -R4, R11-R8, R14-R12	40-37, (15-12) 4- 1, (23-20) 8- 5, (27-24) 11- 9 (31,29, 28)	I/O	Individual I/O: Each line from R14 to R0 is indirectly addressed by the Y-register (Bit #). The addressed line is individually set/reset by SETR/RSTR instruction, and especially each line of R-Port #0 (R3-R0) is directly set/reset by SETD/RSTD instruction. The addressed line is individually testable by TSTR instruction, and each line of R-Port #2 (R11-R8) is directly testable in particular by TSTD instruction. (Before the TSTR and TSTD instructions, the line to be addressed must be set up to "1" (input mode).) Refer to Table 4 User mask options for available making option.

Note: Parenthesis number is applied to suffix -PF

1

DIFFERENCES BETWEEN MB8840 SERIES AND MB88400 SERIES

Table 2: DIFFERENCES BETWEEN MB8840 SERIES AND MB88400 SERIES

Item \ Device	MB8841	MB88401
ROM Size	· 2K x 8 bits	· 4K x 8 bits
RAM Size	· 128 x 4 bits	· 192 x 4 bits
Oscillator Type	· Crystal/Ceramic, RC-network OSC, or external clock drive	· Crystal/Ceramic OSC or external clock drive · RC-network OSC or external clock drive (Mask option)
Min. Instruction Execution Time	· 3.0µs use 4MHz with prescaler	· 2.86µs use 4.19MHz with prescaler
K-Port Input Level	· Standard threshold	· Standard threshold · High-threshold (Mask option)
Watch-dog Timer Function	· No	· No · Yes (Mask option)
Instruction Number	70	75
Members	· MB8842M/-PSH, MB8846M · MB8843M/-PSH, MB8847M · MB8844M/-PSH, MB8848M part above.	· MB88401-P/-PSH/-PF

INPUT/OUTPUT CIRCUITS

All input-only pins are internally pulled up, and all output-only and input/output pins except O-, P-, and R-Ports have push-pull output buffer (standard pull-up). O-, P-, and R-Ports can have push-pull (standard pull-up) or open-drain (standard or high-current) buffer using mask option.

Table 3: INPUT/OUTPUT CIRCUITS

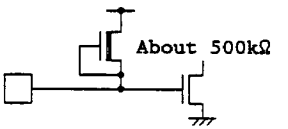
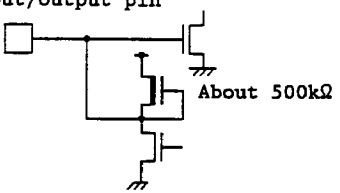
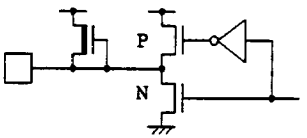
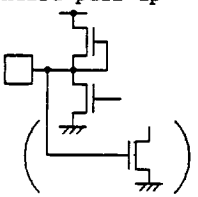
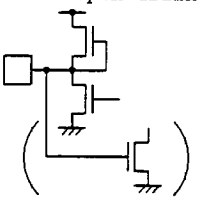
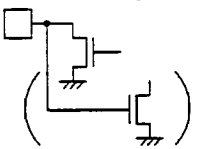
Pin	Circuit	Note
$\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, $\overline{\text{TC}}$, SI, K-Port	• Input only pin 	IIL ≤ -60μA (VCC = 5.5V, VIL = 0.4V)
$\overline{\text{SC}}/\overline{\text{TO}}$	• Input/Output pin 	IIL ≤ -1.8μA (VCC = 5.5V, VIL = 0.4V)
SO	• Output only pin 	VOH ≥ 2.4V (VCC = 4.5V, IOH = -200μA) VOL ≤ 0.4V (VCC = 4.5V, IOL = 1.8mA)
O-Ports, P-Ports, R-Ports	• Standard pull-up 	VOH ≥ 2.4V (VCC = 4.5V, IOH = -200μA) VOL ≤ 0.4V (VCC = 4.5V, IOL = 1.8mA) Internal pullup resistor approx. 10kΩ.
	• Standard open-drain 	VOL ≤ 0.4V (VCC = 4.5V, IOL = 1.8mA) VOL ≤ 0.6V (VCC = 4.5V, IOH = 3.6mA) With 10kΩ pullup resistor

Table 3: INPUT/OUTPUT CIRCUITS (Continued)

Pin	Circuit	Note
O-Ports, P-Ports, R-Ports	• High-current open-drain 	VOL ≤ 0.4V (VCC = 4.5V IOL = 1.8mA) VOL ≤ 2.0V (VCC = 4.5V IOH = 20 mA) With 10kΩ pullup resistor

USER MASK OPTIONS

The MB88400 series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 4: USER MASK OPTIONS

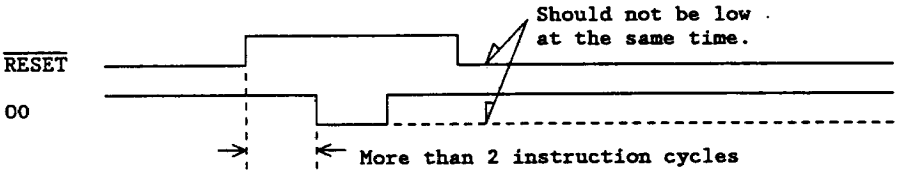
Optional Feature	Symbol	Option	Option No.	Note
Clock Prescaler	CLK	No	0	f_C=0.5 MHz to 2 MHz
		Yes	1	f_C=1 MHz to 4.19MHz
Oscillator Type	OSC	Crystal/ceramic OSC or external clock*	0	* When only external clock drive is used, we recommend RC-network oscillator.
		RC-network OSC or external clock*	1	We recommend no clock prescaler.
Output PLA Data	SPLA	4-bit parallel output	0	
		8-bit parallel output	1	
Output Port Type	PORT	Standard open-drain	2/L	Output port circuit option selected must be the same for all O-, P-, and R-Ports.
		Standard pull-up	3/M	
		High-current open-drain	1/K	
K-Port Input Level	KIN	Standard threshold	0	
		High threshold	1	
Watch-dog Timer Function	WDR	No	0	
		Yes	1	

NOTES ON OPERATION

- **Special Function of O0 Pin**
  The O0 pin has another function as a test terminal, in addition to its normal function O-Port. If the O0 pin is forced low while the $\overline{\text{RESET}}$ pin is low, the MCU is placed in the test mode. Therefore, the O0 pin should not be forced low while the $\overline{\text{RESET}}$ pin is low (when all output ports are initialized).

  Especially when the open-drain is selected for the output port option, the O0 pin should be externally pulled up because such open-drain outputs are subject to noise disturbance if left floating.

  At least 2 instruction cycles are required to change O0 pin from high to low after releasing reset ($\overline{\text{RESET}}$: Low → High)



- **External Capacitors for Crystal Oscillation**
  Fig. 7 gives an aim of an area where the on-chip oscillator has stable oscillator characteristics and short oscillation stabilization time when an average crystal resonator is used.

  The external capacitor should be adjusted to individual crystal resonators when precise oscillation frequency is required. It is recommended to use crystal with a frequency higher than required oscillation frequency, together with the on-chip divided-by-two prescaler, because crystal resonators with lower oscillation frequency generally tends to have longer stabilization time and wider characteristics variation.

- **Supply Voltage**
  Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:
  (1) V_{CC} ripple (peak-to-peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical V_{CC} value.
  (2) V_{CC} transient change rate (such as at switching of power supply): Less than 0.1V/ms.

INSTRUCTION SET DESCRIPTION

The MB88400 series instruction set includes 75 instructions, 82% of which are single-byte and single-cycle, 17% two-byte two-cycle, and 1% two byte three-cycle. The MB88400 series instruction set is exactly the same as the MB88500 series instruction set, and is divided into ten functional groups:

- Register-to-register transfer
- Register-to-memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Control
- Input/Output
- Branch
- Flag manipulation
- Other

Tables 5 and 6 summarize the MB88400 series instruction set.

Table 5: INSTRUCTION SET SUMMARY

	Mnemonic +operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Register-to-Register Transfer	TATH	05	·	·	·	1/1	TH←(AC)
	TATL	06	·	·	·	1/1	TL←(AC)
	TAS	07	·	·	·	1/1	SB←(AC)
	TAY	04	·	·	·	1/1	Y←(AC)
	TSA	17	↕	·	·	1/1	AC←(SB)
	TTHA	15	↕	·	·	1/1	AC←(TH)
	TTLA	16	↕	·	·	1/1	AC←(TL)
	TYA	14	↕	·	·	1/1	AC←(Y)
	XX	1B	↕*1	·	·	1/1	(AC)≠(X)
Register-to-Memory Transfer	L	0D	↕	·	·	1/1	AC←{M(X,Y)}
	LS	2B	↕	·	·	1/1	SB←{M(X,Y)}
	ST	1D	·	·	·	1/1	M(X,Y)←(AC)
	STDC	1A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)-1
	STIC	0A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)+1
	STS	2A	↕	·	·	1/1	M(X,Y)←(SB)
	X	0B	↕*1	·	·	1/1	(AC)≠{M(X,Y)}
	XD D	50-53*	↕*1	·	·	1/1	(AC)≠{M(0,D)}; D=0 to 3 (X=0, Y=D)
	XYD D	54-57*	↕*2	·	·	1/1	(Y) ≠{M(0,D)}; D=4 to 7 (X=0, Y=D)
Constant Transfer	CLA	90	↓	·	·	1/1	AC←0 (Included in LI instruction)
	LI imm	90-9F*	↕	·	·	1/1	AC←imm; imm=0 to 15
	LXI imm	58-5F*	↕	·	·	1/1	X3←0, X2 to X0←imm; imm=0 to 7
	LXID	3D90-3D9F*	↕	·	·	2/2	X←imm; imm=0 to 15
	LRXA imm	3D20-3D3F*	·	·	·	2/3	X ←{ROM(imm | X | Y)}d, d=7-4 AC←{ROM(imm | X | Y)}d, d=3-0 imm=0 to 31
	LYI imm	80-8F*	↕	·	·	1/1	Y ←imm; imm=0 to 15
Arithmetic & Logical Operations	ADC	0E	↕	↕	↓C	1/1	AC←(AC)+{M(X,Y)}+(CF)
	AI imm	3D80-3D8F	↕	↕	↓C	1/1	AC←(AC)+imm; imm=0 to 15
	AND	0F	↕	·	↓Z	1/1	AC←(AC)∩{M(X,Y)}
	C	2E	↕	↕	↓Z	1/1	{M(X,Y)}-(AC)
	CI imm	B0-BF*	↕	↕	↓Z	1/1	imm-(AC); imm=0 to 15
	CYI imm	A0-AF*	·	·	↓Z	1/1	imm-(Y) ; imm=0 to 15

Table 5: INSTRUCTION SET SUMMARY (Continued)

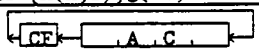
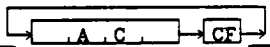
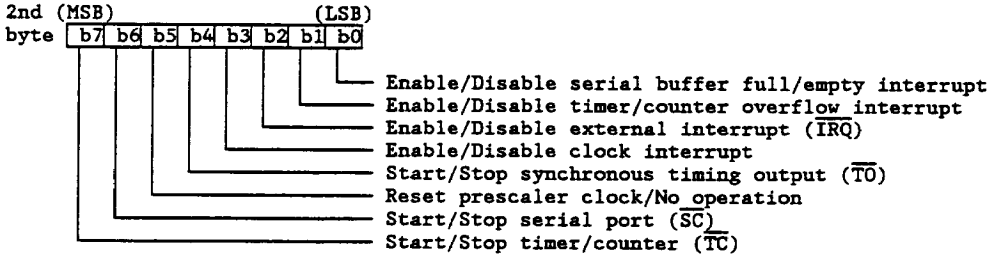
	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Arithmetic & Logical Operation	DAA	10	·	↕	↓C	1/1	AC←(AC)+6 if (AC)>9 or (CF)=1
	DAS	11	·	↕	↓C	1/1	AC←(AC)+10 if (AC)>9 or (CF)=1
	DCA	3D8F	↕	↕	↓C	1/1	AC←(AC)+15 (Included in AI instruc-
	DCM	19	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}-1 tion)
	DCY	18	·	·	↓C	1/1	Y←(Y)-1
	EOR	2F	↕	·	↓Z	1/1	AC←{M(X,Y)}⊕(AC)
	ICA	3D81	↕	↕	↓C	1/1	AC←(AC)+1 (Included in AI instruc-
	ICM	09	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}+1 tion)
	ICX	3DAC	·	·	↓C	2/2	X← (X)+1
	ICY	08	↕	·	↓C	1/1	Y←(Y)+1
	NEG	2D	·	·	↓Z	1/1	AC←(AC)+1
	OR	1F	↕	·	↓Z	1/1	AC←{M(X,Y)}∪(AC)
	ROL	0C	↕	↕	↓C	1/1	
	ROR	1C	↕	↕	↓C	1/1	
	SBC	1E	↕	↕	↓C	1/1	AC←{M(X,Y)}-(AC)-(CF)
Bit Manipulation	RBIT bp	34-37*	·	·	·	1/1	{M(X,Y)}bp←0; bp=0 to 3
	SBIT bp	30-33*	·	·	·	1/1	{M(X,Y)}bp←1; bp=0 to 3
	RBA bp	3DA4 3DA7 *	·	·	·	2/2	(AC)bp←0 ; bp=0 to 3
	SBA bp	3DA0 3DA3 *	·	·	·	2/2	(AC)bp←1 ; bp=0 to 3
	TBA bp	4C-4F*	·	·	↓Z	1/1	(AC)bp-1 ; bp=0 to 3
	TBIT bp	38-3B*	·	·	↓Z	1/1	{M(X,Y)}bp-1; bp=0 to 3
Control	EN imm	3E00-3EFF*	·	·	·	2/2	Enable the internal resources by the operand byte (2nd byte); *3
	DIS imm	3F00-3FFF*	·	·	·	2/2	Disable the internal resources by the operand byte (2nd byte); *3
Input/ Output	IN	13	↕	·	·	1/1	AC←(R)Y ; Y=0 to 3 (Port #) AC←(REG)Y; Y=9 to 15
	INK	12	↕	·	·	1/1	AC←(K)
	OUT	03	·	·	·	1/1	(R)Y←(AC); Y=0 to 3 (Port #) (REG)Y←(R);Y=9 to 15
	OUTO	01	·	·	·	1/1	If CF=0 03-00←(AC) If CF=1 07-04←(AC)
	OUTP	02	·	·	·	1/1	P←(AC)
	RSTD d	44-47*	·	·	·	1/1	(R)d←0; d=0 to 3 (Bit # of Port #0)
	RSTR	22	·	·	·	1/1	(R)Y←0; Y=0 to 15 (Bit #)
	SETD d	40-43*	·	·	·	1/1	(R)d←1; d=0 to 3 (Bit # of Port #0)
	SETR	20	·	·	·	1/1	(R)Y←1; Y=0 to 15 (Bit #)
	TSTD d	48-4B*	·	·	↓Z	1/1	(R)d-1; d=8 to 11 (Bit #)
	TSTR	24	·	·	↓Z	1/1	(R)Y-1; Y=0 to 15 (Bit #)
Branch	CALL addr	6000-6FFF*	·	·	·	2/2	If ST=1, Subroutine Call for addr; addr=0 to 4095. ST=0, Not Subroutine Call.

Table 5: INSTRUCTION SET SUMMARY (Continued)

	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Branch	JMP addr	C0-FF*	·	·	·	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, No Branch.
	JPXY addr	3D00-3D1F*	·	·	·	2/2	Branch always to addr on page #n;
	JPL addr	7000-7FFF*	·	·	·	2/2	If ST=1, Branch to addr; addr=0 to 4095. ST=0, No Branch.
	RTI	3C	·	·	·	1/1	Return From Interrupt Routine
	RTS	2C	·	·	·	1/1	Return From Subroutine
Flag Manipulation	RSTC	23	·	↓	·	1/1	CF←0
	SETC	21	·	↑	·	1/1	CF←1
	TSTC	28	·	·	↓CF	1/1	(CF)-1
	TSTI	25	·	·	↓IF	1/1	(IF)-1, (If $\overline{IRQ}$=L, IF=1)
	TSTS	27	·	·	↓SF	1/1	(SF)-1, SF←0
	TSTV	26	·	·	↓VF	1/1	(VF)-1, VF←0
	TSTZ	29	·	·	↓ZF	1/1	(ZF)-1
Other	NOP	00	·	·	·	1/1	No Operation

Notes:

*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: Each bit of the operand (the second byte) functions as follows:



Symbols and Abreviations

Symbols	Meaning
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
−	Arithmetic minus
⊕	Logical exclusive or
∩	Logical OR
∪	Logical AND
$\overline{\quad}$ (Overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓IF	Set to "0" due to interrupt flag
↓SF	Set to "0" due to serial buffer full/empty flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
-	Not affected

Abbreviation	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
IF	Interrupt flag
imm	Immediate data
$\overline{IRQ}$	Interrupt request
K	K-Port (K3 to K0)
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y-registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
O	O-Port (O7-O0)
PLA	Programmable Logic Array
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R11-R8, #3: R14-R12)
(R)Y; Y=n	① R-Port #n specified by Y-register (Y=0 to 3) ② R-Port bit n specified by Y-register (Y=0 to 14)
(R)d; d=n	R-Port bit n specified by "d" bits in the instruction code
SB	Serial buffer register
SF	Serial buffer full/empty flag
ST	Status flag
TH	Timer/counter high byte
TL	Timer/counter low byte
VF	Timer/counter overflow flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit X-register
Y	Y-register
Z	Zero
ZF	Zero flag

Table 6: INSTRUCTION CODES SUMMARY

L / H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	OUTO	OUTP	OUT	TAY	TATH	TATL	TAS	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	INK	IN	TYA	TTHA	TTLA	TSA	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	TSTS	TSTC	TSTZ	STS	LS	RTS	NEG	C	EOR
3	SBIT bp				RBIT bp				TBIT bp				RTI	* EXT	EN imm	DIS imm
4	SETD d				RSTD d				TSTD d				TBA bp			
5	XD D				XYD D				LXI imm							
6	CALL addr															
7	JPL addr															
8	LYI imm															
9	(CLA)	LI imm														
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

NOTE: : 1-byte/1-cycle instruction : 2-bytes/2-cycles instruction

* See the next page

1

Table 6: INSTRUCTION CODES SUMMARY (Continued)
Extended instruction

3DL / 3DH	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JPXY addr															
1																
2	LRXA imm															
3																
4	NOT USE															
5																
6	NOT USE															
7																
8	(ICA)			AI imm												(DCA)
9	LXID imm															
A	SBA bp				RBA bp				NOT USE				ICX	NOT USE		
B	NOT USE															
C	NOT USE															
D																
E	NOT USE															
F																

Note: : 3 byte/3 cycle instruction

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

The MB88400 series consists of the MB88401. The MB88408U are available as piggyback EPROM evaluation devices. Refer to Table 7.

Table 7: MB88500 SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS

	MB88401-P/-PSH/-PF	MB88408U-C-001E/-002E/-003E
ROM Size	4K x 8 bits (On-chip mask ROM)	4K x 8 bits (External ERPOM)
RAM Size (Directly addressed locations)	192 x 4 bits (0-7)	192 x 4 bits (0-7)
I/O Port: -Input-only Port -Output-only Port -I/O Port -Control Port	Total 36 lines 4 12 15 5 (Including serial I/O)	Total 36 lines 4 12 15 5 (Including serial I/O)
Output Port Type	· Standard pull-up · Standard open-drain · High-current open-drain (Mask option)	· High-current open-drain
K-Port Input Level	· Standard threshold · High threshold	· Standard threshold
Output PLA Pattern	33 patterns · Dual 4-bit parallel ouptut · 8-bit PLA output (32 patterns)	· Dual 4-bit parallel ouptut (-001E) · 8-bit PLA output (-002E/-003E)
Stack Depth (Nesting Level)	8 levels	8 levels
Timer/Counter: -Buffer Size -Clock Source	Yes (Auto loading) 8 bits Internal/External	Yes (Auto loading) 8 bits Internal/External
Serial I/O: -Buffer Size -Clock Source -Output Latch	Yes 4 bits Internal/External Yes	Yes 4 bits Internal/External Yes
Clock Generator: -Oscillator Type -Clock Frequency (With prescaler)	Yes · Crystal/External · RC-network/External (Mask option) 0.5MHz-2MHz (1MHz-4.19MHz)	Yes · Crystal/RC-network/ External 0.5MHz-2MHz (1MHz-4.19MHz)
Clock Prescaler (Divid-by-two)	Yes/No (Mask option)	Yes/No (Selected by external pin)
Interrupt Function -Nesting Level -Interrupt Sources	Yes Single level 4 Sources	Yes Single level 4 Sources
Watch Dog Timer Function	· No · Yes (Mask option)	· No

Table 7: MB88500 SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS

	MB88401-P/-PSH/-PF	MB88408U-C-00XE
Number of Instructions	75	75
Instruction Length/Cycle	1/1, 2/2, or 2/3	1/1, 2/2, or 2/3
Min. Instruction Execution Time	2.86 µs at 4.19 MHz (With prescaler)	2.86 µs at 4.19 MHz (With prescaler)
Power Supply: -Active VCC VM -Standby VM	Single +5V · 4.5V to 5.5V · 4.5V to 5.5V · 3.0V to 5.5V	Single +5V · 4.5V to 5.5V · 4.5V to 5.5V · 3.5V to 6.0V
Operating Temperature range:	-30°C to +70°C	-30°C to +70°C
Process	NMOS	NMOS
Package	· DIP-42P · SH-DIP-42P · QFP-48P	· MDIP-42P
Development Tools: -Hardware -Software	MB2115-01 : CRT unit (Common) MB2115-02 : Monitor board with keyboard (Common) MB2115-04 : EPROM writer (Common) MB2115-13 : DUE board SM05212-A010: Intellec series III MDS cross-assembler SM07415-A012: CP/M-86 cross-assembler SMXXXXX-XXXX: PC-DOS cross-assembler SM07415-G022: CP/M-86 host emulator SMXXXXX-XXXX: PC-DOS host emulator	

ELECTRICAL CHARACTERISTICS

- **ABSOLUTE MAXIMUM RATINGS** †

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	
	V_M	V_{SS}-0.3		V_{SS}+7.0	V	
	V_{SS}		0		V	
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	
Power Dissipation	P_D			1000	mW	
Operating Ambient	T_A	-30		+70	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- **RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Active operation range
	V_M	4.5	5.0	5.5	V	Active operation range
		3.0		5.5	V	Standby operation range
	V_{SS}		0		V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	SI, R-Port, K-Port(Standard threshold)
		2.4		V_{CC}	V	K-Port (High threshold)
	V_{IHS}	4.0		V_{CC}		$\overline{EX}$, $\overline{SC/TO}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{RESET}$
Input Low Voltage	V_{IL}	-0.3		0.8	V	SI, R-Port, K-Port(Standard threshold)
		-0.3		1.2	V	K-Port (High threshold)
	V_{ILS}	-0.3		0.8		$\overline{EX}$, $\overline{SC/TO}$, $\overline{IRQ}$, $\overline{TC}$, $\overline{RESET}$
Operating Ambient Temperature	T_A	-30		+70	°C	

- **DC CHARACTERISTICS**
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage	V_{OH}	O-, P-, R-Ports (Standard pull-up), $\overline{SC}/\overline{TO}$, SO	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
	V_{OHC}	O-, P-, R-Ports (Standard pull-up), $\overline{SC}/\overline{TO}$, SO	V_{CC}=4.5V I_{OH}=-10μA	4.0			V
Output Low Voltage	V_{OL}	$\overline{SC}/\overline{TO}$, SO	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
		O-, P-, R-Ports (All output options)	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
			V_{CC}=4.5V I_{OL}=3.6mA			0.6	V
		O-, P-, R-Ports (High-current open-drain)	V_{CC}=4.5V I_{OL}=20mA			2.0	V
Open-Drain Output Leakage Current	I_{LEAK}	O-, P-, R-Ports (Standard/High-current open-drain)	V_{CC}=5.5V V_{OH}=5.5V (Off state)			40	μA
Input Leakage Current	I_{IL}	R-Port(Standard pull-up), $\overline{SC}/\overline{TO}$	V_{CC}=5.5V V_{IL}=0.4V			-1.8	mA
		$\overline{EX}$, K-Port, $\overline{SI}$, $\overline{RESET}$, $\overline{IRQ}$, $\overline{TC}$	V_{CC}=5.5V V_{IL}=0.4V			-60	μA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V		70		mA
	I_M	V_M	V_M=3.0V		5		μA

- **AC CHARACTERISTICS**

CLOCK TIMING
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_C	EX, X	Crystal/ceramic or RC-network	0.5	2	MHz	Without prescaler
			OSC or external clock drive: Figs. 4 and 5	1	4*		With prescaler * Can use 4.19MHz crystal
Clock Cycle Time	t_{cyc}	EX, X	Figs. 4 and 5	0.5	2	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive(with X open): Figs. 4 and 5	225		ns	Without prescaler
				100			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive(with X open): Figs. 4 and 5	5	200	ns	

Fig. 4: CLOCK TIMING

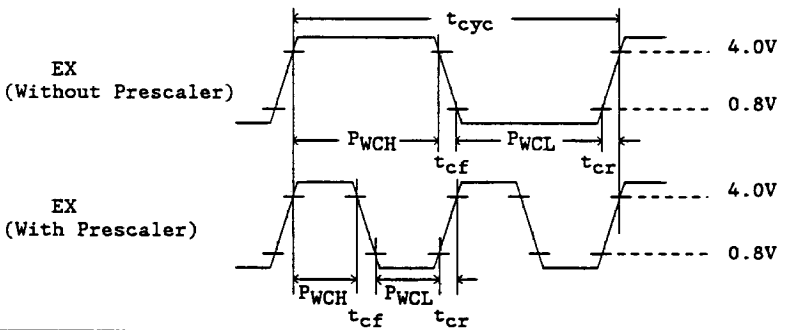
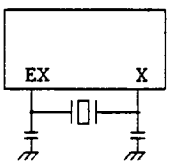
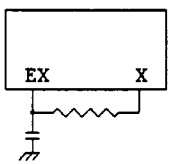


Fig. 5: CLOCK CIRCUIT CONFIGURATIONS

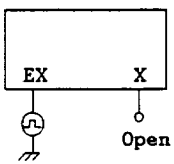
(1) Crystal/Ceramic Oscillator



(2) RC-Network Oscillator*

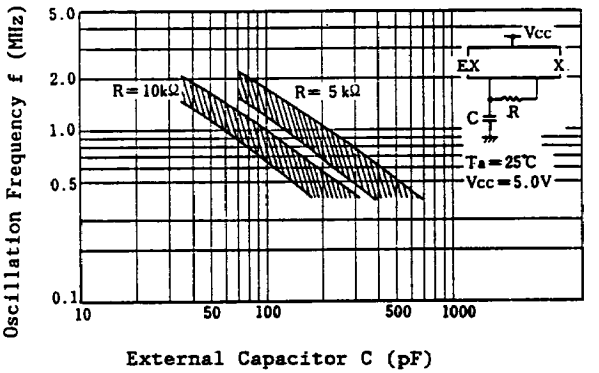


(3) External Clock Drive



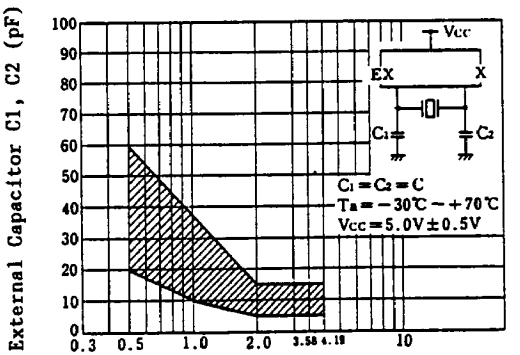
* When the RC-network oscillator is used, the following conditions must be met:
1) The prescaler is not used.
2) V_{CC}=5V±10%
3) T_A=-30°C to +75°C
4) f_C does not exceed 2 MHz (Max. clock frequency is about 1.6 MHz at V_{CC}=5V and T_A=25°C.)

Fig. 6: RC-NETWORK OSCILLATOR CHARACTERISTICS (EXAMPLE)



Note:
When the RC-network oscillator is used, the following conditions must be met:
1) The prescaler is not used. 2) V_{CC}=5V±10%
3) T_A=-30°C to +70°C
4) f_C does not exceed 1.6 MHz.

Fig. 7: CRYSTAL OSCILLATOR CHARACTERISTICS (EXAMPLE)



Notes:
1) The cross-hatched portion is an area where the on-chip oscillator has stable characteristics and short stabilization time when a typical crystal resonator is used. This chart gives an target value of the external capacitor to realize the desired frequency. When an exact frequency is needed, capacitor value should be determined, adjusted to individual crystal resonator characteristics.

2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend a high-frequency crystal resonator with on-chip 1/2 prescaler.

OUTPUT TIMING

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condi-tions	Value		Unit
				Min.	Max.	
O-,P-,R-Ports Delay Time	t_{PDH}	O-Port, P-Port, R-Port	Fig. 8		1000	ns
	t_{PDL}				350	
Serial Port Delay Time	t_{SDH}	SO	Fig. 8		600	ns
	t_{SDL}				600	

Notes:
1. A 10kΩ pull-up is required when open-drain output is used.
2. All the output loading values are 50pF + 1TTL. See figure below.

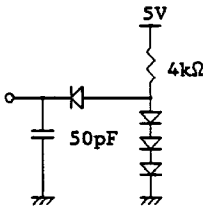
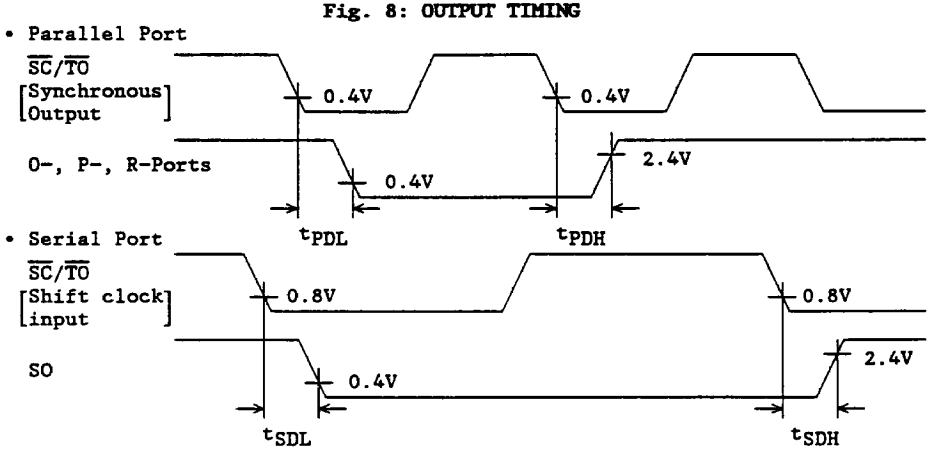


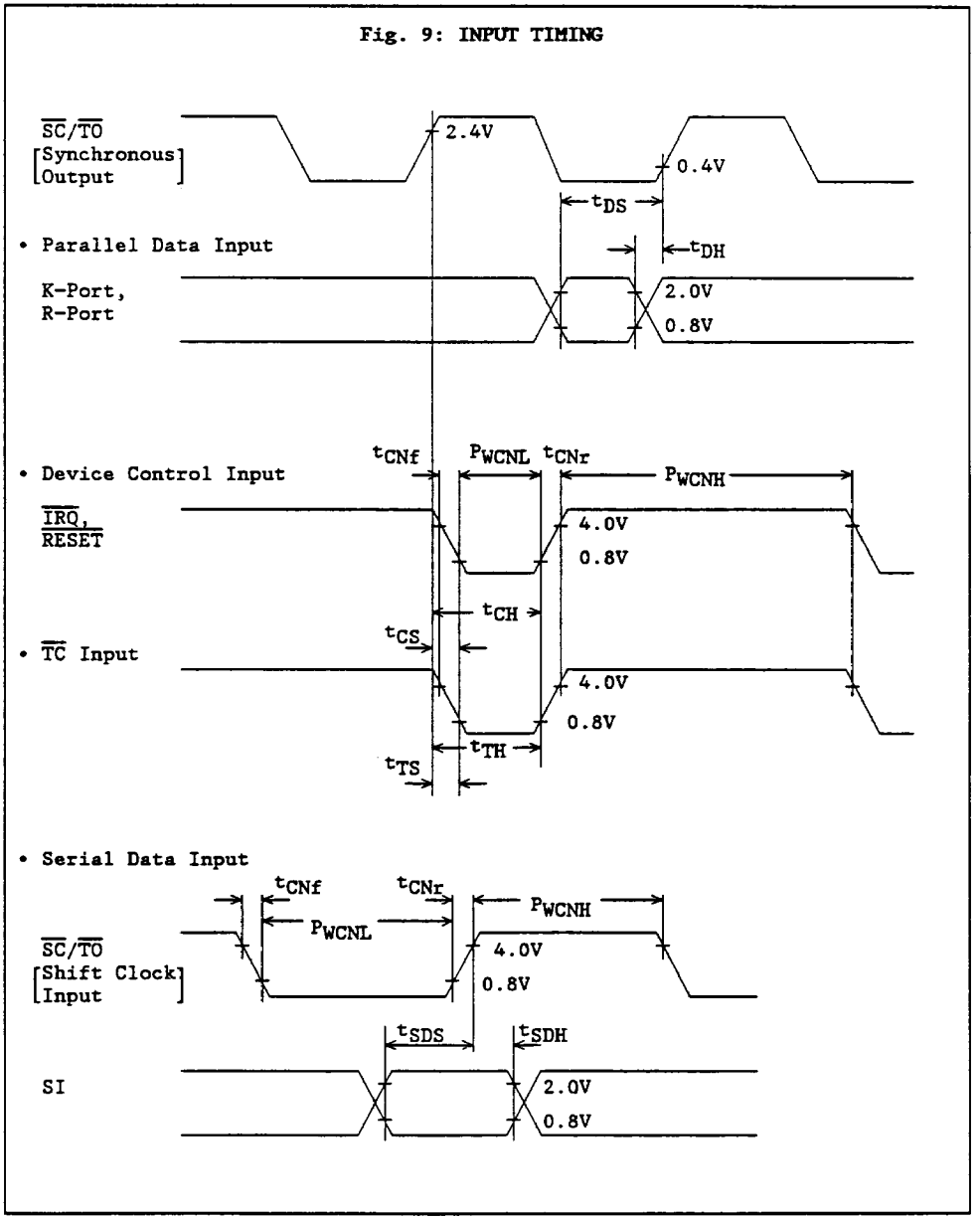
Fig. 8: OUTPUT TIMING



INPUT TIMING(MB88501/A)
(Recommended operating conditions unless otherwise noted.)

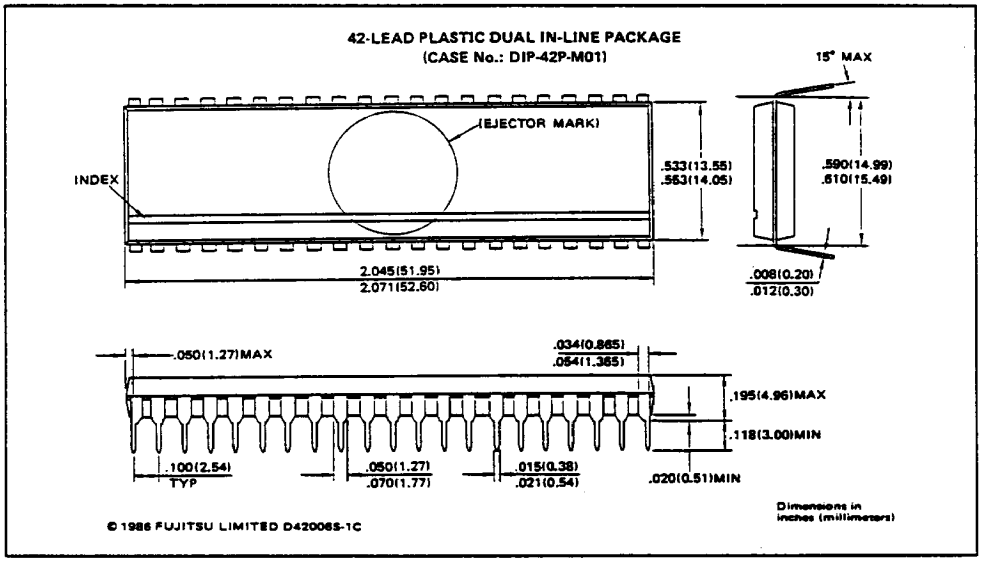
Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	K-Port, R-Port	Fig. 9	$t_{cyc}+1000$		ns
Input Data Hold Time	t_{DH}				$t_{cyc}-50$	
SI Input Setup Time	t_{SDS}	SI	Fig. 9	600		ns
SI Input Hold Time	t_{SDH}			600		
Device Control Setup Time (Synchronous mode)	t_{CS}	$\overline{RESET}$	Fig. 9		$2t_{cyc}-200$	ns
		$\overline{IRQ}$			$2t_{cyc}-200$	
Device Control Hold Time (Synchronous mode)	t_{CH}	$\overline{RESET}$	Fig. 9	$8t_{cyc}+50$		ns
		$\overline{IRQ}$		$2t_{cyc}+50$		
Timing Input Setup Time (synchronous mode)	t_{TS}	$\overline{TC}$	Fig. 9		$2t_{cyc}-200$	ns
Timing Input Hold Time (Synchronous mode)	t_{TH}	$\overline{TC}$	Fig. 9	$2t_{cyc}+50$		ns
Control Signal Low Level Time (Asynchronous mode)	P_{WCNL}	$\overline{SC}/\overline{TO}$	Fig. 9	$6t_{cyc}+250$		ns
		$\overline{IRQ}$, $\overline{TC}$		$6t_{cyc}+250$		
		$\overline{RESET}$		$12t_{cyc}+250$		
Control Signal High Level Time (Asynchronous mode)	P_{WCNH}	$\overline{SC}/\overline{TO}$	Fig. 9	$12t_{cyc}+250$		ns
		$\overline{RESET}$, $\overline{TC}$, $\overline{IRQ}$		$6t_{cyc}+250$		
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	$\overline{START}$, $\overline{SC}/\overline{TO}$, $\overline{IRQ}$ $\overline{RESET}$, $\overline{TC}$	Fig. 9	Should be less than 200ns		

Fig. 9: INPUT TIMING

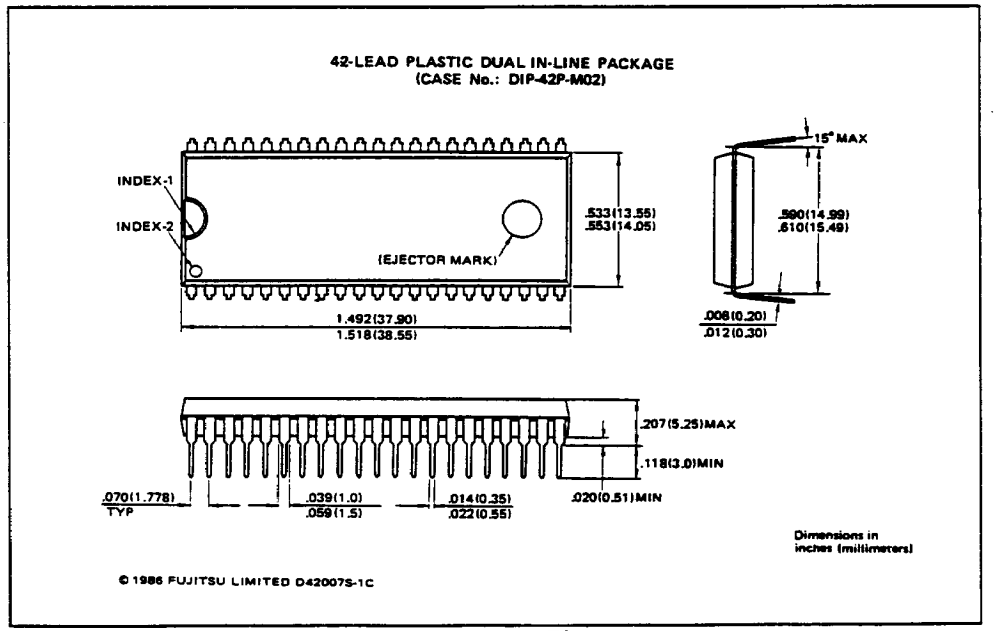


PACKAGE DIMENSIONS

• MB88401-P: 42-PIN PLASTIC STANDARD DIP

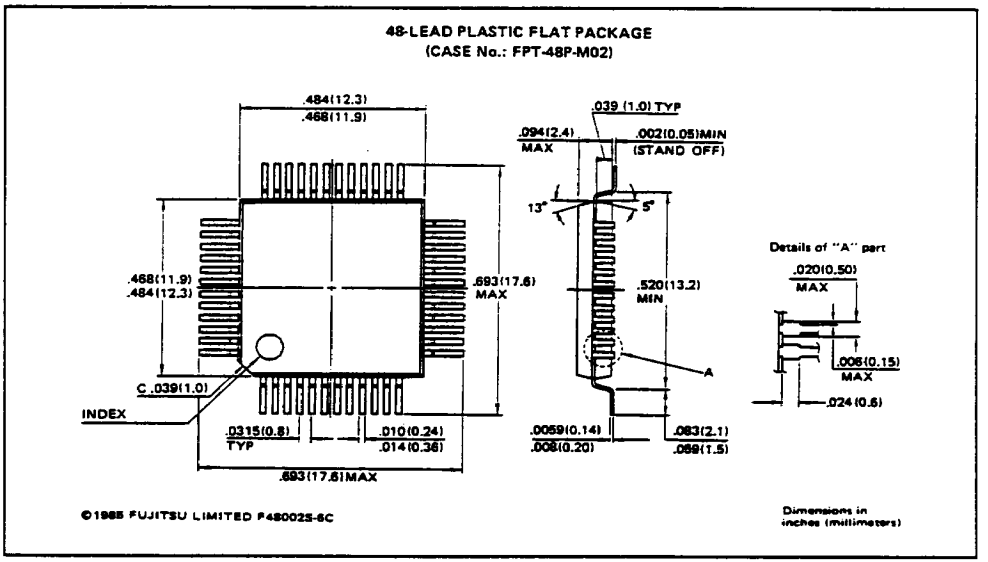


• MB88401-PSH: 42-PIN PLASTIC SHRINK DIP



PACKAGE DIMENSIONS (Continues)

• MB88401-PF: 48-PIN PLASTIC FLAT PACKAGE



• MB88408U-C: 42-PIN CERAMIC MODULE