CPC7583

Line Card Access Switch

Features

- Small 28-pin SOIC or micro-leadframe (MLP) package
- MLP version provides 65% PCB area reduction over 4th generation EMRs, and 60% smaller footprint than SOIC version
- Monolithic IC reliability
- Low, matched, R_{ON}
- Eliminates the need for zero-cross switching
- Flexible switch timing for transition from ringing mode to talk mode.
- Clean, bounce-free switching
- Tertiary protection consisting of integrated current limiting and thermal shutdown for SLIC protection
- 5 V operation with power consumption < 10.5 mW
- Intelligent battery monitor
- Latched logic-level inputs, no external drive circuitry required
- SOIC version pin-compatible with Agere 7583 family

Applications

- Central office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber in the Loop (FITL)
- Pair Gain System
- Channel Banks

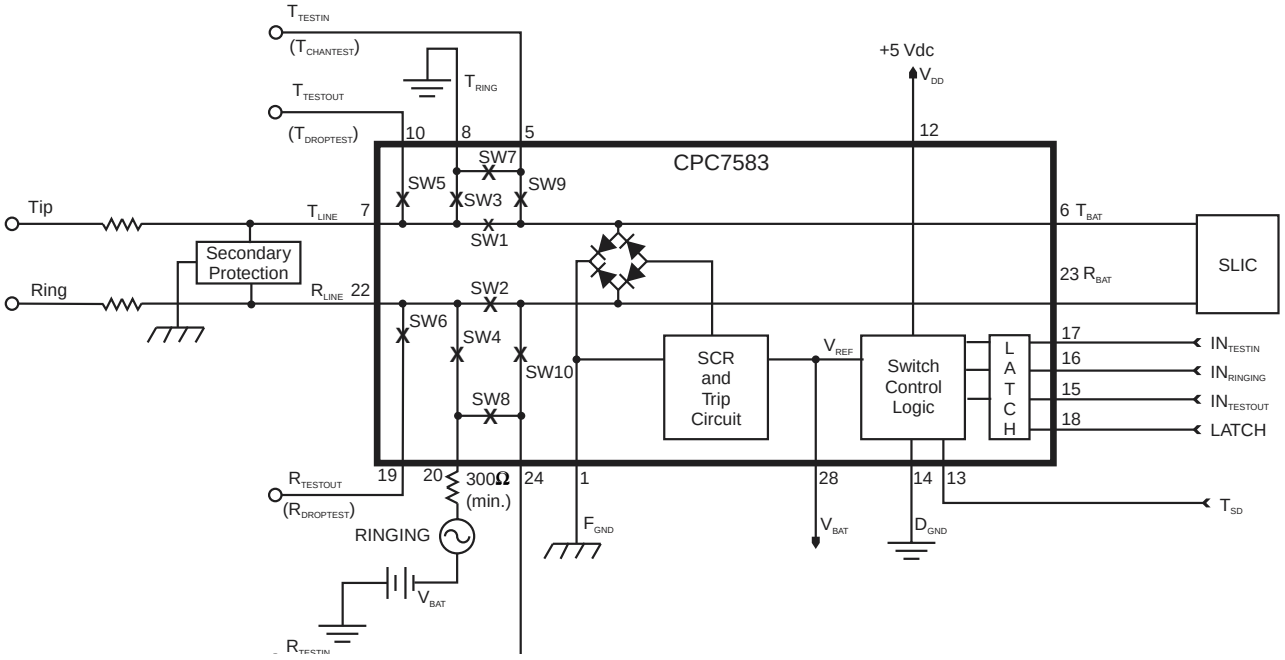
Description

The CPC7583 is a monolithic 10-pole line card access switch in a 28-pin SOIC or MLP package. It provides the necessary functions to replace three 2-Form-C electromechanical relays on analog line cards and combined voice and data line cards found in central office, access, and PBX equipment. The device contains solid state switches for tip and ring line break, ringing injection/ringing return, and test access. The CPC7583 requires only a +5 V supply and offers break-before-make or make-before-break switch operation using simple logic-level input control.

Ordering Information

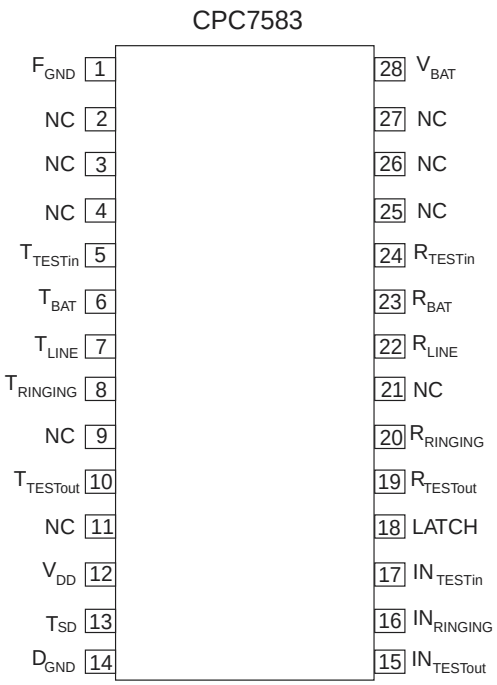
Specify CPC7583Bx for SOIC package in tubes, CPC7583Mx for MLP package in tubes. Add -TR to the part number for tape and reel packaging.

Part Number	Description
CPC7583xA	With protection SCR
CPC7583xB	Without protection SCR
CPC7583xC	With extra logic state and protection SCR
CPC7583xD	With extra logic state but without protection SCR



1. Specifications

1.1 Package Pinout



1.2 Pinout Description

Pin	Name	Description
1	F_{GND}	Fault ground
2	NC	No connection
3	NC	No connection
4	NC	No connection
5	T_{TESTin}	Connect to $TEST_{IN}$ bus tip lead
6	T_{BAT}	Connect to tip on SLIC side
7	T_{LINE}	Connect to tip on line side
8	$T_{RINGING}$	Connect to ringing generator return
9	NC	Not connected
10	$T_{TESTout}$	Connect to $TEST_{OUT}$ bus tip lead
11	NC	No connection
12	V_{DD}	+5 V supply
13	T_{SD}	Temperature shutdown pin. Bi-directional I/O with internal pullup to V_{DD}. Output function indicates status of thermal shutdown circuitry. Input function can be used to set the 'all off' mode using an open-drain type output.
14	D_{GND}	Digital ground
15	$IN_{TESTout}$	Logic-level switch control input
16	$IN_{RINGING}$	Logic-level switch control input
17	IN_{TESTin}	Logic-level switch control input
18	LATCH	Data latch control, active high, transparent low
19	$R_{TESTout}$	Connect to $TEST_{OUT}$ bus ring lead
20	$R_{RINGING}$	Connect to ringing generator current limiting resistor
21	NC	No connection
22	R_{LINE}	Connect to ring on the line side
23	R_{BAT}	Connect to ring on the SLIC side
24	R_{TESTin}	Connect to $TEST_{IN}$ bus ring lead
25	NC	No connection
26	NC	No connection
27	NC	No connection
28	V_{BAT}	Battery voltage supply. Must be capable of sourcing the trigger current for proper operation of the SCR.

1.3 Absolute Maximum Ratings (at 25° C)

Parameter	Minimum	Maximum	Unit
Operating temperature	-40	+110	°C
Storage temperature	-40	+150	°C
Operating relative humidity	5	95	%
Pin soldering temperature (10 seconds max)	-	+260	°C
+5 V power supply	-	7	V
Battery Supply	-	-85	V
Logic input voltage	-	7	V
Logic input to switch output isolation	-	330	V
Switch open contact isolation (SW1, SW2, SW3, SW5, SW6, SW7, SW9, SW10)	-	330	V
Switch open contact isolation (SW4)*	-	480	V
Switch open contact isolation (SW8)*	-	235	V
**Ringing supply side of switch limited to ±210 V with respect to ground*			

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

1.4.1 Power Supply Specifications

Supply	Minimum	Typical	Maximum	Unit
V_{DD}	+4.5	+5.0	+5.5	V
V_{BAT}[1]	-19	-	-72	V

[1] *V_{BAT} is used only for internal protection circuitry. If V_{BAT} rises above -10 V, the device will enter the all-off state and will remain in the all-off state until the battery drops below -15 V.*

ESD Rating (Human Body Model)
1000 V

1.4 Electrical Characteristics, T_A = -40° C to +85° C

Unless otherwise specified, minimum and maximum values are production testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. Typical values are provided for information purposes only and are not part of the testing requirements.

1.4.2 Break Switches, SW1 and SW2

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = +260 V to -60 V	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = +270 V to -60 V			0.3		
-40° C	V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = +250 V to -60 V			0.1		
R_{ON}						
+25° C	T_{LINE} and R_{LINE} = ±10 mA, ±40 mA, R_{BAT} and T_{BAT} = -2 V	R_{ON}	-	14.5	-	Ω
+85° C				20.5	28	
-40° C				10.5	-	
R_{ON} match	Per on-resistance test condition of SW1, SW2	Magnitude R_{ON} SW1-R_{ON} SW2		0.15	0.8	

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
DC current limit						
+25° C	V_{SW} (on) = ±10 V	I_{SW}	-	225	-	mA
+85° C			80	150		
-40° C			-	400	425	
Dynamic current limit (t = <0.5 µs)	Break switches in on state, ringing switches off, apply ±1 kV at 10/1000 µs pulse, with appropriate secondary protection in place.		-	2.5	-	A
Logic input to switch output isolation						
+25° C	V_{SW} (T_{LINE}, R_{LINE}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (T_{LINE}, R_{LINE}) = ±330 V, logic inputs = gnd		-	0.3		
-40° C	V_{SW} (T_{LINE}, R_{LINE}) = ±310 V, logic inputs = gnd		-	0.1		
dv/dt sensitivity	-	-	-	200	-	V/µs

1.4.3 Ringing Return Switch, SW3

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = +260 V to -60 V	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = +270 V to -60 V			0.3		
-40° C	V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = +250 V to -60 V			0.1		
R_{ON}						
+25° C	T_{LINE} = ±0 mA, ±10 mA	R_{ON}	-	60	-	Ω
+85° C				85	100	
-40° C				45	-	
DC current limit						
+25° C	V_{SW} (on) = ± 10 V	I_{SW}	-	120	-	mA
+85° C			70	85		
-40° C			-	210		
Dynamic current limit (t = <0.5 µs)	Break switches in on state, ringing switches off, apply ±1 kV at 10/1000 µs pulse, with appropriate secondary protection in place.			2.5		A
Logic input to switch output isolation						
+25° C	V_{SW} (T_{RING}, T_{LINE}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (T_{RING}, T_{LINE}) = ±330 V, logic inputs = gnd			0.3		
-40° C	V_{SW} (T_{RING}, T_{LINE}) = ±310 V, logic inputs = gnd			0.1		

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
dv/dt sensitivity	-	-	-	200	-	V/µs

1.4.4 Ringing Switch, SW4

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -255 V to +210 V V_{SW} (differential) = +255 V to -210 V	I_{SW}	-	0.05	1	µA
+85° C	V_{SW} (differential) = -270 V to +210 V V_{SW} (differential) = +270 V to -210 V			0.1	1	
-40° C	V_{SW} (differential) = -245 V to +210 V V_{SW} (differential) = +245 V to -210 V			0.05	1	
On Voltage	I_{SW} (on) = ± 1 mA	-		1.5	3	V
Ringing generator current to ground during ringing	V_{CC} = 5 V, inputs set for ringing mode	$I_{RINGING}$		0.1	0.25	mA
On steady-state current*	Inputs set for ringing mode	I_{SW}		-	150	mA
Surge current*	-	-		-	2	A
Release current	-	-		450	-	µA
R_{ON}	I_{SW} (on) = ±70 mA, ±80 mA	R_{ON}		10	15	Ω
Logic input to switch output isolation						
+25° C	V_{SW} (R_{RING}, R_{LINE}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (R_{RING}, R_{LINE}) = ±330 V, logic inputs = gnd			0.3		
-40° C	V_{SW} (R_{RING}, R_{LINE}) = ±310 V, logic inputs = gnd			0.1		
dv/dt sensitivity	-	-		200	-	V/µs
**Secondary protection and ringing source current limiting must prevent exceeding this parameter.*						

1.4.5 $TEST_{OUT}$ Switches, SW5 and SW6

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = +260 V to -60 V	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = +260 V to -60 V			0.3		
-40° C	V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = +250 V to -60 V			0.1		
R_{ON}						
+25° C	R_{LINE} and T_{LINE} = ±10 mA, ±40 mA	R_{ON}	-	35	-	Ω
+85° C				50	70	
-40° C				26	-	
DC current limit						

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
+25° C	V_{SW} (on) = ±10 V	I_{SW}	-	140	-	mA
+85° C			80	100	-	
-40° C			-	210	250	
Dynamic current limit (t = <0.5 µs)	Break switches in on state, ringing switches off, apply ±1 kV at 10/1000 µs pulse, with appropriate secondary protection in place.		-	2.5	-	A
Logic input to switch output isolation						
+25° C	V_{SW} ($T_{TESTout}$, T_{LINE}, $R_{TESTout}$, R_{LINE}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} ($T_{TESTout}$, T_{LINE}, $R_{TESTout}$, R_{LINE}) = ±330 V, logic inputs = gnd	I_{SW}	-	0.3	1	µA
-40° C	V_{SW} ($T_{TESTout}$, T_{LINE}, $R_{TESTout}$, R_{LINE}) = ±310 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
dv/dt sensitivity	-	-		200	-	V/µs

1.4.6 Ringing Test Return Switch, SW7

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = +260 to -60 V	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = +270 V to -60 V			0.3		
-40° C	V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = +250 V to -60 V			0.1		
R_{ON}						
+25° C	$T_{RINGING}$ = ±10 mA, ±40 mA	R_{ON}	-	60	-	Ω
+85° C				85	100	
-40° C				45	-	
DC current limit						
+25° C	V_{SW} (on) = ±10 V	I_{SW}	70	120	-	mA
+85° C				80		
-40° C				210		
Logic input to switch output isolation						
+25° C	V_{SW} (T_{RING}, T_{TESTin}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (T_{RING}, T_{TESTin}) = ±330 V, logic inputs = gnd			0.3		
-40° C	V_{SW} (T_{RING}, T_{TESTin}) = ±310 V, logic inputs = gnd			0.1		
dv/dt sensitivity	-	-		200	-	V/µs

1.4.7 Ringing Test Switch, SW8

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -60 V to +175 V	I_{SW}	-	0.05	1	µA
+85° C				0.1		
-40° C				0.05		
On Voltage	$I_{SW(ON)}$ = ±1 mA	-		0.75	1.5	V
R_{ON}	$I_{SW(ON)}$ = ±70 mA, ±80 mA	R_{ON}		35	-	Ω
Release Current	-	-		450	-	µA
Logic input to switch output isolation						
+25° C	V_{SW} (R_{RING}, R_{TESTin}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (R_{RING}, R_{TESTin}) = ±330 V, logic inputs = gnd			0.3		
-40° C	V_{SW} (R_{RING}, R_{TESTin}) = ±310 V, logic inputs = gnd			0.1		
dv/dt sensitivity	-	-		200	-	V/µs

1.4.8 Test In Switches, SW9 and SW10

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Off-state leakage current						
+25° C	V_{SW} (differential) = -320 V to gnd V_{SW} (differential) = -60 V to +260 V	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (differential) = -330 V to gnd V_{SW} (differential) = -60 V to +270 V			0.3		
-40° C	V_{SW} (differential) = -310 V to gnd V_{SW} (differential) = -60 V to +250 V			0.1		
R_{ON}						
+25° C	$R_{TESTOUT}$ and $T_{TESTOUT}$ = ±10 mA, ±40 mA	R_{ON}	-	35	-	Ω
+85° C				50	70	
-40° C				26	-	
DC current limit						
+25° C	V_{SW} (on) = ±10 V	I_{SW}	-	160	-	mA
+85° C			80	110	-	
-40° C			-	210	250	
Logic input to switch output isolation						
+25° C	V_{SW} (T_{TESTin}, R_{TESTin}) = ±320 V, logic inputs = gnd	I_{SW}	-	0.1	1	µA
+85° C	V_{SW} (T_{TESTin}, R_{TESTin}) = ±330 V, logic inputs = gnd			0.3		
-40° C	V_{SW} (T_{TESTin}, R_{TESTin}) = ±310 V, logic inputs = gnd			0.1		
dv/dt sensitivity	-	-		200	-	V/µs

1.5 Additional Electrical Characteristics

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Digital input characteristics						
Input low voltage	-	V_{IL}	-	-	1.5	V
Input high voltage	-	V_{IH}	3.5	-	-	
Input leakage current (high)	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IH} = 5 V	I_{IH}	-	0.1	1	µA
Input leakage current (low)	V_{DD} = 5.5 V, V_{BAT} = -75 V, V_{IL} = 0 V	I_{IL}	-	0.1	1	
Power requirements						
Power consumption in idle/talk and all-off states	V_{DD} = 5 V, V_{BAT} = -48 V, measure I_{DD} and I_{BAT}	P	-	4.7	10.5	mW
Power consumption in ringing and access states	V_{DD} = 5 V, V_{BAT} = -48 V, measure I_{DD} and I_{BAT}	P		5.2	10.5	
V_{DD} current in idle/talk and all off states	V_{DD} = 5 V, V_{BAT} = -48 V	I_{DD}	-	0.9	2.0	mA
V_{DD} current in ringing and access states		I_{DD}	-	1.0	2.0	
V_{BAT} current in idle/talk and all off states	V_{DD} = 5V, V_{BAT} = -48 V	I_{BAT}	-	4	10	µA
V_{BAT} current in ringing and access states		I_{BAT}	-	4	10	
Temperature Shutdown Requirements (temperature shutdown flag is active low)						
Shutdown activation temperature	-	-	110	125	150	°C
Shutdown circuit hysteresis	-	-	10	-	25	°C

1.6 Protection Circuitry Electrical Specifications

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Parameters Related to the Diodes in the Diode Bridge						
Voltage drop at continuous current (50/60 Hz)	Apply ± dc current limit of break switches	Forward Voltage	-	2.8	3.5	V
Voltage drop at surge current	Apply ± dynamic current limit of break switches	Forward Voltage	-	5	-	
Parameters Related to the Protection SCR (when equipped)						
Surge current	-	-	-	-	*	A
Trigger current (+25° C)		I_{TRIG}		60	-	mA
Trigger current (+85° C)		I_{TRIG}		35	-	
Hold current (+25° C)		I_{HOLD}		110	-	
Hold current (+85° C)		I_{HOLD}	60	70	-	
Gate trigger voltage	$I_{GATE} = I_{TRIGGER}$§	-	V_{BAT} -4	-	V_{BAT} -2	V
Reverse leakage current	V_{BAT} = -48 V	-	-	-	1.0	µA
On-state voltage	0.5 A, t = 0.5 µs	V_{ON}	-	-3	-	V
	2.0 A, t = 0.5 µs	V_{ON}		-5	-	V

*Passes GR1089 and ITU-T K.20 with appropriate secondary protection in place.
§V_{BAT} must be capable of sourcing $I_{TRIGGER}$ for the internal SCR to activate.

1.7 Truth Tables

1.7.1 Truth Table for CPC7583xA and CPC7583xB

State	$IN_{RINGING}$	IN_{TESTIN}	$IN_{TESTOUT}$	Latch	T_{SD}[1]	$TEST_{IN}$ Switches	Break Switches	Ringing Test Switches	Ringing Switches	$TEST_{OUT}$ Switches
Idle/Talk	0	0	0	0	1 or Floating	Off	On	Off	Off	Off
TESTout	0	0	1			Off	Off	Off	Off	On
TESTin	0	1	0			On	Off	Off	Off	Off
Simultaneous TESTin and TESTout	0	1	1			On	Off	Off	Off	On
Ringing	1	0	0			Off	Off	Off	On	Off
Ringing Generator Test	1	1	0			Off	Off	On	Off	Off
Latched	X	X	X	1		Unchanged	Unchanged	Unchanged	Unchanged	Unchanged
All Off	1	0	1	0		Off	Off	Off	Off	Off
	1	1	1	0		Off	Off	Off	Off	Off
	X	X	X	X	0[2]	Off	Off	Off	Off	Off

[1]If T_{SD} is tied high, thermal shutdown is disabled. If T_{SD} is left floating, the thermal shutdown mechanism functions normally.
[2]Forcing T_{SD} to ground overrides the logic input pins and forces an all off state.

1.7.2 Truth Table for CPC7583xC and CPC7583xD

State	$IN_{RINGING}$	IN_{TESTIN}	$IN_{TESTOUT}$	Latch	T_{SD}[1]	$TEST_{IN}$ Switches	Break Switches	Ringing Test Switches	Ringing Switches	$TEST_{OUT}$ Switches
Idle/Talk	0	0	0	0	1 or Floating	Off	On	Off	Off	Off
TESTout	0	0	1			Off	Off	Off	Off	On
TESTin	0	1	0			On	Off	Off	Off	Off
Simultaneous TESTin and TESTout	0	1	1			On	Off	Off	Off	On
Ringing	1	0	0			Off	Off	Off	On	Off
Simultaneous TESTout and Ringing Generator Test	1	1	0			Off	Off	On	Off	On
Latched	X	X	X	1		Unchanged	Unchanged	Unchanged	Unchanged	Unchanged
All Off	1	0	1	0		Off	Off	Off	Off	Off
	X	X	X	X	0[2]	Off	Off	Off	Off	Off

[1] If T_{SD} is tied high, thermal shutdown is disabled. If T_{SD} is left floating, the thermal shutdown mechanism functions normally.

[2] Forcing T_{SD} to ground overrides the logic input pins and forces an all off state.

2. Functional Description

2.1 Introduction

The CPC7583 has the following states:

- **Idle/talk**. Loop break switches SW1, and SW2 closed, all other switches open.
- **Ringing**. Ringing switches SW3, SW4 closed, all other switches open.
- **TESTout**. Testout switches SW5, SW6 closed, all other switches open.
- **Ringing generator test**. SW7, SW8 closed, all other switches open.
- **TESTin**. Testin switches SW9 and SW10 closed.
- **Simultaneous TESTin and TESTout**. SW9, SW10, SW5, and SW6 closed, all other switches open.
- **Simultaneous test out and ringing generator test**. SW5, SW6, SW7, and SW8 closed, all other switches open (only on the xC and xD versions).
- **All Off**. All switches open.

See **"Truth Tables" on page 10** for more information.

The CPC7583 offers break-before-make and make-before-break switching with simple logic-level input control. Solid-state switch construction means no impulse noise is generated when switching during ring cadence or ring trip, eliminating the need for external zero-cross switching circuitry. State-control is via logic-level input so no additional driver circuitry is required. The line break switches SW1 and SW2 are linear switches that have exceptionally low R_{ON} and excellent matching characteristics. The ringing access switch SW4 has an open contact breakdown voltage rating of greater than 480 V. This is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition (i.e., passing the transient on to the ring generator).

Integrated into the CPC7583 is a diode bridge/SCR clamping circuit, current limiting, and a thermal shutdown mechanism to provide protection to the SLIC device during a fault condition. Positive and negative surges are reduced by the current limiting circuitry and hazardous potentials are diverted to ground via diodes and the integrated SCR. Power-cross transients are also reduced by the current limiting and thermal shutdown circuits.

To protect the CPC7583 from an overvoltage fault condition, the use of a secondary protector is required. The secondary protector must limit the voltage seen at the T_{LINE} and R_{LINE} terminals to a level below the maximum breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is recommended. With proper selection of the secondary protector, a line card using the CPC7583 will meet all relevant ITU, LSSGR, FCC and UL protection requirements.

The CPC7583 operates from a +5 V supply only. This gives the device extremely low idle and active power dissipation and allows use with virtually any range of battery voltage. A battery voltage is also used by the CPC7583 as a reference for the integrated protection circuit. In the event of a loss of battery voltage, the CPC7583 enters the all-off state.

2.2 Switch Logic

The CPC7583 provides, when switching from the ringing state to the idle/talk state, the ability to control the release timing of the ringing switches SW3 and SW4 relative to the state of the loop break switches SW1 and SW2 using simple logic-level input. This is referred to a make-before-break or break-before-make operation. When the line break switch contacts (SW1 and SW2) are closed (or made) before the ringing access switch contacts (SW3 and SW4) are opened (or broken), this is referred to make-before-break operation. Break-before-make operation occurs when the ringing access contacts (SW3 and SW4) are opened (broken) before the line break switch contacts (SW1 and SW2) are closed (made). With the CPC7583, the make-before-break and break-before-make operations can easily be selected by applying the proper sequence of logic inputs to $IN_{TESTout}$, $IN_{RINGING}$, and IN_{TESTin}.

The logic sequences for either mode of operation are given in **"Make-Before-Break Operation (Ringing to Idle/Talk Transition)" on page 13** and **"Break-Before-Make Operation (Ringing to Idle/Talk Transition)" on page 13**. Logic states and explanations are given in **"Truth Tables" on page 10**.

Break-before-make operation can also be achieved using pin 13 (T_{SD}) as an input. In **"Break-Before-Make Operation (Ringing to Idle/Talk Transition)" on page 13**, lines 2 and 3, it is possible to induce the switches to the all-off state by grounding pin 13 (T_{SD}) instead of applying logic input to the pins. This has the effect of overriding the logic inputs and forcing the device to the all-off state. Hold this input state for 25 ms. During this hold period, toggle the inputs from the ringing state to the idle/talk state. After the 25 ms, release pin 13

(T_{SD}) to return switch control to the input pins $IN_{TEST-out}$, $IN_{RINGING}$, and IN_{TESTin} and the latch control pin.

2.2.1 Make-Before-Break Operation (Ringing to Idle/Talk Transition)

State	$IN_{RINGING}$	IN_{TESTIN}	$IN_{TESTOUT}$	Latch	T_{SD}	Timing	Break Switches 1 and 2	Ring Return Switch 3	Ring Access Switch 4	All Other Test Switches
Ringing	1	0	0	0	Floating	-	Off	On	On	Off
Make-before-break	0	0	0		Floating	SW4 waiting for next zero-current crossing to turn off. Maximum time is one-half of ringing. In this transition state, current that is limited to the dc break switch current limit value will be sourced from the ring node of the SLIC.	On	Off	On	Off
Idle/Talk	0	0	0		Floating	Zero-cross current has occurred	On	Off	Off	Off

2.2.2 Break-Before-Make Operation (Ringing to Idle/Talk Transition)

State	$IN_{RINGING}$	IN_{TESTIN}	$IN_{TESTOUT}$	Latch	T_{SD}	Timing	Break Switches 1 and 2	Ring Return Switch 3	Ring Access Switch 4	All Other Test Switches
Ringing	1	0	0	0	Floating	-	Off	On	On	Off
All off	1	0	1		Floating	Hold this state for one-half of ringing cycle. SW4 waiting for zero current to turn off.	Off	Off	On	Off
All off	1	0	1		Floating	Zero current has occurred. SW4 has opened	Off	Off	Off	Off
Idle/Talk	0	0	0		Floating	Release break switches	On	Off	Off	Off

2.3 Alternate Break-Before-Make Operation

Note that break-before-make operation can also be achieved using T_{SD} as an input. In lines 2 and 3 of the table **"Break-Before-Make Operation (Ringing to Idle/Talk Transition)" on page 13**, instead of using the logic input pins to force the all-off state, force T_{SD} to ground. This overrides the logic inputs and also forces the all off state. Hold this state for one-half of the ringing cycle. During this 25 ms all-off state, change the inputs from the power ringing state (IN_{RING} = 1, IN_{TESTIN} = 0, $IN_{TESTOUT}$ = 0) to the idle/talk state (IN_{RING} = 0, IN_{TESTIN} = 0, $IN_{TESTOUT}$ = 0). After the hold period, release T_{SD} to return switch control to the input pins which will set the idle talk state.

When using the CPC7583 in this mode, forcing T_{SD} low overrides the input pins and forces an all off state. Setting T_{SD} high allows switch control via the logic input pins and returns the thermal protection circuit to normal operation. Forcing T_{SD} high disables the thermal shutdown mechanism and is not recommended. Therefore, to allow switch control via the logic input pins, allow T_{SD} to float.

When using T_{SD} as an input, the two recommended states are 0 (overrides logic input pins and forces all off state) and float (allows switch control via logic input pins and the thermal shutdown mechanism is active). This requires the use of an open-collector type buffer.

2.4 Data Latch

The CPC7583 has an integrated data latch. The latch operation is controlled by logic-level input pin 18 (LATCH). The data input of the latch are the input pins, while the output of the data latch is an internal node used for state control. When the LATCH control pin is at logic 0, the data latch is transparent and data

control signals flow directly through to state control. A change in input will be reflected in a change is switch state. When LATCH control pin is at logic 1, the data latch is active and a change in input control will not affect switch state. The switches will remain in the position they were in when the LATCH changed from logic 0 to logic 1 and will not respond to changes in input as long as the latch is at logic 1. The T_{SD} input is not tied to the data latch. Therefore, T_{SD} is not affected by the LATCH input and the T_{SD} input will override state control via the inputs.

2.5 T_{SD}

Setting T_{SD} to +5 V allows switch control using the logic inputs. This setting, however, also disables the thermal shutdown circuit and is therefore not recommended. When using logic controls via the input pins, pin 13 (T_{SD}) should be allowed to float. As a result, the two recommended states when using pin 13 (T_{SD}) as a control are 0, which forces the device to the all-off state, or float, which allows logic inputs to remain active. This requires the use of an open-collector type buffer.

2.6 Ringing Switch Zero-Cross Current Turn Off

After the application of a logic input to turn SW4 off, the ringing switch is designed to delay the change in state until the next zero-crossing. Once on, the switch requires a zero-current cross to turn off, and therefore should not be used to switch a pure DC signal. The switch will remain in the on state no matter the logic input until the next zero crossing. These switching characteristics will reduce and possibly eliminate overall system impulse noise normally associated with ringing switches. See Clare application note **AN-144, Impulse Noise Benefits of Line Card Access Switches** for more information. The attributes of ringing switch SW4 may make it possible to eliminate the need for a zero-cross switching scheme. A minimum impedance of 300 Ω in series with the ringing generator is recommended.

2.7 Power Supplies

Both a +5 V supply and battery voltage are connected to the CPC7583. CPC7583 switch state control is powered exclusively by the +5 V supply. As a result, the CPC7583 exhibits extremely low power dissipation during both active and idle states.

The battery voltage is not used for switch control but rather as a supply for the integrated secondary protection circuitry. The integrated SCR is designed to trigger when pin 6 (T_{BAT}) or pin 23 (R_{BAT}) drops 2 to 4 V below the voltage on pin 28 (V_{BAT}). This trigger prevents a fault induced overvoltage event at the T_{BAT} or R_{BAT} nodes.

2.8 Battery Voltage Monitor

The CPC7583 also uses the V_{BAT} voltage to monitor battery voltage. If battery voltage is lost, the CPC7583 immediately enters the all-off state. It remains in this state until the battery voltage is restored. The device also enters the all-off state if the battery voltage rises above –10 V and remains in the all-off state until the battery voltage drops below –15 V. This battery monitor feature draws a small current from the battery (less than 1 µA typical) and will add slightly to the device's overall power dissipation.

2.9 Protection

2.9.1 Diode Bridge/SCR

The CPC7583 uses a combination of current limited break switches, a diode bridge/SCR clamping circuit, and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events such as lightning. During a positive transient condition, the fault current is conducted through the diode bridge to ground via F_{GND}. Voltage is clamped to a diode drop above ground. During a negative transient of 2 to 4 V more negative than the voltage at V_{BAT}, the SCR conducts and faults are shunted to F_{GND} via the SCR and diode bridge.

In order for the SCR to crowbar or foldback, the on voltage (see **"Protection Circuitry Electrical Specifications" on page 10**) of the SCR must be less negative than the V_{BAT} voltage. If the V_{BAT} voltage is less negative the T_{LINE} and R_{LINE} voltage, or if the V_{BAT} supply is unable to source the trigger current, the SCR will not crowbar, however it will conduct fault currents to ground.

For power induction or power-cross fault conditions, the positive cycle of the transient is clamped to a diode drop above ground and the fault current directed to ground. The negative cycle of the transient will cause the SCR to conduct when the voltage exceeds the battery reference voltage by two to four volts, steering the current to ground.

2.9.2 Current Limiting function

If a lightning strike transient occurs when the device in the talk/idle state, the current is passed along the line to the integrated protection circuitry and restricted by

the dynamic current limit response of break switches SW1 and SW2. When a 1000V 10/1000 µS pulse (GR-1089-CORE lightning) is applied to the line though a properly clamped external protector, the current seen at pin 6 (T_{BAT}) or pin 23 (R_{BAT}) will be a pulse with a typical magnitude of 2.5 A and a duration of less than 0.5 µs.

If a power-cross fault occurs with the device in the talk/idle state, the current is passed though break switches SW1 and SW2 on to the integrated protection circuit and is limited by the dynamic DC current limit response of the two break switches. The DC current limit, specified over temperature, is between 80 mA and 425 mA, and the circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to power cross fault, the measured current at pin 6 (T_{BAT}) or pin 23 (R_{BAT}) will decrease as the device temperature increases. If the device temperature rises sufficiently, the temperature shutdown mechanism will activate and the device will default to the all-off state.

2.10 Temperature Shutdown

The thermal shutdown mechanism will activate when the device temperature reaches a minimum of 110° C, placing the device in the all-off state regardless of logic input. During thermal shutdown mode, pin 13 (T_{SD}) will read 0 V. Normal output of T_{SD} is +5 V.

If presented with a short duration transient such as a lightning event, the thermal shutdown feature will typically not activate. But in an extended power-cross transient, the device temperature will rise and the thermal shutdown will activate forcing the switches to the all-off state. At this point the current measured at pin 6 (T_{BAT}) and pin 23 (R_{BAT}) will drop to zero. Once the device enters thermal shutdown it will remain in the all-off state until the temperature of the device drops below the activation level of the thermal shutdown circuit. This will permit the device to return to normal operation. If the transient has not passed, current will flow up to the value allowed by the dynamic DC current limiting of the switches and heating will begin again, reactivating the thermal shutdown mechanism. This cycle of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector could activate and shunt all current to ground.

The thermal shutdown mechanism of the CPC7583 can be disabled by applying a logic 1 to pin 13 (T_{SD}).

2.11 External Protection Elements

The CPC7583 requires only overvoltage secondary protection on the loop side of the device. The integrated protection feature described above negates the need for protection on the line side. The secondary protector limits voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7583. A foldback or crowbar type protector is recommended to minimize stresses on the device.

Consult Clare's application note, AN-100, "Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces" for equations related to the specifications of external secondary protectors, fused resistors and PTCs.

3. Manufacturing Information

3.1 Soldering

3.1.1 Moisture Reflow Sensitivity

Clare has characterized the moisture reflow sensitivity of LCAS products using IPC/JEDEC standard J-STD-020A. Moisture uptake from atmospheric humidity occurs by diffusion. During the solder reflow process, in which the component is attached to the PCB, the whole body of the component is exposed to high process temperatures. The combination of moisture uptake and high reflow soldering temperatures may lead to moisture induced delamination and cracking of the component. To prevent this, this component must be handled in accordance with IPC/JEDEC standard J-STD-020A per the labelled moisture sensitivity level (MSL), level 1 for the SOIC package, and level 3 for the MLP package.

3.1.2 Reflow Profile

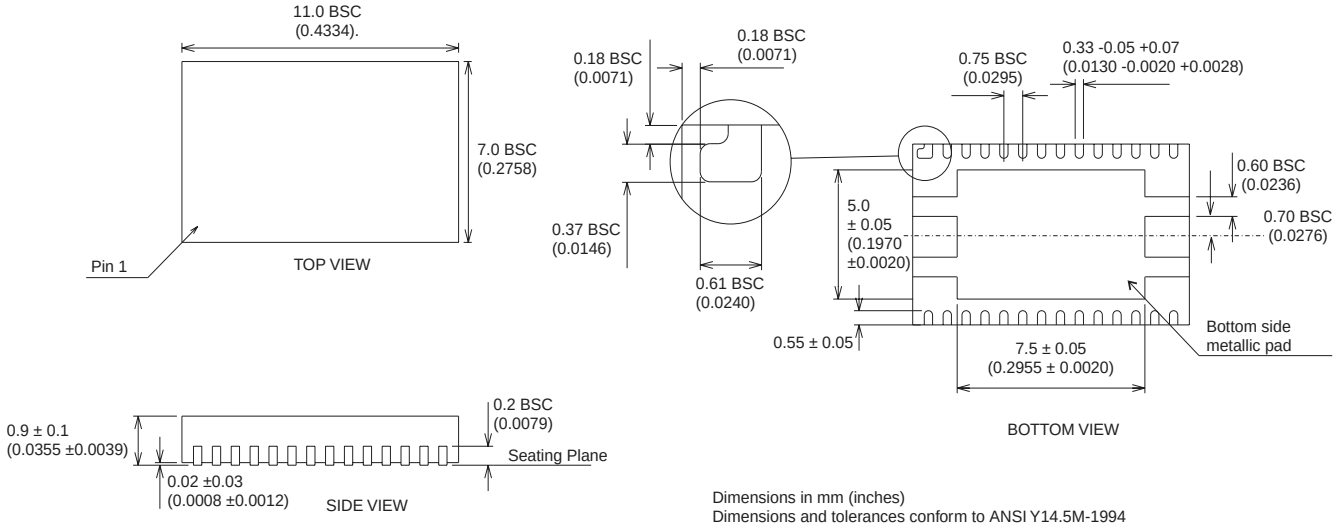
The maximum ramp rates, dwell times, and temperatures of the assembly reflow profile should not exceed those specified in IPC standard IPC-9502, table 2. Soldering processes are limited to 220 °C component body temperature.

3.2 Washing

Clare does not recommend ultrasonic cleaning of LCAS parts.

3.3 Mechanical Dimensions

3.3.1 MLP Package

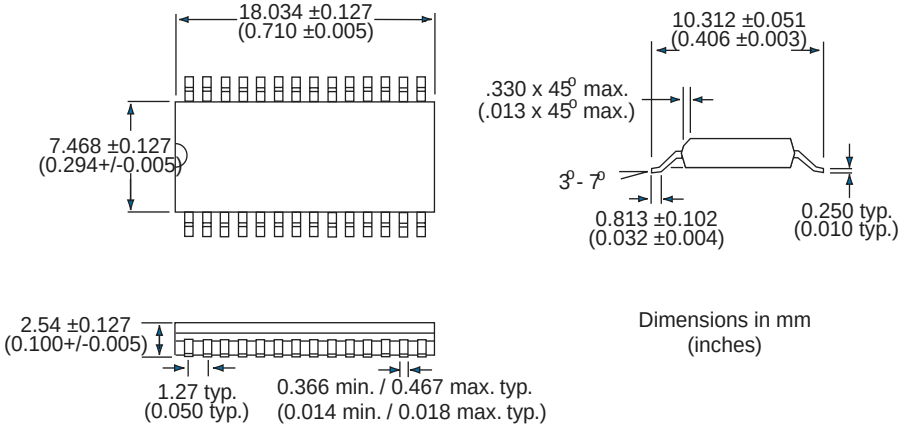


Dimensions in mm (inches)
Dimensions and tolerances conform to ANSI Y14.5M-1994

NOTE: For optimum solder joint size, MLP package printed-circuit board pads should extend no more than .05 mm past the chip post on the short sides, and no more than .025 mm past the chip posts on the long sides.

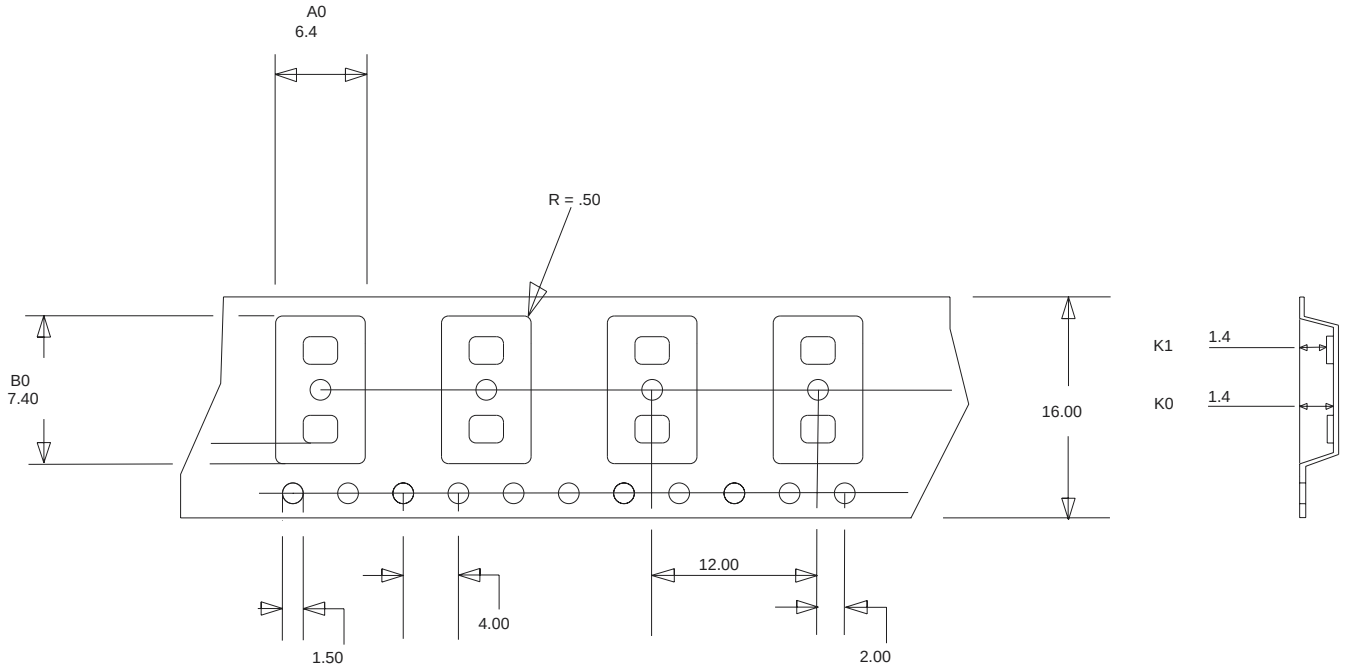
As the metallic pad on the bottom of the MLP package is connected to the substrate of the die, Clare recommends that no printed circuit board to traces cross this area to maintain minimum creepage and clearance values.

3.3.2 SOIC Package



Dimensions in mm
(inches)

3.3.3 MLP Tape Dimensions



A0 =	6.4 mm
B0 =	7.4 mm
K0 =	1.4 mm
K1 =	1.4 mm

NOTES:1. ALL DIMENSIONS ARE IN MILLIMETERS AND CARRY TOLERANCES OF EIA STANDARD 481-2. 2. THE TAPE COMPLIES WITH ALL "NOTES" FOR CONSTANT DIMENSIONS LISTED ON PAGE 5 OF EIA-481-2.

For additional information please visit www.clare.com

Specification: DS-CPC7583-R 2.0

9/16/2002