To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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M61283FP

NTSC TV Signal Processor

REJ03F0054-0100Z
Rev.1.0
Sep.23.2003

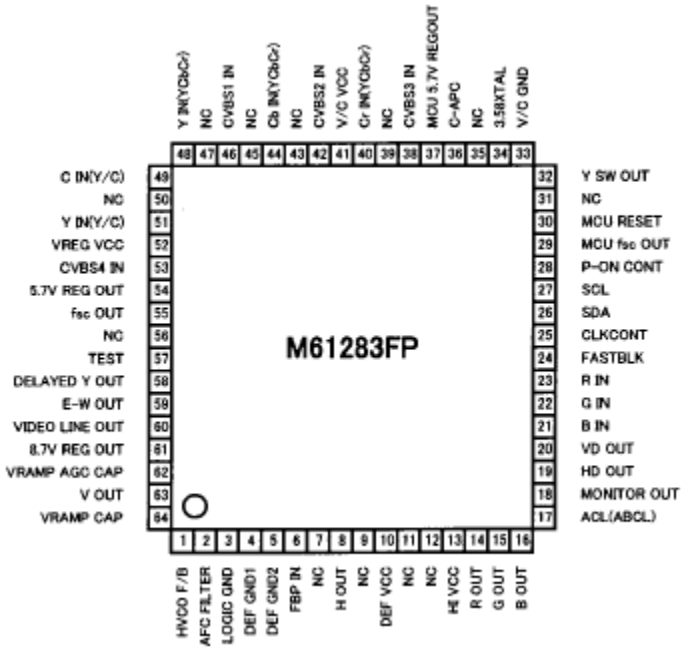
Features

- 4 line composite video signal, 1 line S video signal and 1 line component video signal inputs are available
- Built-in input video switch with Y/C mixing output
- Built-in high speed switch for component video signal
- East-West geometry output
- VM (Delayed Y) output
- H output of open corrector type (H at stopping)
- Selectable of ACL/ABCL
- Built-in H OSC resonator
- Built-in vertical saw tooth generator
- Various signal output for intelligent monitoring function
- Correspond to fsc clock output
- H & V pulse output for OSD
- Built-in 5V & 8V regulator
- Built-in MCU reset circuit
- Variable function of BLK width for 16:9 screen

Applications

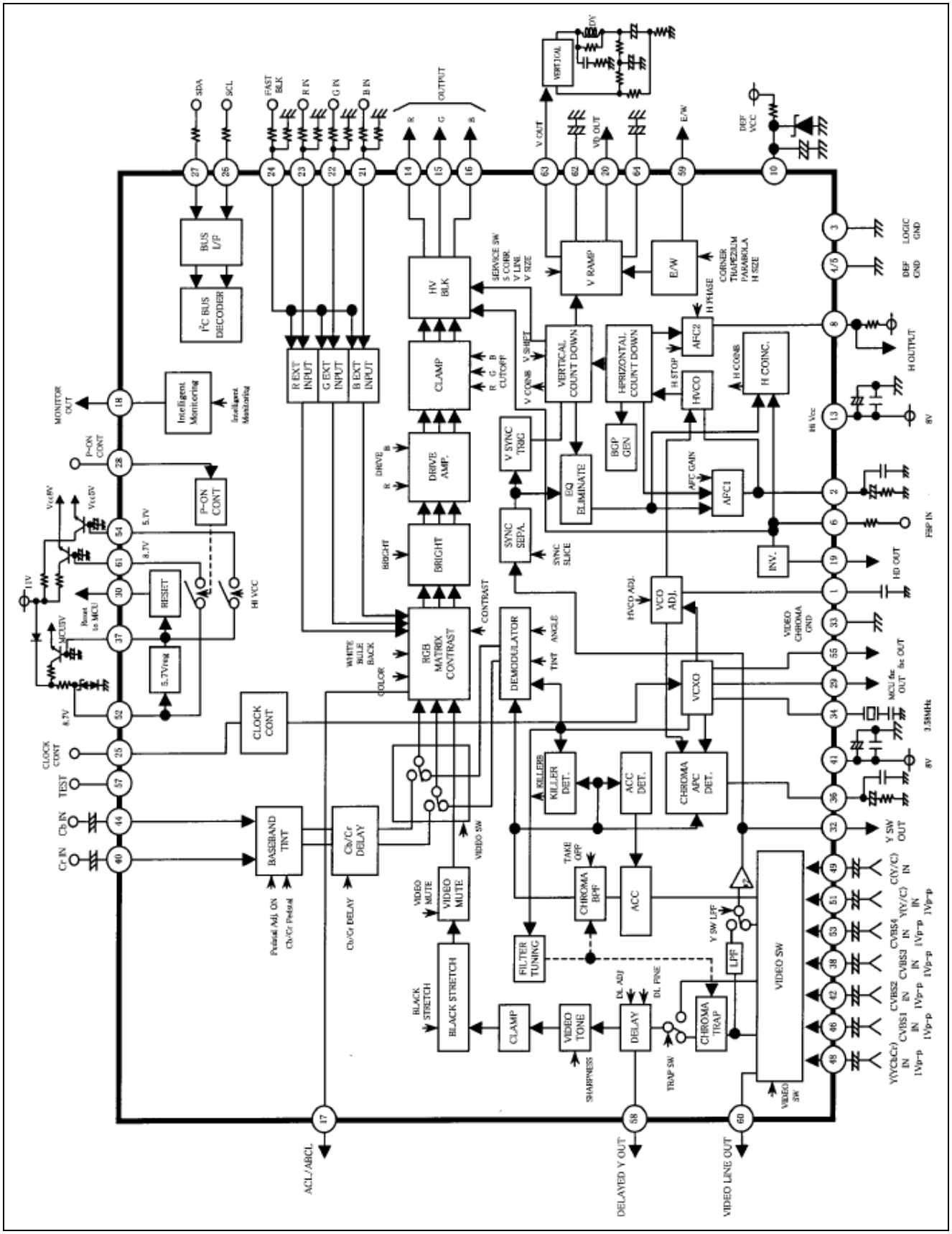
- NTSC color television receivers

Pin Configuration



Package: 64P6U

Block Diagram



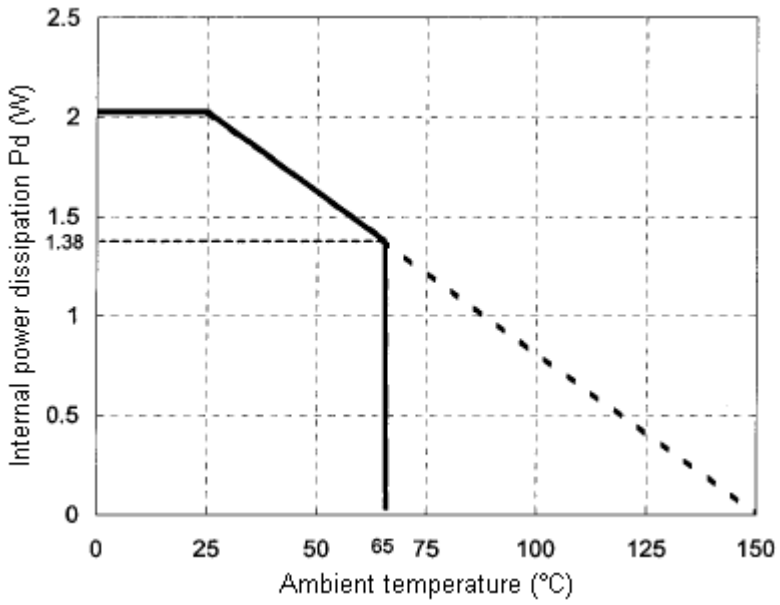
Absolute Maximum Ratings

Item	Symbol	Condition	Ratings	Unit
Power supply voltage	Vcc		6.0, 10.0	V
Power dissipation	Pd	Ta = 25°C	2026	mW
Thermal reduction	Kt		16.2	mW/°C
Operating ambient temperature	Topr		–10 to 65	°C
Storage temperature	Tstg		–40 to 125	°C

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage1 (Pin41)	Vcc1	4.75	5.0	5.25	V
Power supply voltage2 (Pin10)	Vcc2	7.6	8.0	8.4	V
Power supply voltage3 (Pin13)	Vcc3	7.6	8.0	8.4	V
Power supply voltage4 (Pin52)	Vcc4	8.3	8.7	9.1	V

Thermal Derating (Maximum Rating)



I²C Bus Table

1. Slave Address = BAH (WRITE), BBH (READ)

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	1	1	1	0	1	1/0

2. Write Table (input bytes)

SUB ADDRESS		DATA								INITIAL	
HEX	BIN	D7	D6	D5	D4	D3	D2	D1	D0	HEX	DEC
00H	00000000	OSD Clip Off	Contrast Control								
		V0	V1	V0	V0	V0	V0	V0	V0	40H	64
01H	00000001	Brightness Control									
		V1	V0	V0	V0	V0	V0	V0	V0	80H	128
02H	00000010	Force Mono	Drive(R)								
		0	1	0	0	0	0	0	0	40H	64
03H	00000011	White Back	Drive(B)								
		0	1	0	0	0	0	0	0	40H	64
04H	00000100	Cut Off(R)									
		1	0	0	0	0	0	0	0	80H	128
05H	00000101	Cut Off(G)									
		1	0	0	0	0	0	0	0	80H	128
06H	00000110	Cut Off(B)									
		1	0	0	0	0	0	0	0	80H	128
07H	00000111	ACL Off	Fsc Free	ABCL	ABCL Gain	C-Trap Off	H Tone	Killer Level	Take Off		
		0	0	0	0	0	0	0	0	00H	0
08H	00001000	BGP FBP Off	Tint Control								
		0	V1	V0	V0	V0	V0	V0	V0	40H	64
09H	00001001	Blue Back	Color Control								
		V0	V1	V0	V0	V0	V0	V0	V0	40H	64
0AH	00001010	Video Mute	HV Blk Off	Video Tone							
		0	0	V1	V0	V0	V0	V0	V0	20H	32
0BH	00001011	Black Stre. Off	Black Stretch Cont			Fast Blk H	TEST	CVBS SW			
		0	0	0	0	0	V0	V0	V0	00H	0
0CH	00001100	V.TWidow	Matrix Control		C.Angle 95	Y SW LPF	Y DL Fine Adj	Y DL Time Adj			
		0	0	0	0	0	0	0	0	00H	0
0DH	00001101	Service SW	Slice Det Down	S.Slice Down		V Blk Half	V Shift				
		0	1	0	0	0	0	0	0	40H	64
0EH	00001110	TEST	V Free	V Size							
		0	0	1	0	0	0	0	0	20H	32
0FH	00001111	H Start	H Free	Not Assigned	AFC2 Gain Down	AFC2 H Phase					
		0	0	0	0	1	0	0	0	08H	8
10H	00010000	TEST	TEST	TEST	V Blk Wide	V Blk Wide Top		V Blk Wide Bottom			
		0	0	0	0	0	0	0	0	00H	0
11H	00010001	Monitoring				TEST	Internal FBP	Video SW			
		0	0	0	0	0	0	0	0	00H	0
12H	00010010	TEST	TEST	TEST		Vsync Det Time	AFC1 Gain				
		0	0	0	0	0	1	0	0	04H	4
13H	00000110	TEST	Baseband Tint Control								
		0	V1	V0	V0	V0	V0	V0	V0	40H	64
14H	00000111	TEST	TEST	Cb Delay Fine Adj		Cb Pedestal Adj					
		0	0	0	0	1	0	0	0	08H	64
15H	00001000	CTI	CbCr Pedestal Adj On	Cr Delay Fine Adj		Cr Pedestal Adj					
		0	0	0	0	1	0	0	0	08H	8
16H	00001001	DL Y Adj		V S-Correction							
		0	0	1	0	0	0	0	0	20H	32
17H	00001010	DL Y On	V AGC	V Linearity							
		0	1	1	0	0	0	0	0	A0H	96
18H	00001011	Y GAMMA		E/W Parabola							
		0	0	1	0	0	0	0	0	20H	32
19H	00001100	Not Assigned	Not Assigned	E/W Corner							
		0	0	1	0	0	0	0	0	20H	32
1AH	00001101	Not Assigned	Not Assigned	E/W Trapezium							
		0	0	1	0	0	0	0	0	20H	32
1BH	00001110	Not Assigned	Not Assigned	E/W H Size							
		0	0	1	0	0	0	0	0	20H	32
1CH	00001111	TEST		ANA OSD	TEST	TEST	H VCO Adj				
		0	0	0	1	0	1	0	0	14H	20
1DH	00010000	TEST 1	TEST 0	TEST On	TEST	Black Discharge2	Force Color	C-Trap Adj			
		0	0	0	0	0	0	0	0	00H	0
1EH	00010001	TEST	TEST	OSD Clip Level		TEST	C-Sync Adj				
		0	0	0	0	0	0	0	0	08H	0
1FH	00010010	TEST	TEST	TEST	TEST	OSD Bright	TEST	Video Line Out SW			
		0	0	0	0	0	0	0	0	04H	0

NOTE: V0/V1->V-LATCH BIT

If it needs to write any data on TEST bit, the initial data : 0 is requested.

3. Read Table (output byts)

D7	D6	D5	D4	D3	D2	D1	D0
KILLERB	2WIN WIDEB	VFREEB	VCOINB	0	1	HCOINB	1

4. Bus Functions

- Write

	Function	Bit	Sub Add	DATA	Discription	Note
Video	Video Tone	6	0AH	D5-D0	Sharpness level control	V Latch
	Contrast Control	7	00H	D6-D0	Contrast level control	V Latch
	Y DL Time Adj	2	0CH	D1-D0	Y signal delay adjustment	
	Y DL Fine Adj	1	0CH	D2	Y signal delay fine adjustment	
	CVBS SW	2	0BH	D1-D0	CVBS input select; 0: pin 46, 1: pin 42, 2: pin 38, 3: pin 53	V Latch
	Vidio SW	2	11H	D1-D0	Video switch select; 0: CVBS mode, 1: Y/C mode, 2: YcbCr mode, 3: CVBS mode	
	Video Line Out SW	2	1FH	D1-D0	Video Line output select; 0: CVBS SW output, 1: Y/C mix output, 2: Video SW output, 3: mute	
	Y SW LPF	1	0CH	D3	Pin 14 (Y SW OUT) output f-characteristic switching; 0: flat, 1: LPF (fc = 700 kHz)	
	Vidio Mute	1	0AH	D7	Y signal output on/off (mute) switching; 0: mute off, 1: mute	
	TRAP Off	1	07H	D3	Y signal chroma trap on/off switching; 0: trap on, 1: trap off	
	C-TRAP Adj	2	1DH	D1-D0	Chroma trap frequency fine adjust	
	Black Stretch Off	1	0BH	D7	Black stretch circuit on/off switching; 0: black stretch on, 1: black stretch off	
	Black Stretch Cont	3	0BH	D6-D4	Black stretch charge, discharge time constant adjustment; D4, D5: charge time constant adjustment; D6: discharge time constant adjustment	
	DL Y On	1	17H	D7	S-VM Y signal output on/off; 0: off, 1: on	
	DL Y Adj	2	16H	D7-D6	S-VM Y signal output delay fine adjustment	
CHROMA	Tint Control	7	08H	D6-D0	Hue control	V Latch
	Color Control	7	09H	D6-D0	Color level control	V Latch
	Take Off	1	07H	D0	Chroma BPF take-off function on/off switching; 0: BPF; 1: take off	
	C Angle95	1	0CH	D4	Color demodulation angle switching; 0: 103 deg, 1: 95 deg	
	Killer Level	1	07H	D1	Colorkiller sensitivity switching; 0: 41 dB, 1: 34 dB	
	Force Mono	1	02H	D7	Forced b/w mode; 0: normal; 1: b/w	
	Force Color	1	1DH	D2	Forced color mode; 0: normal; 1: color	
	Fsc Free	1	07H	D6	Crystal oscillation circuit forced free-running mode; 0: off, 1: free-running	
	CTI(Color Tras Improvement	1	15H	D7	Color difference signal (R-Y) delay time adjustment; 0: normal, 1: fast	
	Baseband Tint Control	7	13H	D6-D0	Hue adjustment for color difference input	V Latch
	Cbcr Pedestal Adj On	1	15H	D6	Pedestal adjustment ON/OFF during color difference input; 0: on, 1: off	
	Cb Pedestal Fine Adj	4	14H	D3-D0	Pedestal level fine adjustment for Cb input signal	
	Cr Pedestal Fine Adj	4	15H	D3-D0	Pedestal level fine adjustment for Cr input signal	
	CbDL Fine Adj	2	14H	D5-D4	Cb signal delay time fine adjustment	
	CrDL Fine Adj	2	15H	D5-D4	Cr signal delay time fine adjustment	
RGB	Brightness Control	8	01H	D7-D0	Bright level control	V Latch
	Drive (R)	7	02H	D6-D0	R output level control	
	Drive (B)	7	03H	D6-D0	B output level control	
	Cut Off (R)	8	04H	D7-D0	R output DC level control	
	Cut Off (G)	8	05H	D7-D0	G output DC level control	
	Cut Off (B)	8	06H	D7-D0	B output DC level control	
	Blue Back	1	09H	D7	Blue back screen on/off switching; 0: off, 1: blue back	
	WhiteBack	1	03H	D7	White raster on/off switching; 0: off, 1: white back	
	ABCL	1	07H	D5	ABCL on/off switching; 0: off, 1: ABCL on	
	ABCL Gain	1	07H	D4	ABCL sensitivity low/high switching; 0: low, 1: hi	
	ACL OFF	1	07H	D7	ACL on/off switching; 0: normal, 1: ACL max	
	ANA OSD	1	1CH	D5	Analog/digital OSD switching; 0: digital, 1: analog	
	OSD Clip Off	1	00H	D7	EXT RGB contrast limit value clipping switch; 0: clipping on, 1: clipping off	V Latch

- Write (cont.)

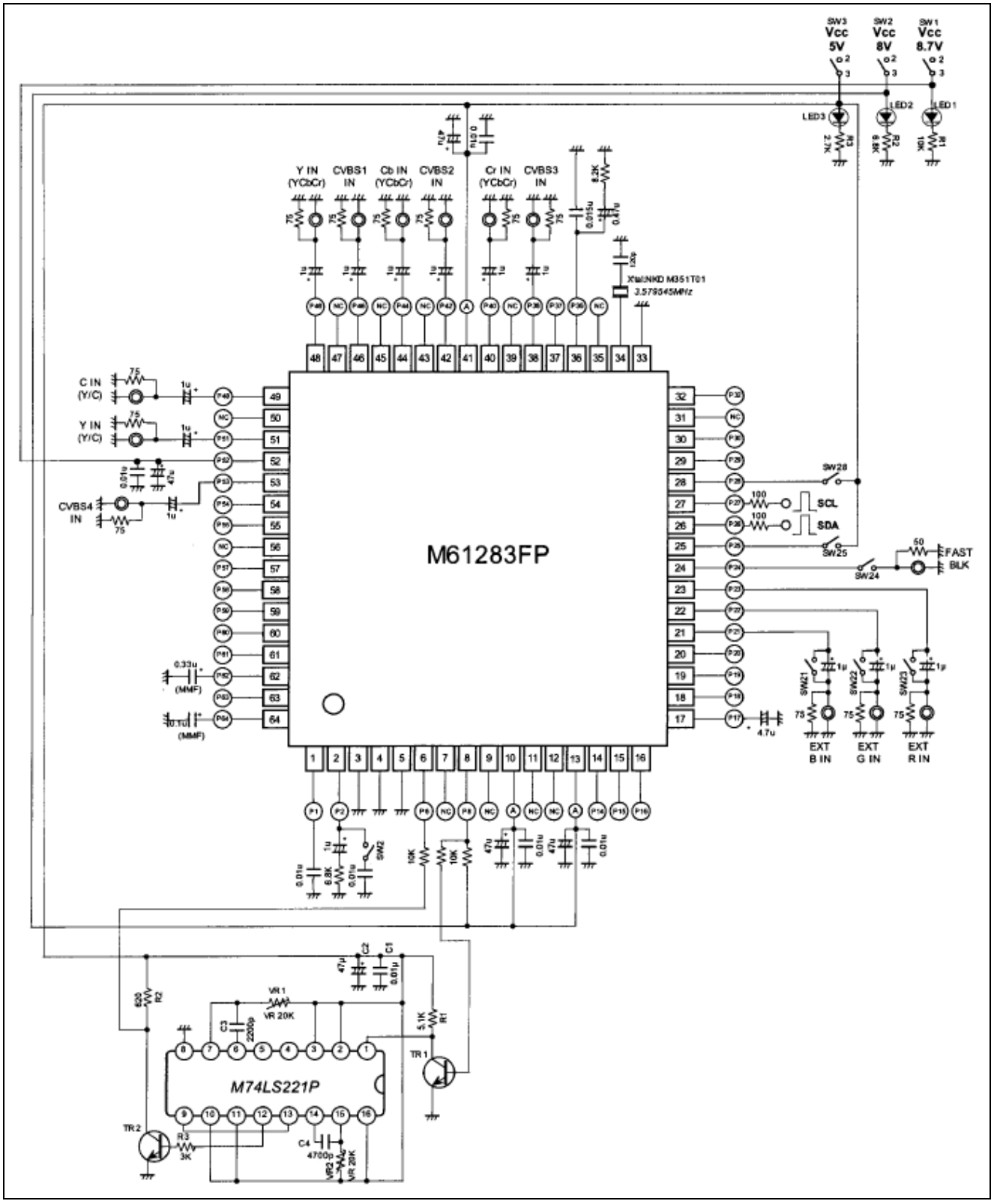
	Function	Bit	Sub Add	DATA	Discription	Note
RGB	OSD Clip Level	2	1EH	D5-D4	EXT RGB contrast limit value change; 0: 63, 1: 95, 2: 127, 3: 127	
	HTONE	1	07H	D2	Halftone on/off switching; 0: normal, 1: halftone	
	Matrix Control	2	0CH	D6-D5	Matrix control; 0: normal, 1: G-Y 10% up, 2: R-Y 5% down, 3: R-Y 5% down, G-Y 10% up	
	HV BLK OFF	1	0AH	D6	RGB HV blanking switch; 0: blanking enabled 1: blanking disabled	
	V BLK HALF	1	0DH	D3	When used for under-scanning; 0: normal, 1: hide half line	
	FASTBLK Hi	1	0BH	D3	FASTBLK switching; 0: normal, 1: hi (full-screen OSD mode)	
	OSD Bright	1	1FH	D3	OSD level switching; 0: normal, 1: –12%	
DEF	AFC2 H Phase	4	0FH	D3-D0	Screen horizontal position adjustment	
	V Out Stop	1	0EH	D7	Pin 38 VOUT (ramp) forced stop mode (when stopped, pin 38 at DC GND level); 0: VOUT, 1: STOP	
	Service SW	1	0DH	D7	Vertical output on/off switching; 0: vertical output on, 1: vertical output off	
	H Start	1	0FH	D7	Horizontal output out/stop switching; 0: stop, 1: H out	
	AFC1 Gain	3	12H	D2-D0	Horizontal AFC gain adjustment; 000: low to 111: hi	
	AFC2 Gain Down	1	0FH	D4	Horizontal AFC2 gain high/low switching; 0: high, 1: low	
	H VCO Adj	3	1CH	D2-D0	H VCO free-running frequency adjustment	
	V Shift	3	0DH	D2-D0	Vertical ramp start timing adjustment	
	V-Size	6	0EH	D5-D0	Vertical ramp amplitude adjustment	
	H-free	1	0FH	D6	Horizontal output forced free-running mode on/off switching; 0: off, 1: horizontal free-running	
	V-free	1	0EH	D6	Vertical output forced free-running mode on/off switching; 0: off, 1: vertical free-running	
	S Slice Down	2	0DH	D5-D4	Sync detection slice level switching (0: 65%, 1: 40%, 2: 55%, 3: 35%)	
	Slice Det Down	1	0DH	D6	0: normal, 1: lower sync detection sensitivity	
	V SYNC DET TIME	1	12H	D3	Vertical minimum sync detection width switching; 0: sync detect width =18 μs, 1: sync detect width =14 μs	
	V1 Window	1	0CH	D7	Vertical sync detection switching (1 window/2 windows); 0: 2 windows, 1: 1 window	
	BGPFBP OFF	1	08H	D7	Internal BGP on/off switching when no FBP input; 0: BGP on, 1: BGP off	
	C-SYNC Adj	3	1EH	D0-D2	C-sync output LPF cutoff frequency adjustment	
	V AGC	1	17H	D6	V RAMP AGC speed adjustment; 0: slow, 1: fast (increase AGC speed by five)	
	E/W Parabola	6	18H	D5-D0	Parabola adjustment	
	E/W Corner	6	19H	D5-D0	Corner pin adjustment	
	E/W Trapezium	6	1AH	D5-D0	Trapezium correction adjustment	
	E/W H Size	6	1BH	D5-D0	Horizontal size adjustment	
	V S-Correction	6	16H	D5-D0	Vertical S-pattern correction adjustment	
	V Linearity	6	17H	D5-D0	Vertical linearity adjustment	
	V Blk Wide Bottom	2	10H	D1D0	Screen bottom blanking adjustment (at VBLK WIDE = 1 only)	
	V Blk Wide Top	2	10H	D3D2	Screen top blanking adjustment (at VBLK WIDE = 1 only)	
	V Blk Wide	1	10H	D4	V BLK WIDE mode switching; 0: normal, 1 WIDE mode	
	Monitoring	4	11H	D7-D4	Pin 18 intelligent monitor mode switching	

- Read

HCONB	1	00H	D1	Horizontal sync detection; "1" when asynchronous
—	1	00H	D2	1
—	1	00H	D3	0
VCOINB	1	00H	D4	Vertical sync detection; "1" when asynchronous
VFREEB	1	00H	D5	V free-running mode; 0: V free-running, 1: V lock
2WIN WIDEB	1	00H	D6	Vertical 2-window detection; 0: wide window, 1: narrow window
KILLERB	1	00H	D7	Colorkiller information output; 0: killer on, 1: killer off

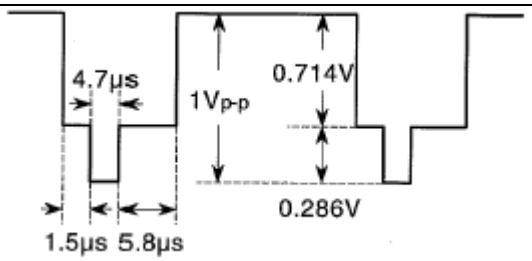
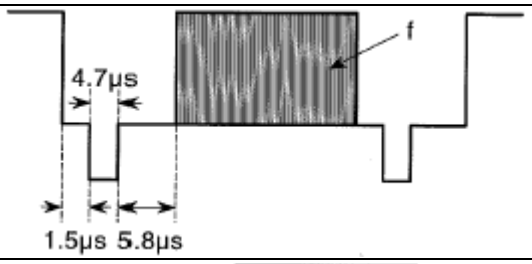
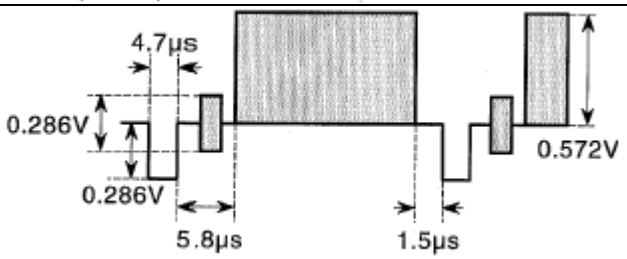
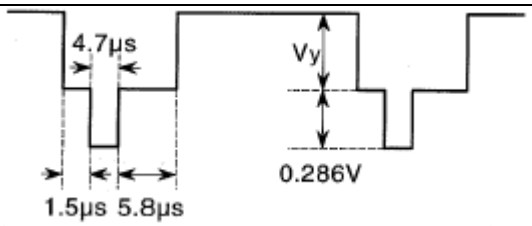
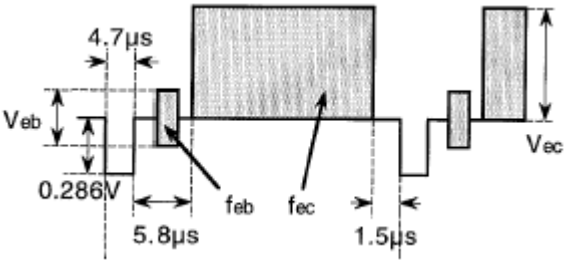
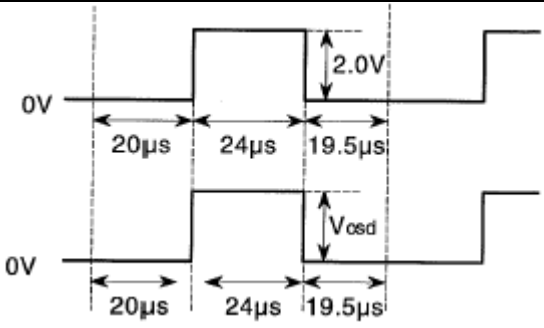
Note: Functions not listed in this bus function table are used only in testing, and operation is not guaranteed.

Test Circuit

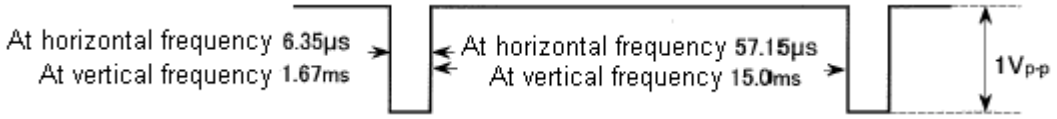
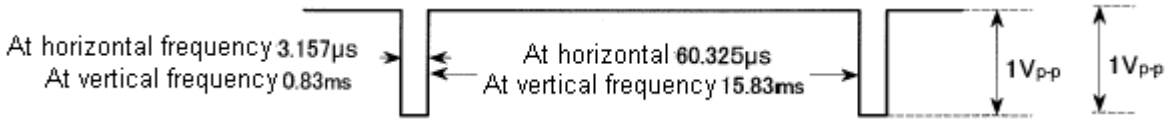
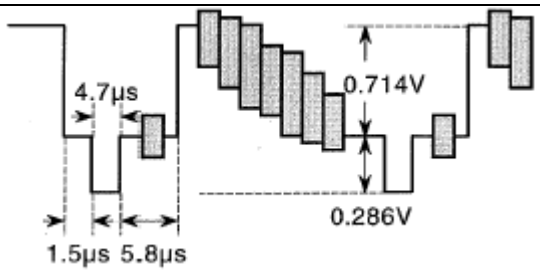
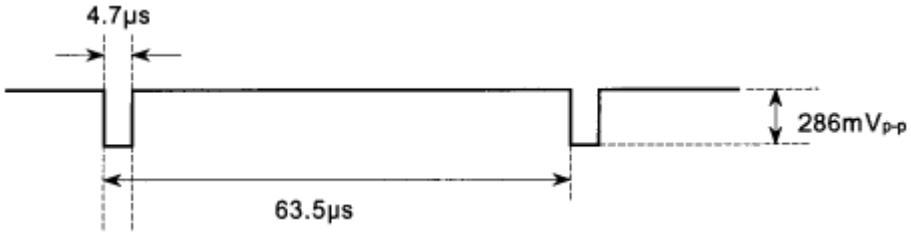
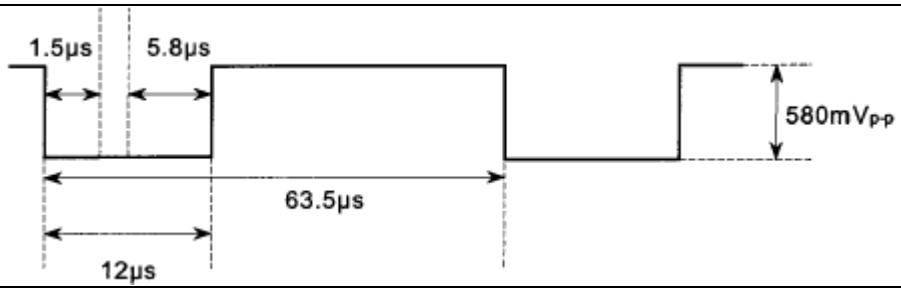


Input Signals

Video/Chroma/RGB/DEF Block

SG No.	Signal Description (75 Ω termination)	
SG. A	NTSC format APL 100% standard video signal. Vertical signal is interlaced at 60 Hz.	
SG. B	In the SG.A signal, the Lumi. signal frequency and amplitude can be changed. However, standard amplitude is 0.714 Vp-p. In the figure on the right, the Lumi. signal is represented by f.	
SG. C	NTSC standard monochrome video signal. Vertical signal is interlaced at 60 Hz.	
SG. D	NTSC format video signal; APL variable. Vertical signal is interlaced at 60 Hz.	
SG. E	NTSC format monochrome video signal. In the SG.C signal, the burst and chroma part frequency and amplitude can be changed. Vertical signal is interlaced at 60 Hz. (Standard state: Veb = 0.286 V, Vec = 0.572 V, feb = fec = 3.579545 MHz)	
SG. F	Fast blanking signal; synchronized with video input signal. External RGB (OSD) signal; synchronized with video input signal and blanking signal.	

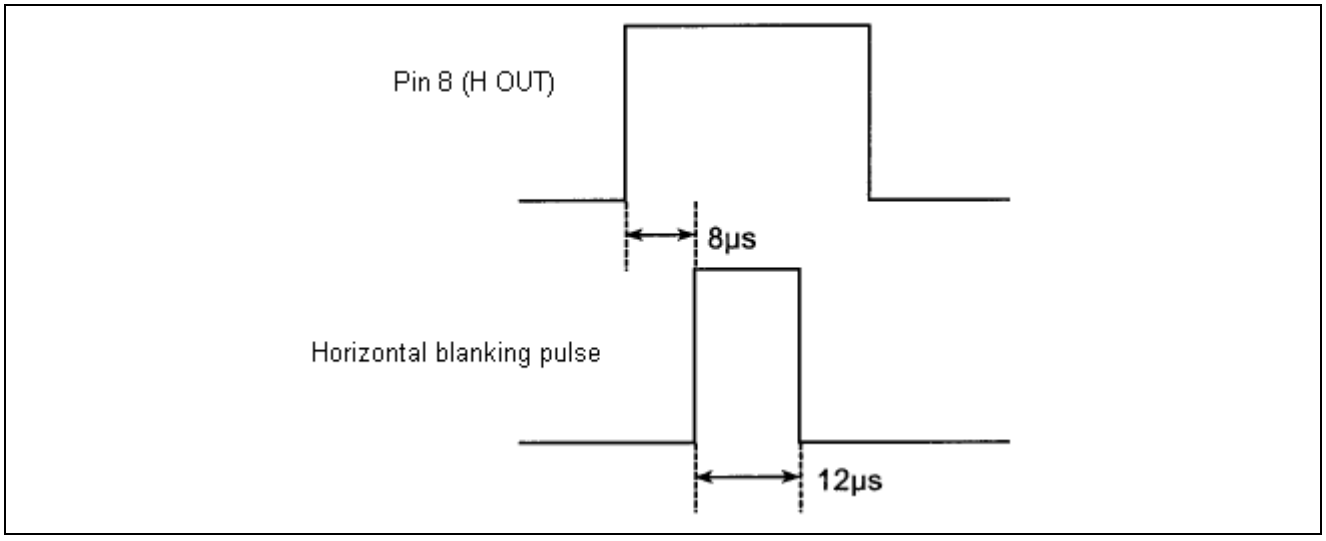
Video/Chroma/RGB/DEF Block (cont.)

SG No.	Signal Description (75 Ω termination)
SG.G	NTSC format rainbow color bar video signal. Vertical signal is interlaced at 60 Hz.
SG. H	Duty 90%, variable frequency, variable level. (Standard horizontal frequency = 15.734 kHz, vertical frequency = 60 Hz, 1 Vp-p) 
SG. I	Duty variable (standard 95%), frequency variable, level variable (Standard: horizontal frequency = 15.734 kHz, vertical frequency = 60 Hz, 1 Vp-p) 
SG. J	NTSC format standard color bar video signal; vertical signal is interlaced at 60 Hz. 
SG. K	NTSC format, standard 8-step wave signal; vertical signal is interlaced at 60 Hz.
SG. L	NTSC format red raster signal; vertical signal is interlaced at 60 Hz.
SG. M	NTSC format H SYNC. 
SG. N	

Setup Instructions for Evaluation PCB

1. Horizontal Blanking Pulse Adjustment

The horizontal blanking pulse timing and pulse width are adjusted using the variable resistances of a one-shot multivibrator, as shown below.



The timing is adjusted to 8 µs using the pin 15 variable resistance of the M74LS221P TTL IC. Also, the pulse width is adjusted to 12 µs using the VR1 variable resistance.

2. H VCO Adjustment

Prior to measurement of the M61283FP, the following method is used for H VCO adjustment.

1. The H VCO control I^2C bus data (1 CH D0-D2) is adjusted, and the pin 8 (H OUT) frequency is set to approx. 15.734 kHz.

Electrical Characteristics

(Ta = 25°C)

Symbol	Item	Input signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
ICC	Standard conditions								Pin 41 = 5 V, pins 3, 4, 5, 24, 33 = 0 V; pins 10, 13 = 8 V; pin 52 = 8.7 V
ICC5V	5 V circuit current (pin 41)	—	—	41	45	60	75	mA	VIDEO/Chroma Vcc
ICC8V	8 V circuit current	—	—	10,13	27	42	57	mA	Deflection/RGB Drive/East-West 8 V Vcc
ICC10	Pin 10 circuit current	—	—	10	—	23	—	mA	Reference data; Deflection/East-West Vcc
ICC13	Pin 13 circuit current	—	—	13	—	19	—	mA	Reference data; RGB Drive 8 V Vcc
ICC52	Pin 52 circuit current	—	—	52	3	6	9	mA	8.7 VREG Vcc
Power	Power supply circuit standard conditions								Pin 41 = 5 V, pins 3, 4, 5, 24, 33 = 0 V; pins 10, 13 = 8 V; pin 52 = 8.7 V
V61H	8.7 VREG output voltage 1	—	—	61	8.3	8.7	9.1	V	Pin 28 = 5 V
V61L	8.7 VREG output voltage 2	—	—	61	—	0	0.3	V	Pin 28 = 0 V
V54	5.7 VREG output voltage 1	—	—	54	5.55	5.8	6.05	V	Pin 28 = 5 V
V37H1	MCU 5.7 VREG output voltage 1	—	—	37	5.45	5.7	5.95	V	Pin 28 = 5 V
V37H2	MCU 5.7 VREG output voltage 2	—	—	37	5.45	5.7	5.95	V	Pin 28 = 0 V
Reset	Reset standard conditions								Pin 41 = 5 V, pins 3, 4, 5, 24, 33 = 0 V; pins 10, 13 = 8 V; pin 52 = 8.7 V
V30H	Maximum reset output voltage	—	—	30	4.5	5.0	5.5	V	
V30L	Minimum reset output voltage	—	—	30	—	0	0.5	V	
TH30	Reset threshold voltage	—	—	30	4.0	4.2	4.4	V	
I^2C	I^2C standard conditions	—	—	—	—	—	—	—	
IACK	ACK current	—	—		—	1	—	mA	Reference data
VIL	SCL/SDA VTH (L)	—	—	26,27	0.0	0.75	1.5	V	
VIH	SCL/SDA VTH (H)	—	—	26,27	3.5	4.25	5.0	V	
F_{SCL}	Clock frequency	—	—	27	—	—	100	kHz	

Symbol	Subaddress																													
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
ICC	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	40	08	08	20	60	20	20	20	20	14	00	00	00
ICC5V																																
ICC8V																																
ICC10																																
ICC13																																
ICC 52																																
Power	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	40	08	08	20	60	20	20	20	20	14	00	00	00
V61H																																
V61L																																
V54																																
V37H1																																
V37H2																																
Reset	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	40	08	08	20	60	20	20	20	20	14	00	00	00
V30H																																
V30L																																
TH30																																
I^2C	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	40	08	08	20	60	20	20	20	20	14	00	00	00
I_{ACK}																																
VIL																																
VIH																																
F_{SCL}																																

Symbol	Item	Input signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
VIDEO	Video standard conditions	—	—	—	—	—	—	—	Pin 41 = 5 V, pins 3, 4, 5, 24, 33 = 0 V; pins 10, 13 = 8 V; pin 52 = 8.7 V
2AGV1	Video SW1 output level (CVBS1 input)	46	SG.A	32	1.6	2.0	2.6	Vpp	
2AGV2	Video SW2 output level (CVBS2 input)	42	SG.A	32	1.6	2.0	2.6	Vpp	
2AGV3	Video SW3 output level (CVBS3 input)	38	SG.A	32	1.6	2.0	2.6	Vpp	
2AGV4	Video SW4 output level (CVBS4 input)	53	SG.A	32	1.6	2.0	2.6	Vpp	
2AGVY1	Video SWY output level 1 (Y:Y/C input)	51	SG.A	32	1.6	2.0	2.6	Vpp	
2AGVY2	Video SWY output level 2 (Y:YCbCr input)	48	SG.A	32	1.6	2.0	2.6	Vpp	
2AGV1L	Video line SW1 output level (CVBS1 input)	46	SG.A	60	0.6	1.0	1.4	Vpp	
2AGV2L	Video line SW2 output level (CVBS2 input)	42	SG.A	60	0.6	1.0	1.4	Vpp	
2AGV3L	Video line SW3 output level (CVBS3 input)	38	SG.A	60	0.6	1.0	1.4	Vpp	
2AGV4L	Video line SW4 output level (CVBS4 input)	53	SG.A	60	0.6	1.0	1.4	Vpp	
2AGVYL1	Video line SWY output level 1 (Y/C input)	51	SG.A	60	0.6	1.0	1.4	Vpp	
2AGVYL2	Video line SWY output level 2 (YcbCr input)	48	SG.A	60	0.6	1.0	1.4	Vpp	
Ymax	Maximum video output	46	SG.A	14,15,16	2.9	4.2	5.6	V	
GY	Video gain	46	SG.A	14,15,16	12	15	18	dB	
FBY	Video frequency characteristic	46	SG.B	14,15,16	–5	–2	—	dB	f = 800 k, 5 MHz, C-trap: OFF
CRF1	Chroma trap attenuation 1	46	SG.C	14,15,16	—	—	–18	dB	
CRF2	Chroma trap attenuation 2	46	SG.L	14,15,16	—	—	–6.5	dB	
YDL1	YDL time 1	46	SG.A	14,15,16	190	260	330	ns	
YDL2	YDL time 2	46	SG.A	14,15,16	100	150	250	ns	YDL2 = measured value – YDL1 measured value
YDL3	YDL time 3	46	SG.A	14,15,16	100	150	250	ns	YDL3 = measured value – YDL2 measured value
YDL4	YDL time 4	46	SG.A	14,15,16	100	150	250	ns	YDL4 = measured value – YDL3 measured value
DLYO1	DL YOUT DL time 1	46	SG.A	58	0	50	100	ns	
DLYO2	DL YOUT DL time 2	46	SG.A	58	100	150	250	ns	DLYO2 = measured value – DLYO1 measured value
DLYO3	DL YOUT DL time 3	46	SG.A	58	100	150	250	ns	DLYO3 = measured value – DLYO2 measured value
DLYO4	DL YOUT DL time 4	46	SG.A	58	100	150	250	ns	DLYO4 = measured value – DLYO3 measured value
Gtnor	Video tone control characteristic 1	46	SG.B	14,15,16	1.0	1.4	1.8	V	f = 2.5 MHz
GTmax	Video tone control characteristic 2	46	SG.B	14,15,16	7	10	14	dB	f = 2.5 MHz
GTmin	Video tone control characteristic 3	46	SG.B	14,15,16	–6	–2	2	dB	f = 2.5 MHz
GT2M	Video tone control characteristic 4	46	SG.B	14,15,16	–1	2	5	dB	f = 2 MHz
GT5M	Video tone control characteristic 5	46	SG.B	14,15,16	–9	–5	–1	dB	f = 5 MHz
BLS	Black stretch characteristic	46	SG.K	14,15,16	0.01	0.03	0.05	V	
VMF	Video mute function	46	SG.A	14,15,16	—	–45	–35	dB	

Symbol	Subaddress																														
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
VIDEO	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	40	08	08	20	60	20	20	20	20	14	00	00	00
2AGV1																																
2AGV2												81																				
2AGV3												82																				
2AGV4												83																				
2AGVY1																		01														
2AGVY2																		02														
2AGV1L																																
2AGV2L												81																				
2AGV3L												82																				
2AGV4L												83																				
2AGVYL1																		01														01
2AGVYL2																		02														02
Ymax	7F									00																						
GY	7F									00																						
FBY	7F							08		00																						
CRF1										00																				02		
CRF2	54				50	50	50			40																				02		
YDL1										00																						
YDL2										00			01																			
YDL3										00			02																			
YDL4										00			03																			
DLYO1										00														E0								
DLYO2										00													60	E0								
DLYO3										00													A0	E0								
DLYO4										00													E0	E0								
GTnor										00																						
GTmax										00	3F																					
GTmin										00	00																					
GT2M										00																						
GT5M										00																						
BLS	adj	adj								00		C0V 40																				
VMF	7F									00	80																					

Symbol	Item	Input signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
CHROMA	Chroma standard conditions	—	—	—	—	—	—	—	Pin 41 = 5 V, pins 3, 4, 5, 24, 33 = 0 V; pins 10, 13 = 8 V; pin 52 = 8.7 V
CnorR	Chroma standard output (R-Y)	46	SG.C	18	390	560	790	mVpp	
CnorB	Chroma standard output (B-Y)	46	SG.C	18	640	920	1290	mVpp	
CnorCr	Chroma standard output (Cr)	48,44, 40	SG.M, SG.N	18	390	560	790	mVpp	
CnorCb	Chroma standard output (Cb)	48,44, 40	SG.M, SG.N	18	500	720	940	mVpp	
ACC1	ACC characteristic 1	46	SG.E	18	–3	0	3	dB	Veb, Vec: standard input level +6 dB
ACC2	ACC characteristic 2	46	SG.E	18	–6.5	0	1.5	dB	Veb, Vec: standard input level –18 dB
OV	Chroma overload characteristic	46	SG.E	18	–3	2	5	dB	Vec = 800 mV
VikN	Killer operation input level	46	SG.E	18	—	–40	–35	dB	Veb, Vec: variable
KillP	Color remaining on colorkilling	46	SG.E	18	—	–45	–30	dB	Veb = 0 mV
APCU	APC pull-in range (upper)	46	SG.E	18	300	600	—	Hz	feb = fec: variable
APCL	APC pull-in range (lower)	46	SG.E	18	—	–600	–300	Hz	feb = fec: variable
R/BN	Demodulation ratio	46	SG.E	18	0.40	0.57	0.80	—	fec = feb + 50 kHz
R-YN1	Demodulation angle 1	46	SG.E	18	86	103	120	deg	fec = feb + 50 kHz
R-YN2	Demodulation angle 2	46	SG.E	18	78	95	112	deg	fec = feb + 50 kHz
TC1	TINT control characteristic 1	46	SG.E	18	30	45	60	deg	fec = feb + 50 kHz
TC2	TINT control characteristic 2	46	SG.E	18	30	45	60	deg	fec = feb + 50 kHz
BTC1	Base band TINT characteristic 1	48,44, 40	SG.M, SG.N	18	30	45	—	deg	
BTC2	Base band TINT characteristic 2	48,44, 40	SG.M, SG.N	18	30	45	—	deg	
CbDL1	CbDL time 1	48,44, 40	SG.M, SG.N	18	200	350	500	ns	
CbDL2	CbDL time 2	48,44, 40	SG.M, SG.N	18	20	50	80	ns	CbDL2 = measured value – CbDL1 measured value
CbDL3	CbDL time 3	48,44, 40	SG.M, SG.N	18	20	50	80	ns	CbDL3 = measured value – CbDL2 measured value
CbDL4	CbDL time 4	48,44, 40	SG.M, SG.N	18	20	50	80	ns	CbDL4 = measured value – CbDL3 measured value
CrDL1	CrDL time 1	48,44, 40	SG.M, SG.N	18	200	350	500	ns	
CrDL2	CrDL time 2	48,44, 40	SG.M, SG.N	18	20	50	80	ns	CrDL2 = measured value – CrDL1 measured value
CrDL3	CrDL time 3	48,44, 40	SG.M, SG.N	18	20	50	80	ns	CrDL3 = measured value – CrDL2 measured value
CrDL4	CrDL time 4	48,44, 40	SG.M, SG.N	18	20	50	80	ns	CrDL4 = measured value – CrDL3 measured value
Ffsc1	fsc output frequency 1	46	SG.C	55	3.5793	3.5796	3.5799	MHz	
Vfsc1	fsc output amplitude 1	46	SG.C	55	250	500	800	mVpp	
Ffscfree1	fsc output frequency 1 in fsc free mode	46	SG.C	55	3.5790	3.5795	3.5810	MHz	
Vfscfree1	fsc output amplitude 1 in fsc free mode	46	SG.C	55	250	500	800	mVpp	
Ffsc2	fsc output frequency 2	46	SG.C	29	3.5793	3.5796	3.5799	MHz	
Vfsc2	fsc output amplitude 2	46	SG.C	29	1400	2000	2600	mVpp	
Ffscfree2	fsc output frequency 2 in fsc free mode	46	SG.C	29	3.5790	3.5795	3.5810	MHz	
Vfscfree2	fsc output amplitude 2 in fsc free mode	46	SG.C	29	1400	2000	2600	mVpp	

Symbol	Subaddress																														
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
CHROMA	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	40	08	08	20	60	20	20	20	20	14	00	00	00
CnorR																		10														
CnorB																		20														
CnorCr																		12														
CnorCb																		22														
ACC1																		20														
ACC2																		20														
OV																		20														
VikN																		20														
KillP																		20														
APCU																		20														
APCL																		20														
R/BN																		10/20														
R-YN1																		10/20														
R-YN2													10					10/20														
TC1									7F									20														
TC2									00									20														
BTC1																		12/22		00												
BTC2																		12/22		7F												
CbDL1																		22														
CbDL2																		22			18											
CbDL3																		22			28											
CbDL4																		22			38											
CrDL1																		12														
CrDL2																		12				18										
CrDL3																		12				28										
CrDL4																		12				38										
Ffsc1																																
Vfsc1																																
Ffscfree1								40																								
Vfscfree1								40																								
Ffsc2																																
Vfsc2																																
Ffscfree2								40																								
Vfscfree2								40																								

Symbol	Item	Input signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
RGB	RGB standard conditions	—	—	—	—	—	—	—	Pin 41 = 5 V, pins 3, 4, 5, 24, 33 = 0 V; pins 10, 13 = 8 V; pin 52 = 8.7 V
VBLK	Output blanking voltage	46	SG.A	14,15, 16	0	0.1	0.3	V	
Gytyp	Contrast control characteristic 1	46	SG.B	14,15, 16	1.8	2.4	2.9	Vpp	f = 100 kHz
GYmin	Contrast control characteristic 2	46	SG.B	14,15, 16	—	200	300	mVpp	f = 100 kHz
GYEnor	Contrast control characteristic 3	46	SG.A	14,15, 16	1.8	2.4	2.9	Vpp	Pin 17 = 2.9 V
GYEmin	Contrast control characteristic 4	46	SG.A	14,15, 16	—	100	200	mVpp	Pin 17 = 0.0 V
GYEclip	Contrast control characteristic 5	21,22, 23	SG.F	14,15, 16	0.50	0.65	0.80	Vpp	Pin 24 = 2.0 V
Lum nor	Brightness control characteristic 1	46	SG.D	14,15, 16	2.0	2.4	2.8	V	Vy = 0.0 V
Lum max	Brightness control characteristic 2	46	SG.D	14,15, 16	2.6	3.3	—	V	Vy = 0.0 V
Lum min	Brightness control characteristic 3	46	SG.D	14,15, 16	—	1.6	2.3	V	Vy = 0.0 V
D(R)1	R driving control characteristic 1	46	SG.A	14	2.0	4.0	6.0	dB	
D(B)1	B driving control characteristic 1	46	SG.A	16	2.0	4.0	6.0	dB	
D(R)2	R driving control characteristic 2	46	SG.A	14	–5.0	–3.0	–1.0	dB	
D(B)2	B driving control characteristic 2	46	SG.A	16	–5.0	–3.0	–1.0	dB	
EXD1(R)	Digital OSD (R) I/O characteristic 1	23,24, 46	SG.F, SG.A	14	1.0	1.5	2.0	Vpp	Vosd = 1.0 V, SW23 = ON
EXD1(G)	Digital OSD (G) I/O characteristic 1	22,24, 46	SG.F, SG.A	15	1.0	1.5	2.0	Vpp	Vosd = 1.0 V, SW22 = ON
EXD1(B)	Digital OSD (B) I/O characteristic 1	21,24, 46	SG.F, SG.A	16	1.0	1.5	2.0	Vpp	Vosd = 1.0 V, SW21 = ON
EXD2(R)	Digital OSD (R) I/O characteristic 2	23,24, 46	SG.F, SG.A	14	200	300	400	V	Vosd = 1.0 V, EXD2(R) = measured value – EXD1(R)
EXD2(G)	Digital OSD (G) I/O characteristic 2	22,24, 46	SG.F, SG.A	15	200	300	400	V	Vosd = 1.0 V, EXD2(G) = measured value – EXD1(G)
EXD2(B)	Digital OSD (B) I/O characteristic 2	21,24, 46	SG.F, SG.A	16	200	300	400	V	Vosd = 1.0 V, EXD2(B) = measured value – EXD1(B)
EXD1(R-G)	Digital OSD (R-G) amplitude difference	—	—	—	–350	0	350	mV	
EXD1(G-B)	Digital OSD (G-B) amplitude difference	—	—	—	–350	0	350	mV	
EXD1(B-R)	Digital OSD (B-R) amplitude difference	—	—	—	–350	0	350	mV	
EXD2(R-G)	Digital OSD black level DC voltage difference (R-G)	—	—	—	–350	0	350	mV	
EXD2(B-G)	Digital OSD black level DC voltage difference (B-G)	—	—	—	–350	0	350	mV	
EXA(R)	Analog OSD (R) I/O characteristic	23,24, 46	SG.F, SG.A	14	1.2	2	3	Vpp	Vosd = 0.7 V
EXA(G)	Analog OSD (G) I/O characteristic	22,24, 46	SG.F, SG.A	15	1.2	2	3	Vpp	Vosd = 0.7 V
EXA(B)	Analog OSD (B) I/O characteristic	21,24, 46	SG.F, SG.A	16	1.2	2	3	Vpp	Vosd = 0.7 V
EXA1(R-G)	Analog OSD (R-G) amplitude difference	—	—	—	–350	0	350	mV	
EXA1(G-B)	Analog OSD (G-B) amplitude difference	—	—	—	–350	0	350	mV	
EXA1(B-R)	Analog OSD (B-R) amplitude difference	—	—	—	–350	0	350	mV	
EXA2(R-G)	Analog OSD black level DC voltage difference (R-G)	—	—	—	–250	0	250	mV	
EXA2(B-G)	Analog OSD black level DC voltage difference (B-G)	—	—	—	–250	0	250	mV	

Symbol	Subaddress																														
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
RGB	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	40	08	08	20	60	20	20	20	20	14	00	00	00
VBLK										00																						
GYtyp										00																						
GYmin	00									00																						
GYEnor										00																						
GYEmin										00																						
GYEclip	00									00																						
Lum nor										00																						
Lum max		FF								00																						
Lum min		00								00																						
D(R)1		00	7F							00																						
D(B)1		00		7F						00																						
D(R)2		00	00							00																						
D(B)2		00		00						00																						
EXD1(R)										00																						08
EXD1(G)										00																						08
EXD1(B)										00																						08
EXD2(R)										00																						
EXD2(G)										00																						
EXD2(B)										00																						
EXD1 (R-G)																																
EXD1 (G-B)																																
EXD1 (B-R)																																
EXD2 (R-G)																																
EXD2 (B-G)																																
EXA(R)																													34			
EXA(G)																													34			
EXA(B)																													34			
EXA1 (R-G)																																
EXA1 (G-B)																																
EXA1 (B-R)																																
EXA2 (R-G)																																
EXD2 (B-G)																																

Symbol	Item	Input signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
OFRG	Offset voltage (R-G)	46	SG.D	14,15	–100	0	100	mV	Vy = 0.0 V
OFBG	Offset voltage (B-G)	46	SG.D	15,16	–100	0	100	mV	Vy = 0.0 V
C(R)1	R cutoff control characteristic 1	46	SG.D	14	2.8	3.1	3.4	V	Vy = 0.0 V
C(G)1	G cutoff control characteristic 1	46	SG.D	15	2.8	3.1	3.4	V	Vy = 0.0 V
C(B)1	B cutoff control characteristic 1	46	SG.D	16	2.8	3.1	3.4	V	Vy = 0.0 V
C(R)2	R cutoff control characteristic 2	46	SG.D	14	1.3	1.6	1.9	V	Vy = 0.0 V
C(G)2	G cutoff control characteristic 2	46	SG.D	15	1.3	1.6	1.9	V	Vy = 0.0 V
C(B)2	B cutoff control characteristic 2	46	SG.D	16	1.3	1.6	1.9	V	Vy = 0.0 V
Ccon1	Color control characteristic 1	46	SG.C	15	3	6	9	dB	
Ccon2	Color control characteristic 2	46	SG.C	15	—	–17	–12	dB	
Ccon3	Color control characteristic 3	46	SG.C	15	—	–40	–35	dB	
MTXRB	Matrix ratio R/B	46	SG.G	14,16	0.9	1.10	1.2	—	
MTXGB	Matrix ratio G/B	46	SG.G	15,16	0.29	0.37	0.45	—	
DOSD1	Digital OSD switching characteristic 1	23,24, 46	SG.F, SG.A	14	—	0.05	0.13	μs	Vosd = 1.0 V, SW23 = ON
DOSD2	Digital OSD switching characteristic 2	23,24, 46	SG.F, SG.A	14	—	0.05	0.13	μs	Vosd = 1.0 V, SW23 = ON
AOSD1	Analog OSD switching characteristic 1	23,24, 46	SG.F, SG.A	14	—	0.05	0.13	μs	Vosd = 1.0 V
AOSD2	Analog OSD switching characteristic 2	23,24, 46	SG.F, SG.A	14	—	0.05	0.13	μs	Vosd = 1.0 V
BB(R)	Blue background function (R)	46	SG.A	14	1.7	2.1	2.5	V	
BB(G)	Blue background function (G)	46	SG.A	15	1.7	2.1	2.5	V	
BB(B)	Blue background function (B)	46	SG.A	16	2.7	3.7	4.7	V	
WB	White raster function	46	SG.A	14,15, 16	2.7	3.7	4.7	V	
WBL-RB	White balance difference--RB	46	SG.A Y=30%	14,16	–80.0	–20.0	10.0	mV	White level difference with, without burst, with reference to pin 16 (Bout)
WBL-GB	White balance difference--GB	46	SG.A Y=30%	14,16	–10.0	10.0	80.0	mV	White level difference with, without burst, with reference to pin 16 (Bout)

Symbol	Subaddress																														
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
OFRG										00																					
OFBG										00																					
C(R)1					FF					00																					
C(G)1						FF				00																					
C(B)1							FF			00																					
C(R)2					00					00																					
C(G)2						00				00																					
C(B)2							00			00																					
Ccon 1										7F	80																				
Ccon 2										01	80																				
Ccon 3										00	80																				
MTXRB																															
MTXGB																															
DOSD1	7F																														
DOSD2	7F																														
AOSD1	7F																												34		
AOSD2	7F																												34		
BB(R)										80																					
BB(G)										80																					
BB(B)										80																					
WB				C0																											
WBL-RB		40																													
WBL-GB		40																													

Symbol	Item	Input signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
DEF	Deflection system standard conditions	—	—	—	—	—	—	—	Pin 41 = 5 V, pins 3, 4, 5, 24, 33 = 0 V; pins 10, 13 = 8 V; pin 52 = 8.7 V
fH1	Horizontal free-running frequency 1	—	—	8	15.3	15.7	16.1	kHz	
fH2	Horizontal free-running frequency 2	—	—	8	14.7	15.1	15.5	kHz	
fH3	Horizontal free-running frequency 3	—	—	8	15.8	16.2	16.6	kHz	
Hfree	Forced horizontal free-running operation	46	SG.A	8	15.3	15.7	16.1	kHz	In Hfree operation (0FH: D6 = 1)
FPHU	Horizontal pull-in range (upper)	46	SG.H	8	250	500	—	Hz	Variable input frequency
FPHL	Horizontal pull-in range (lower)	46	SG.H	8	—	–500	–250	Hz	Variable input frequency
HPT1	Horizontal pulse timing 1	46	SG.A	8	4.5	6.0	7.5	μs	
HPT2	Horizontal pulse timing 2	46	SG.A	8	3.5	5.0	6.5	μs	
HPTW	Horizontal pulse width	—	—	8	21	25	29	μs	
AFCG	AFC gain operation	46	SG.A	2	2.0	3.0	10.0	dB	When 12H is 03, 07, measure and compute amplitude
FV	Vertical free-running frequency	—	—	20	55	60	65	Hz	
Vfree	Forced vertical free-running operation	46	SG.A	20	55	60	65	Hz	In Vfree operation (0EH: D6 = 1)
SVC	Service mode operation	—	—	63	3.5	4	4.5	V	
FPVU	Vertical pull-in frequency (upper)	46	SG.H	20	63	67	—	Hz	Variable input frequency
FPVL	Vertical pull-in frequency (lower)	46	SG.H	20	—	55	57	Hz	Variable input frequency
VRsi1	Vertical ramp size	46	SG.A	63	1.7	2.1	2.5	Vpp	
VRsc1	Vertical ramp size control range 1	46	SG.A	63	2.5	2.9	3.3	Vpp	
VRsc2	Vertical ramp size control range 2	46	SG.A	63	0.8	1.2	1.6	Vpp	
VRpo1	Vertical ramp position control range 1	46	SG.A	63	18	38	58	μs	
VRpo2	Vertical ramp position control range 2	46	SG.A	63	820	870	920	μs	Measured value – VRpo 1
VW	Vertical pulse width	46	SG.A	20	0.35	0.53	0.65	ms	
VBLKW	Vertical blanking width	46	SG.A	14,15, 16	1.42	1.57	1.72	ms	
VBLKW1	Vertical blanking width 1	46	SG.A	14,15, 16	1.41	1.52	1.63	ms	
VBLKW2	Vertical blanking width 2	46	SG.A	14,15, 16	2.33	2.43	2.55	ms	
VBLKW3	Vertical blanking width 3	46	SG.A	14,15, 16	2.84	2.95	3.06	ms	
VBLKW4	Vertical blanking width 4	46	SG.A	14,15, 16	3.34	3.45	3.56	ms	
WVSS	Minimum width in minimum sync operation	46	SG.I	63	14	—	—	μs	Variable input signal duty

Symbol	Subaddress																														
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
DEF	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	40	08	08	20	60	20	20	20	20	14	00	00	00
fH1																																
fH2																													00			
fH3																													06			
Hfree																C8																
FPHU																																
FPHL																																
HPT1																80			0F													
HPT2																8F			0F													
HPTW																																
AFCG																			Adj													
fV																																
Vfree															60																	
SVC														C0																		
FPVU																																
FPVL																																
VRsi 1																																
VRsc 1															3F																	
VRsc 2															00																	
VRpo 1																																
VRpo 2														47																		
VW																																
VBLKW										00																						
VBLKW1										00							10															
VBLKW2										00							15															
VBLKW3										00							1A															
VBLKW4										00							1F															
WVSS																																

Symbol	Item	Input signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
VSco1	Vertical S-correction control range 1	46	SG.A	63	0.1	0.5	0.9	Vpp	(measured value) – (VRSi 1)
VSco2	Vertical S-correction control range 2	46	SG.A	63	–0.9	–0.5	–0.1	Vpp	(measured value) – (VRSi 1)
VL T	Vertical linearity top voltage	46	SG.A	63	3.6	4.0	4.4	V	
VL B	Vertical linearity bottom voltage	46	SG.A	63	1.5	1.9	2.3	V	
VLTco1	Vertical linearity top voltage control range 1	46	SG.A	63	0.05	0.25	0.45	V	(measured value) – (VLT)
VLTco2	Vertical linearity top voltage control range 2	46	SG.A	63	–0.45	–0.25	0.05	V	(measured value) – (VLT)
VLBco1	Vertical linearity bottom voltage control range 1	46	SG.A	63	–0.45	–0.25	0.05	V	(measured value) – (VLB)
VLBco2	Vertical linearity bottom voltage control range 2	46	SG.A	63	0.05	0.25	0.45	V	(measured value) – (VLB)
EWP	Parabola size	46	SG.A	59	1.0	1.4	1.8	Vpp	
EWPco1	Parabola control range 1	46	SG.A	59	1.6	2.0	2.4	Vpp	
EWPco2	Parabola control range 2	46	SG.A	59	—	0.1	0.5	Vpp	
EWCco1	Corner control range 1	46	SG.A	59	–1.0	–0.4	0.1	Vpp	
EWCco2	Corner control range 2	46	SG.A	59	2.1	2.5	2.9	Vpp	
EWTa	Trapezoid bottom voltage a	46	SG.A	59	2.3	2.7	3.1	V	
EWTb	Trapezoid bottom voltage b	46	SG.A	59	2.3	2.7	3.1	V	
EWTcoa1	Trapezoid control voltage a1	46	SG.A	59	–0.7	–0.3	–0.05	V	(measured value) – (EWTa)
EWTcoa2	Trapezoid control voltage a2	46	SG.A	59	0.05	0.3	0.7	V	(measured value) – (EWTa)
EWTcob1	Trapezoid control voltage b1	46	SG.A	59	0.05	0.3	0.7	V	(measured value) – (EWTb)
EWTcob2	Trapezoid control voltage b2	46	SG.A	59	–0.7	–0.3	–0.05	V	(measured value) – (EWTb)
EWSi	Parabola top voltage	46	SG.A	59	3.8	4.2	4.6	V	
EWSico1	Horizontal size control range 1	46	SG.A	59	0.5	0.9	1.3	V	(measured value) – (EWSi)
EWSico2	Horizontal size control range 2	46	SG.A	59	–1.5	–1.1	–0.7	V	(measured value) – (EWSi)

Symbol	Subaddress																														
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
VSco1																							3F								
VSco2																							00								
VL T																															
VL B																															
VLTco1																								7F							
VLTco2																								40							
VLBco1																								7F							
VLBco2																								40							
EWP																															
EWPco1																									3F						
EWPco2																									00						
EWCco1																										3F					
EWCco2																										00					
EWTa																															
EWTb																															
EWTcoa1																											3F				
EWTcoa2																											00				
EWTcob1																											3F				
EWTcob2																											00				
EWSi																															
EWSico1																												3F			
EWSico2																												00			

Symbol	Item	Input signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
Monitoring	Intelligent monitor system standard conditions	—	—	—	—	—	—	—	Pin 41 = 5 V, pins 3, 4, 5, 24, 33 = 0 V; pins 10, 13 = 8 V; pin 52 = 8.7 V
MONI1	Intelligent monitor 1 (composite sync)	46	SG.A	18	—	4.9	—	V	Reference data
MONI2	Intelligent monitor 2 (R-Y OUT)	46	SG.J	18	—	1090	—	mVpp	Reference data
MONI3	Intelligent monitor 3 (B-Y OUT)	46	SG.J	18	—	1350	—	mVpp	Reference data
MONI4	Intelligent monitor 4 (R-Y REF OUT)	46	—	18	—	3.0	—	V	Reference data
MONI5	Intelligent monitor 5 (B-Y REF OUT)	46	—	18	—	3.0	—	V	Reference data
MONI6	Intelligent monitor 6 (video SW output)	46	SG.A	18	—	0.90	—	Vpp	Reference data
MONI7	Intelligent monitor 7 (G out)	46	SG.A	18	—	1.5	—	Vpp	Reference data. Amplitude measured from blanking level
MONI8	Intelligent monitor 8 (R out)	46	SG.A	18	—	1.5	—	Vpp	Reference data. Amplitude measured from blanking level
MONI9	Intelligent monitor 9 (B out)	46	SG.A	18	—	1.5	—	Vpp	Reference data. Amplitude measured from blanking level
MONI10	Intelligent monitor 10 (ACL)	—	—	18	—	4.5	—	V	Reference data
MONI11	Intelligent monitor 11 (V sync)	46	SG.A	18	—	3.5	—	Vpp	Reference data
MONI12	Intelligent monitor 12 (H out)	46	SG.A	18	—	3.5	—	Vpp	Reference data
MONI14	Intelligent monitor 14 (DEF Vcc)	—	—	18	—	4.00	—	V	Reference data
MONI15	Intelligent monitor 15 (video/chroma Vcc)	—	—	18	—	3.00	—	V	Reference data
MONI16	Intelligent monitor 16 (Hi Vcc)	—	—	18	—	2.70	—	V	Reference data

- Intelligent Monitor Map
  1. Sub Address: 11HD4 – D7
  2. Output Pin: Pin18
  3. Specification

No.	11H	11H				Output
	HEX	D7	D6	D5	D4	Signal
0	0	0	0	0	0	Composite Sync
1	1	0	0	0	1	R-Y OUT
2	2	0	0	1	0	B-Y OUT
3	3	0	0	1	1	R-Y REF OUT
4	4	0	1	0	0	B-Y REF OUT
5	5	0	1	0	1	Y SW OUT
6	6	0	1	1	0	G OUT
7	7	0	1	1	1	R OUT
8	8	1	0	0	0	B OUT
9	9	1	0	0	1	ACL/ABCL
10	A	1	0	1	0	V SYNC
11	B	1	0	1	1	H OUT
12	C	1	1	0	0	DEF VCC
13	D	1	1	0	1	DEF VCC
14	E	1	1	1	0	V/C VCC
15	F	1	1	1	1	HI VCC

Symbol	Subaddress																													
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	16H	17H	18H	19H	1AH	1BH	1CH	1DH	1EH	1FH
MONITORING	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	40	08	08	20	60	20	20	20	20	14	00	00	00
MONI1																		00														
MONI2																		10														
MONI3																		20														
MONI4																		30														
MONI5																		40														
MONI6																		50														
MONI7										00								60														
MONI8										00								70														
MONI9										00								80														
MONI10																		90														
MONI11																		A0														
MONI12																		B0														
MONI14																		D0														
MONI15																		E0														
MONI16																		F0														

Method of Measurement of Electrical Characteristics

Video Block

2AGV1-4 video SW output level 1-4(CVBS1-4 input)
2AGVY1 video SW output level 1(Y input: Y/C)
2AGVY2 video SW output level 2(Y input: YCbCr)

1. Input SG.A to pin 46 (CVBS1), or pin 42 (CVBS2), or pin 38 (CVBS3), or pin 53 (CVBS4), or pin 51 (Y(Y/C)), or pin 48 (Y(YCbCr)).
2. The amplitude (p-p) at pin 32 is measured.

* In order to select TV or external input, use the sub-addresses 0BH and 11H.

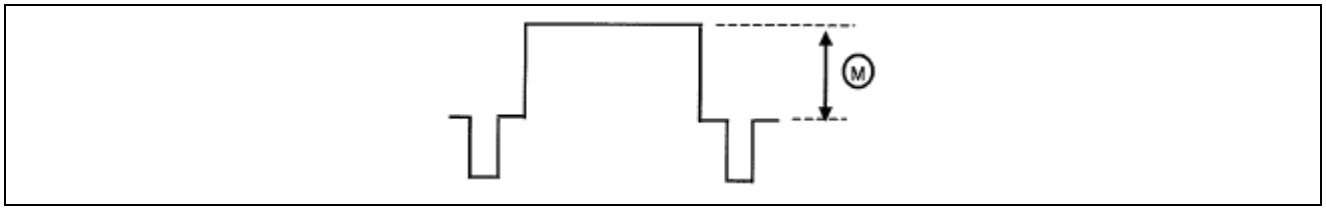
2AGVL1-4 video line SW output level 1-4(CVBS1-4 input)
2AGVYL1 video line SW output level 1(Y input: Y/C)
2AGVYL2 video line SW output level 2(Y input: YCbCr)

1. Input SG.A to pin 46 (CVBS1), or pin 42 (CVBS2), or pin 38 (CVBS3), or pin 53 (CVBS4), or pin 51 (Y(Y/C)), or pin 48 (Y(YCbCr)).
2. The amplitude (p-p) at pin 60 is measured.

* In order to select TV or external input, use the sub-addresses 0BH, 11H, and 1F.

Y max maximum video output

1. Input SG.A to pin 46.
2. Measure the amplitude (p-p) other than the blanking part of the output of pins 14, 15, 16.



FBY video frequency characteristic

1. Input SG.B (800kHz, 5 MHz) to pin 46.
2. Measure the amplitude (p-p) other than the blanking part of the output of pins 14, 15, 16, take the results at 800 kHz and 5 MHz as Vr1 and Vr2 respectively.
3. FBY is defined as follows.

$$FBY = 20 \log \frac{Vr2\ (Vp\text{-}p)}{Vr1\ (Vp\text{-}p)} (dB)$$

CRF1 chroma trap attenuation 1 (normal R/G/B output)
TRF maximum chroma trap attenuation

1. Input SG.C to pin 46, measure the 3.58 MHz frequency level with TRAP ON/OFF (07H D3) DATA 1, take the results to be N_0.
2. Also measure the level with TRAP ON/OFF (07H D3) DATA 0.
3. CRF1 is defined as follows.

$$CRF1 = 20 \log \frac{\text{measured value}\ (mVp\text{-}p)}{N_0\ (mVp\text{-}p)} (dB)$$

4. Take the minimum value of CRF1 when the I^2C BUS data of the TRAP fine ADJ (1DH D0/D1) is adjusted to be TRF.

CRF2 chroma trap attenuation 2 (normal R/G/B output)

1. Input SG.L to pin 46. The input 3.58 MHz frequency level is N_1.
2. Measure the 3.58 MHz frequency level when TRAP ON/OFF (07H D3) DATA 0.
3. CRF2 is defined as follows.

$$CRF2 = 20 \log \frac{\text{measured value (mVp-p)}}{N_1 \text{ (mVp-p)}} \text{ (dB)}$$

YDL1: YDL time 1

1. Input SG.A to pin 46.
2. Measure the delay time relative to the input signal of pins 14, 15, 16.

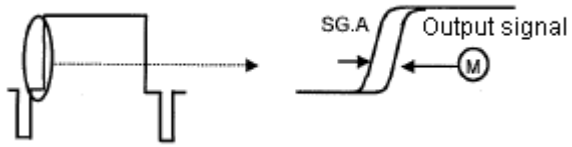
The delay time at 50% rise level is measured.

YDL2, 3, 4: YDL time 2, 3, 4

1. Input SG.A to pin 46.
2. Measure the delay time of the input signal and the pin 14, 15, 16 output signals.
3. YDL2, YDL3, YDL4 are defined as follows.
   YDL2 = measured value (ns) – YDL1 (measured value)
   YDL3 = measured value (ns) – YDL2 (measured value)
   YDL4 = measured value (ns) – YDL3 (measured value)

DLYO1: DELAYED YOUT time 1

1. Input SG.A to pin 46.
2. Measure the delay time relative to the input signal of pin 58.



The delay time at 50% rise level is measured.

DLYO2,3,4: DELAYED YOUT time 2, 3, 4

1. Input SG.A to pin 46.
2. Measure the delay time of the input signal and the pin 58 output signal.
3. DLYO2, DLYO3, DLYO4 are defined as follows.
   DLYO2 = measured value (ns) - DLYO1 (measured value)
   DLYO3 = measured value (ns) - DLYO2 (measured value)
   DLYO4 = measured value (ns) - DLYO3 (measured value)

GTmax video tone control characteristic 2

1. Input SG.B (f = 2.5 MHz) to pin 46.
2. The output amplitude of pins 14, 15, 16 when the video tone data is at the center (20 H) is taken to be GTnor.
3. The output amplitude of pins 14, 15, 16 when the video tone data is maximum is measured.
4. GTmax is defined as follows.

$$GTmax = 20 \log \frac{\text{measured value (Vp-p)}}{GTnor(Vp\text{-}p)} (dB)$$

GTmin video tone control characteristic 3

1. Input SG.B (f = 2.5 MHz) to pin 46.
2. The output amplitude of pins 14, 15, 16 when the video tone data is at the center (20 H) is taken to be GTnor.
3. The output amplitude of pins 14, 15, 16 when the video tone data is minimum is measured.
4. GTmin is defined as follows.

$$GTmin = 20 \log \frac{\text{measured value (Vp-p)}}{GTnor(Vp\text{-}p)} (dB)$$

GT2M video tone control characteristic 4

1. Take pin 14, 15, 16 output amplitude when input signal frequency is 2.5 MHz to be GTnor.
2. Input SG.B (f = 2 MHz) to pin 46.
3. Measure pin 14, 15, 16 output amplitude.
4. GT2M is defined as follows

$$GT2M = 20 \log \frac{\text{measured value (Vp-p)}}{GTnor(Vp\text{-}p)} (dB)$$

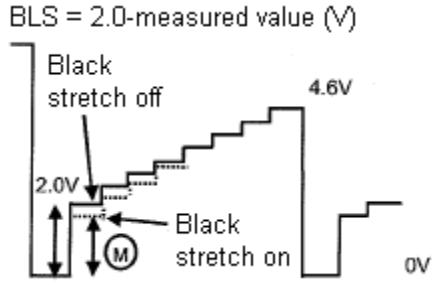
GT5M video tone control characteristic 5

1. Take pin 14, 15, 16 output amplitude when input signal frequency is 2.5 MHz to be GTnor.
2. Input SG.B (f = 5 MHz) to pin 46.
3. Measure pin 14, 15, 16 output amplitude.
4. GT5M is defined as follows.

$$GT5M = 20 \log \frac{\text{measured value (Vp-p)}}{GTnor(Vp\text{-}p)} (dB)$$

BLS black stretch characteristic

1. Input SG.K to pin 25.
2. With black stretch off (0BH D7 = 1), adjust the contrast (00H) and brightness (01H), and set the first stage (lowest stage) output level of pin 14, 15, 16 to 2.0 V, and the eighth stage (highest stage) output level to 4.6 V.
3. Change black stretch to on (0BH D7=0), and measure the pin 14, 15, 16 first stage output level.
4. BLS is defined as follows.



VMF video mute function

1. Input SG.A to pin 46.
2. With the mute switch (0AH D7) on "VMFon", off "VMFoff", measure the output amplitude.
3. VMF is defined as follows.

$$VMF = 20 \log \frac{VMFon(Vp\text{-}p)}{VMFoff(Vp\text{-}p)} (dB)$$

Chroma Block

CnorR chroma standard output (R-Y)
CnorB Chroma standard output (B-Y)

1. Input SG.C to pin 46.
2. When I^2C data is 11H D4 = 1 and 11H D5 = 1, take the pin 18 output amplitude as the chroma standard output (R-Y) and chroma standard output (B-Y), respectively.

CnorCr chroma standard output (Cr)
CnorCb chroma standard output (Cb)

1. Input SG.M and SG.N to pin 48 and pins 40 & 44, respectively.
2. In YCbCr mode (11H data O2H), take the pin 18 output amplitude as the chroma standard output (Cr) and chroma standard output (Cb), respectively.

ACC1 ACC characteristic 1

1. Input SG.E (eb = 570 mV: level + 6 dB) to pin 46.
2. Measure the pin 18 output amplitude.
3. ACC1 is defined as follows.

$$ACC1 = 20 \log \frac{\text{measured value (mVp-p)}}{\text{chroma standard output 1 (mVp-p)}} (dB)$$

ACC2 ACC characteristic 2

1. Input SG.E (input level: -18 dB) to pin 46.
2. Measure the pin 18 output amplitude.
3. ACC2 is defined as follows.

$$ACC2 = 20 \log \frac{\text{measured value (mVp-p)}}{\text{chroma standard output 1 (mVp-p)}} \text{(dB)}$$

OV chroma overload characteristic

1. Input SG.E (eb = 800 mVp-p: chroma + 3 dB) to pin 46.
2. Measure the pin 18 output amplitude.
3. OV is defined as follows.

$$OV = 20 \log \frac{\text{measured value (mVp-p)}}{\text{chroma standard output 1 (mVp-p)}} \text{(dB)}$$

VikN killer operation input level

1. Input SG.E (variable level) at input level 0 dB to pin 46.
2. While monitoring the pin 18 output amplitude, lower the input level, and measure the input level when the output amplitude vanishes.

KillP hue remaining with killer

1. Input SG.E (level: –40 dB) to pin 46.
2. Measure the pin 18 output amplitude.

APCU APC pull-in range (upper)
APCL APC pull-in range (lower)

1. Input SG.E (feb = fec = 3.579545 MHz) to pin 46.
2. After raising the frequency until the output from pin 18 vanishes, lower the frequency, and take the point at which an output appears to be fu.
3. After lowering the frequency until the output from pin 18 vanishes, raise the frequency, and take the point at which an output appears to be fl.
4. APCU and APCL are defined as follows.

   APCU = fu – 3579545 Hz
   APCL = fl – 3579545 Hz

R/BN demodulation ratio R-Y/B-Y

1. Input SG.E (eb = single chroma = ec + 50 kHz) to pin 46.
2. Take the pin 18 output amplitude when I^2C data is 11H D4 = 1 to be VRY.
3. Take the pin 18 output amplitude when I^2C data is 11H D5=1 to be VBY.
4. R/BN is defined as follows.

$$R/BN = \frac{VRY\ (mVp\text{-}p)}{VBY\ (mVp\text{-}p)}$$

R-YN demodulation angle

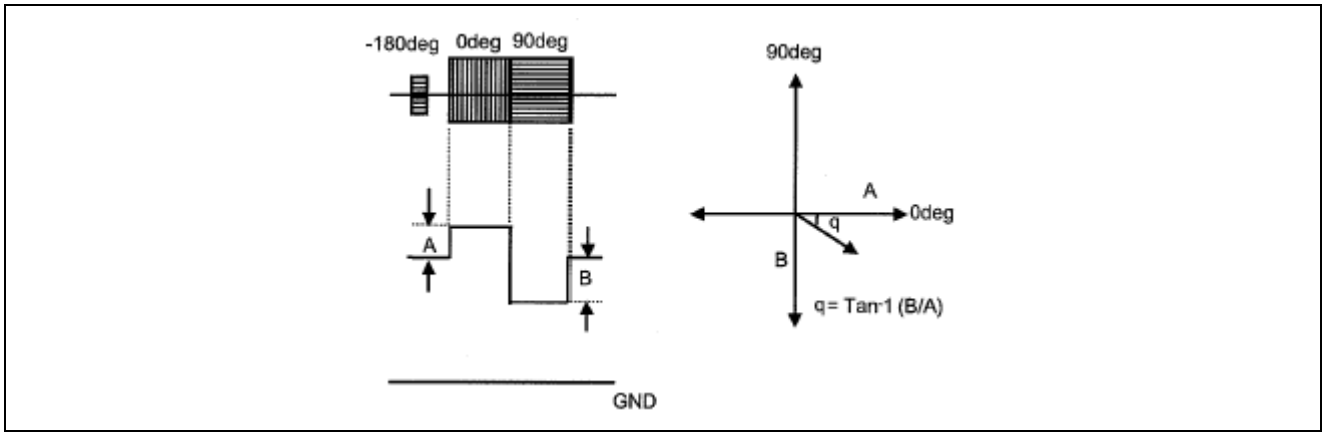
1. Input SG.E (eb = single chroma = ec + 5 kHz) to pin 46.
2. Take the pin 18 output amplitude when I^2C data is 11H D4=1 to be VRY.
3. Take the pin 18 output amplitude when I^2C data is 11H D5=1 to be VBY.
4. R-YN is defined as follows.

$$\text{R-YN} = \text{Tan}^{-1}\frac{\text{VRY} \times 3.8}{(\text{VBY} \times 1.9) + 45}(\text{deg})$$

* The vector is determined taking the demodulator gain into account.

TC1 TINT control characteristic 1
TC2 TINT control characteristic 2

1. Input SG.C (see figure below) to pin 46. Measure the absolute angle with reference to the pin 18 output voltage, referring to the figure below.



2. Take the TINT data center part (08H data 3CH) to be reference angle "TC", determine the TINT DATA maximum and minimum values. TC1 and TC2 are defined as follows.
   TC1 = Tcmax – TC(deg)
   TC2 = TC – Tcmin(deg)

BTC1 baseband TINT characteristic 1
BTC2 baseband TINT characteristic 2

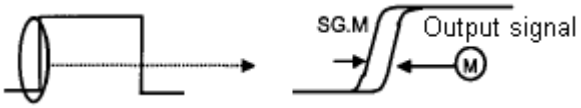
1. Input SG.M and SG.N to pin 48 and pins 40 & 44, respectively.
2. Set to YCbCr mode (11H data 02H).
3. The output amplitude of pin 18 when the baseband TINT is minimum (13H data 00H) is taken ~~to be~~as ~~-~~Crmin and Cbmin, respectively.
4. The output amplitude of pin 18 when the baseband TINT is at the center (13H data 40H) is taken as~~to be~~ Crtyp and Cbtyp, respectively.
5. The output amplitude of pin 18 when the baseband TINT is maximum (13H data 7FH) is taken as~~to be~~ Crmax and Cbmax, respectively.
6. BTC1 and BTC2 are defined as follows.

$$\text{BTC1} = \tan^{-1}\left(\frac{\text{Crtyp}}{\text{Cbtyp}}\right) - \tan^{-1}\left(\frac{\text{Crmin}}{\text{Cbmin}}\right)$$

$$\text{BTC2} = \tan^{-1}\left(\frac{\text{Crmax}}{\text{Cbmax}}\right) - \tan^{-1}\left(\frac{\text{Crtyp}}{\text{Cbtyp}}\right)$$

CrDL CrDL time 1
CbDL CbDL time 1

1. Input SG.M and SG.N to pin 48 and pins 40 & 44, respectively.
2. Set to YCbCr mode (11H data 02H).
3. Measure the delay time relative to the input signal of pin 18.



The delay time at 50% rise level is measured.

CrDL2,3,4 CrDL time 2,3,4
CbDL2,3,4 CbDL time 2,3,4

1. Input SG.M and SG.N to pin 48 and pins 40 & 44, respectively.
2. Set to YCbCr mode (11H data 02H) and measure the delay time of the input signal and the pin 18 output signal.
3. CrDL2, CrDL3, and CrDL4 are defined as follows.
   CrDL2 = measured value (ns) - CrDL1 (measured value)
   CrDL3 = measured value (ns) - CrDL2 (measured value)
   CrDL4 = measured value (ns) - CrDL3 (measured value)

Ffsc fsc output frequency 1, 2
Vfsc fsc output amplitude 1, 2

1. Input SG.C to pin 46.
2. Measure the output frequency and amplitude at pin 55 and pin 29.

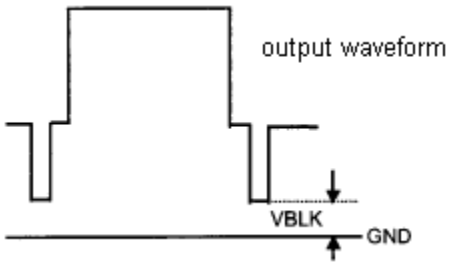
Ffscfree output frequency 1, 2 in fsc free mode
Vfscfree output amplitude 1, 2 in fsc free mode

1. Input SG.C to pin 46.
2. Measure the output frequency and amplitude at pin 55 and pin 29 with fsc free (07H D6) DATA 1.

RGB Interface Block

VBLK output blanking voltage

1. Input SG.A to pin 46.
2. Measure the voltage of the pin 14, 15, 16 pedestal and blanking parts.



GYmax contrast control characteristic 1
GYmin contrast control characteristic 2

1. Input SG.B (f = 100 kHz) to pin 46.
2. Measure the pin 14, 15, 16 output amplitude.

GYEnor contrast control characteristic 3
GYEmin contrast control characteristic 4

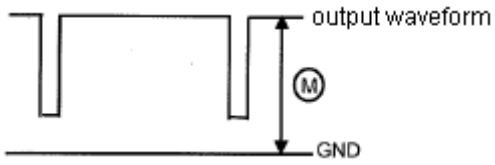
1. Input SG.A to pin 46.
2. Measure the pin 14, 15, 16 output amplitude when applying 2.9 V and 0 V to pin 18.

GYEclip contrast control characteristic 5

1. Input SG.F to pins 21, 22, 23, 24.
2. Minimize the contrast control data, and measure the output amplitude at and above the pedestal part of pins 14, 15, 16. The amplitude of the blanking part is not measured.

Lum nor brightness control characteristic 1
Lum max brightness control characteristic 2
Lum min brightness control characteristic 3

1. Input SG.D (Vy = 0 V) to pin 46.
2. Measure the DC voltage other than the blanking part of the output of pins 14, 15, 16.



D(R)1 R drive control characteristic 1

1. Input SG.A to pin 46.
2. Measure the pin 14 output amplitude when the drive control data is at center and is maximum, take the results to be DRnor and DRmax respectively.
3. D (R) 1 is defined as follows.

$$D(R)1 = 20 \log \frac{DRmax\ (Vp\text{-}p)}{DRnor\ (Vp\text{-}p)} (dB)$$

D(B)1 B drive control characteristic 1

1. Input SG.A to pin 46.
2. Measure the pin 16 output amplitude when the drive control data is at center and is maximum, take the results to be DBnor and DBmax respectively.
3. D(B)1 is defined as follows.

$$D(B)1 = 20 \log \frac{DBmax\ (Vp\text{-}p)}{DBnor\ (Vp\text{-}p)} (dB)$$

D(R)2 R drive control characteristic 2

1. Input SG.A to pin 46.
2. Measure the pin 14 output amplitude when the drive control data is at center and is minimum, take the results to be DRnor and DRmin respectively.
3. D(R)2 is defined as follows.

$$D(R)2 = 20 \log \frac{DRmin\ (Vp\text{-}p)}{DRnor\ (Vp\text{-}p)} (dB)$$

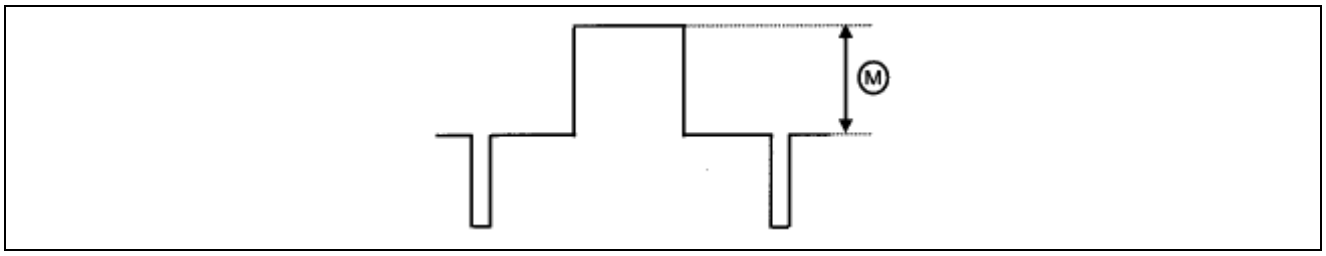
D(B)2 B drive control characteristic 2

1. Input SG.A to pin 46.
2. Measure the pin 16 output amplitude when the drive control data is at center and is minimum, take the results to be DBnor and DBmin respectively.
3. D(B)2 is defined as follows.

$$D(B)2 = 20 \log \frac{DBmin\ (Vp\text{-}p)}{DBnor\ (Vp\text{-}p)} (dB)$$

EXD(R) digital OSD(R) input/output characteristic
EXD(G) digital OSD(G) input/output characteristic
EXD(B) digital OSD(B) input/output characteristic

1. Input SG.F (Vosd=1.0 V) to pins 21, 22, 23, 24.
2. Measure the output amplitude at and above the pedestal part of pins 14, 15, 16. The amplitude of the blanking part is not measured.



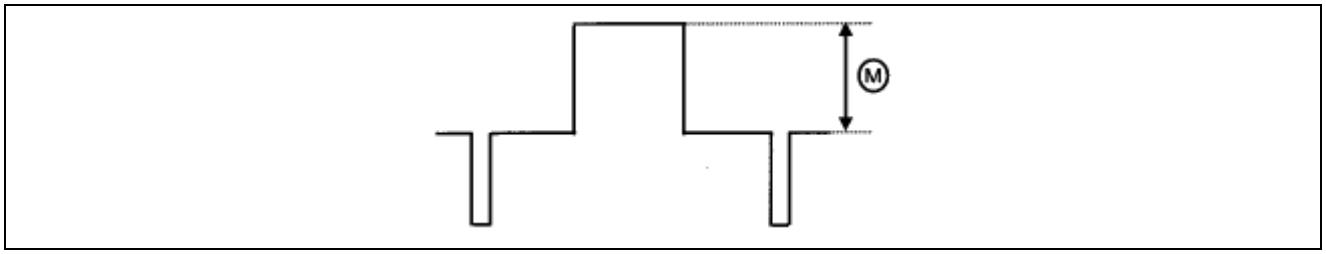
EXD(R-G) digital OSD (R-G) amplitude difference
EXD(G-B) digital OSD (G-B) amplitude difference
EXD(B-R) digital OSD (B-R) amplitude difference

1. EXD (R-G), EXD (G-B) and EXD (B-R) are defined as follows.

EXD(R-G) = EXD(R) – EXD(G)
EXD(G-B) = EXD(G) – EXD(B)
EXD(B-R) = EXD(B) – EXD(R)

EXA(R) analog OSD (R) input/output characteristic
EXA(G) analog OSD(G) input/output characteristic
EXA(B) analog OSD(B) input/output characteristic

1. Input SG.F (Vosd=0.7 V) to pins 21, 22, 23, 24.
2. Measure the output amplitude at and above the pedestal part of pins 14, 15, 16. The amplitude of the blanking part is not measured.



EXA(R-G) analog OSD (R-G) amplitude difference
EXA(G-B) analog OSD (G-B) amplitude difference
EXA(B-R) analog OSD (B-R) amplitude difference

1. EXA(R-G), EXA(G-B) and EXA(B-R) are defined as follows
   EXA(R-G) = EXA(R) – EXA(G)
   EXA(G-B) = EXA(G) – EXA(B)
   EXA(B-R) = EXA(B) – EXA(R)

C(R)1 R cutoff characteristic 1
C(G)1 G cutoff characteristic 1
C(B)1 B cutoff characteristic 1
C(R)2 R cutoff characteristic 2
C(G)2 G cutoff characteristic 2
C(B)2 B cutoff characteristic 2

1. Input SG.D (Vy = 0 V) to pin 46.
2. Measure the DC voltage of other than the blanking part in the outputs of pins 14, 15, 16.

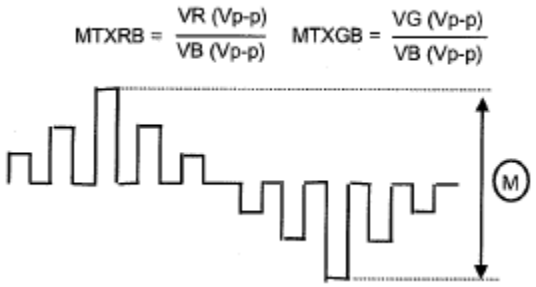
Ccon1 color control characteristic 1
Ccon2 color control characteristic 2
Ccon3 color control characteristic 3

1. Input SG.C to pin 46.
2. Measure the output amplitudes of pins 14, 15, 16 when IIC DATA 09H=40h, take the results as Ccon0.
3. Measure the output amplitudes of pins 14, 15, 16 under each set of conditions.
4. Ccon1, Ccon2, Ccon3 are defined as follows.

$$\text{Ccon1,Ccon2,Ccon3} = 20 \log \frac{\text{measured value (Vp-p)}}{\text{Ccon0 (Vp-p)}} \text{ (dB)}$$

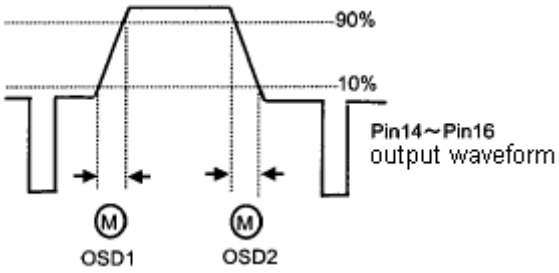
MTXRB matrix ratio R/B
MTXGB matrix ratio G/B

1. Input SG.G (rainbow color bar) to pin 46.
2. Measure the output amplitude when pins 14, 15, 16 are respectively VR, VG, VB.
3. MTXRB and MTXGB are defined as follows.



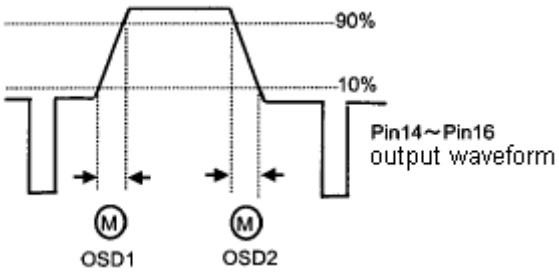
DOSD1 digital OSD switching characteristic 1
DOSD2 digital OSD switching characteristic 2

1. Input SG.F (Vosd=1.0 V) to pins 24, 21, 22, 23.
2. Measure the rise time and fall time of the output signals of pins 14, 15, 16 at and above the pedestal level. The blanking part is not measured.



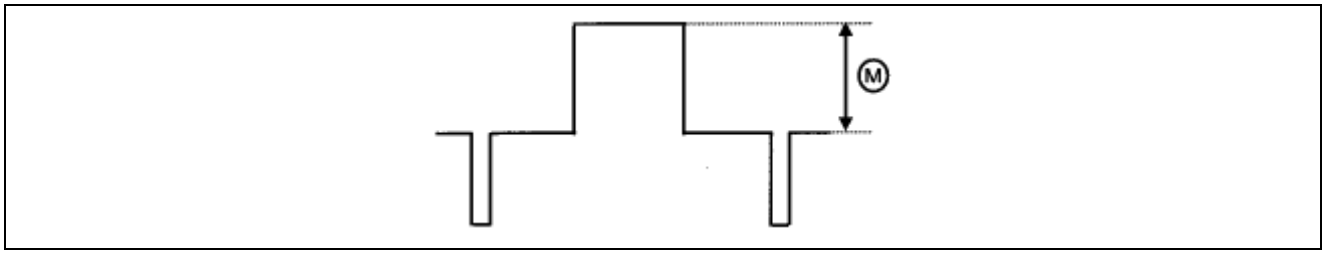
AOSD1 analog OSD switching characteristic 1
AOSD2 analog OSD switching characteristic 2

1. Input SG.F (Vosd = 0.7 V) to pins 24, 21, 22, 23.
2. Measure the rise time and fall time of the output signals of pins 14, 15, 16 at and above the pedestal level. The blanking part is not measured.



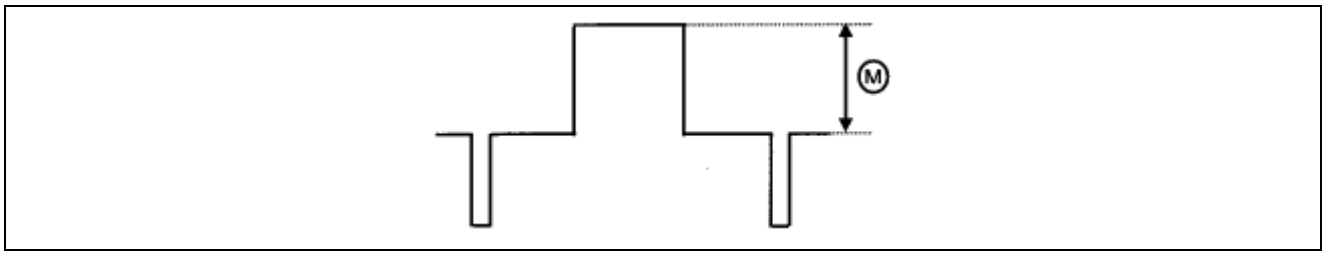
BB(R) blue back function (R)
BB(G) blue back function (G)
BB(B) blue back function (B)

1. Input SG.A to pin 46.
2. Measure the output amplitude (p-p) of pins 14, 15, 16 other than the blanking part.



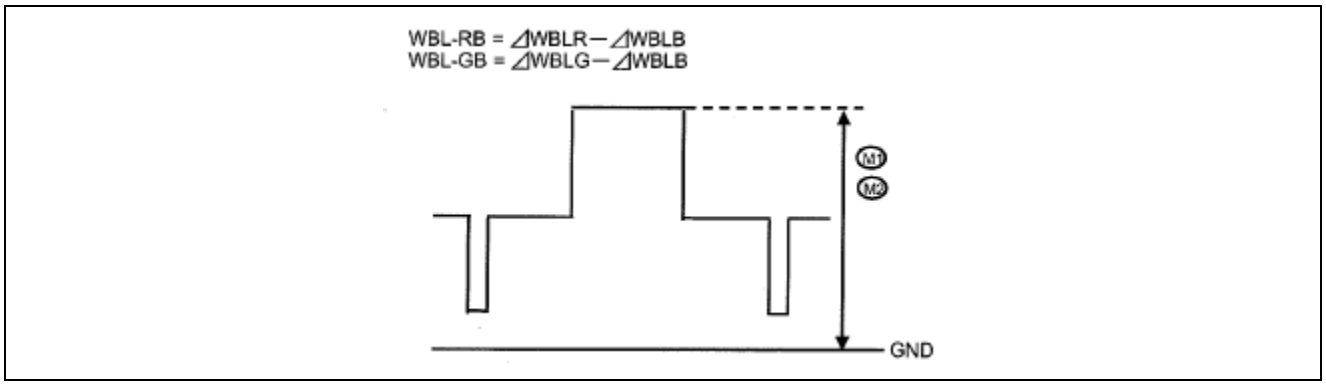
WB white raster function

1. Input SG.A to pin 46.
2. Measure the output amplitude (p-p) of pins 14, 15, 16 other than the blanking part.



WBL-RB white balance difference-RB
WBL-GB white balance difference-GB

1. Input SG.A (Y = 30%L with burst) to pin 46.
2. Measure the pin 14, 15, 16 output white level potential from GND. Measured values are taken to be M1R, M1G, M1B respectively.
3. Input SG.A (Y = 30%: without burst) to pin 46.
4. Measure the pin 14, 15, 16 output white level potential from GND. Measured values are taken to be M2R, M2G, M2B respectively.
5. Calculate the differences in measured values.
6. Calculate the differences between calculated values of Rch and Bch with the Bch measured value as reference, defined as follows.



Deflection Block

fH1 horizontal free-running frequency 1
fH2 horizontal free-running frequency 2
fH3 horizontal free-running frequency 3

1. Measure the frequency of pin 8 with no input.

Hfree forced horizontal free-running operation

1. Input SG.A to pin 46.
2. Set H-FREE CONTROL DATA to on, measure the frequency at pin 8.

FPHU horizontal pull-in range (upper)
FPHL horizontal pull-in range (lower)

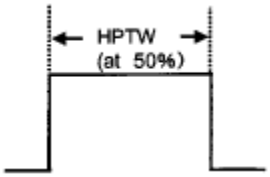
1. Input SG.H to pin 46.
2. Change the frequency of SG.H, measure the frequency range for which the pin 8 output signal and pin 46 input signal are pulled in, with respect to the video signal horizontal frequency.

HPT1 horizontal pulse timing 1

HPT2 horizontal pulse timing 2

1. Measure the horizontal pulse timing using the method for HPT1.
2. Standard
   HPT2 = (measured value) – HPT1

HPTW horizontal pulse width



AFCG AFC gain operation

1. Measure the pin 38 output amplitude during AFC switching, taking the result when 12HD0 = 1, D1 = 1, D2 = 0 to be AFCtyp, and 12H D0 = 1, D1 = 1, D2 = 1 to be AFCmax.
2. AFCG is defined as follows.

$$AFCG = 20 \log \frac{AFCmax\ (Vp\text{-}p)}{AFCtyp\ (Vp\text{-}p)}\ (dB)$$

fV vertical free-running frequency

1. Measure the pin 20 output frequency with no input.

Vfree forced vertical free-running operation

1. Input SG.A to pin 46.
2. Set V-FREE CONTROL DATA to on, measure the pin 20 output amplitude.

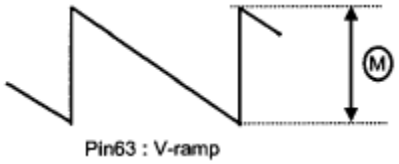
SCV service mode operation

1. Measure the pin 63 output DC voltage with the service switch on.

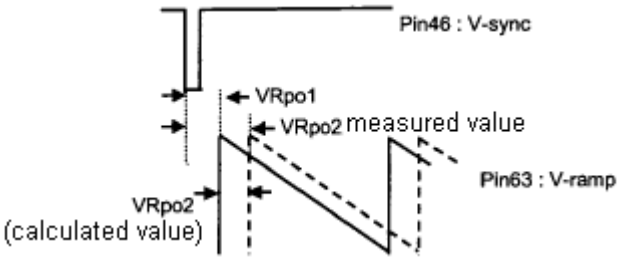
FPVU vertical pull-in frequency (upper)
FVPL vertical pull-in frequency (lower)

1. Change the SG.H vertical frequency, and measure the frequency when the pin 20 output waveform is pulled in.

VRsi vertical ramp size
VRsc1 vertical ramp size control range 1
VRsc2 vertical ramp size control range 2



VRpo1 vertical ramp position control range 1

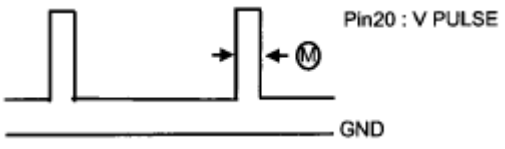


VRpo2 vertical ramp position control range 2

1. Measure the vertical ramp timing using the same method as for VRpo1.
2. VRpo2 is defined as follows.

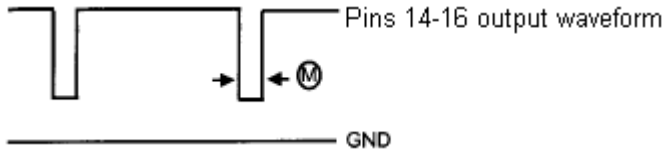
VRpo2 = (measured value) - VRpo1

VW vertical pulse width



VBLKW vertical BLK width
VBLKW1-4 vertical BLK width 1-4

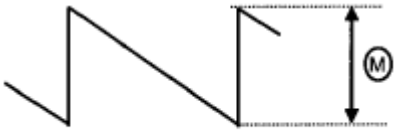
1. VBLKW: Measure the vertical BLK width with V BLK Wide (10H D4 = 0).
2. VBLKW1-4: Measure the vertical BLK width when V Blk Wide Top(10H D3, D2) and V Blk Wide Bottom(10H D1, D0) have been changed with V BLK Wide(10H D4 = 1)



WVSS minimum width at minimum sync operation

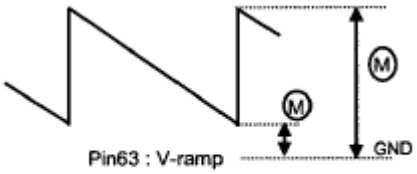
1. Reduce the width of the SG.I signal, and measure the input signal width when the pin 63 output waveform pull-in is lost.

VSco1 vertical S-correction control range 1
VSco2 vertical S-correction control range 2



VSco1,VSco2=(measured value) – VRsi1

VLt vertical linearity top voltage
VLb vertical linearity bottom voltage
VLcot1 vertical linearity top voltage control range 1
VLcot2 vertical linearity top voltage control range 2
VLcob1 vertical linearity bottom voltage control range 1
VLcob2 vertical linearity bottom voltage control range 2



VLcot1,VLcot2=(measured value) – VLt
VLcob1,VLcob2=(measured value) – VLb

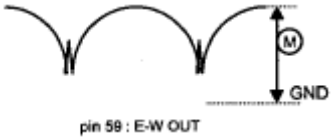
EW P parabola size
EW Pco1 parabola control range 1
EW Pco1 parabola control range 2

EW Cco1 corner control range 1
EW Cco1 corner control range 2

EW Ta trapezoid bottom voltage a
EW Tb trapezoid bottom voltage b
EW Tcoa1 trapezoid control range a1
EW Tcoa2 trapezoid control range a2
EW Tcob1 trapezoid control range b1
EW Tcob2 trapezoid control range b2

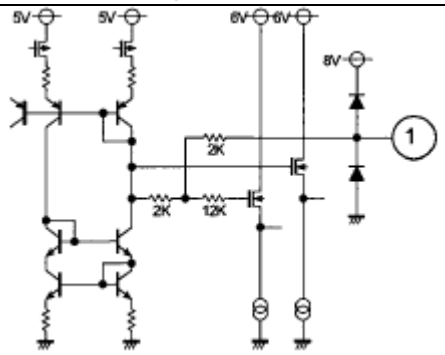
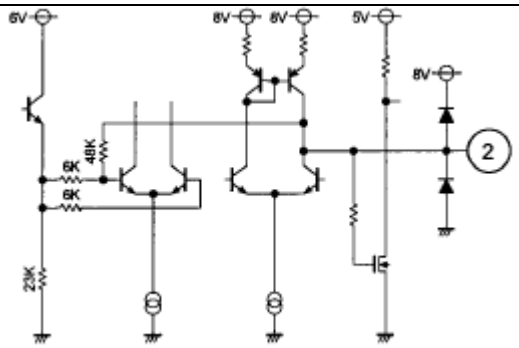
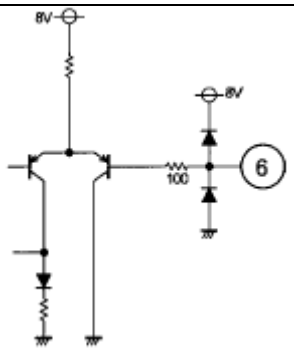
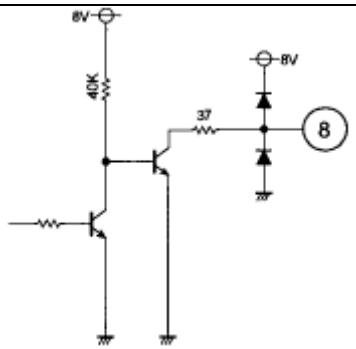
EW Tcoa1, EW T coa2 = (measured value) – EWTa
EW Tcob1, EW T cob2 = (measured value) – EWTb

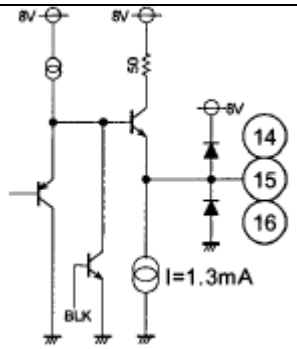
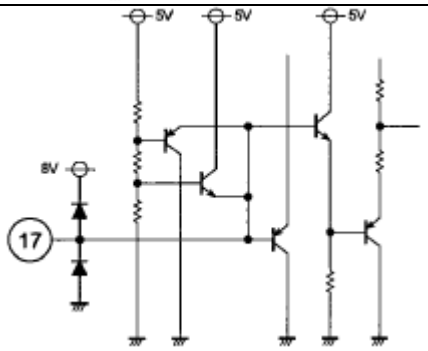
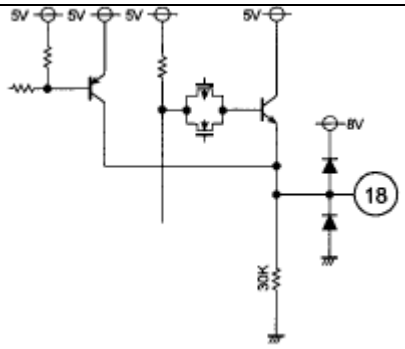
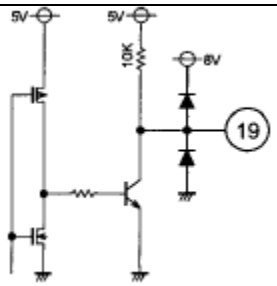
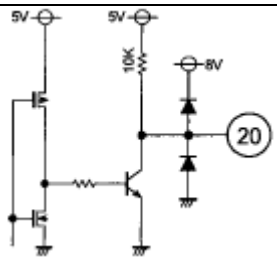
EW Si parabola top voltage
EW Sico1 horizontal size control range 1
EW Sico2 horizontal size control range 2

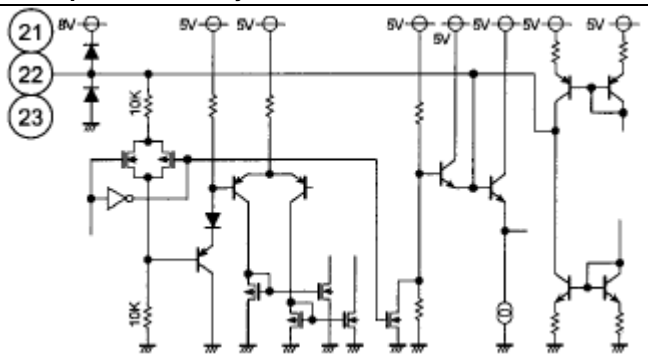
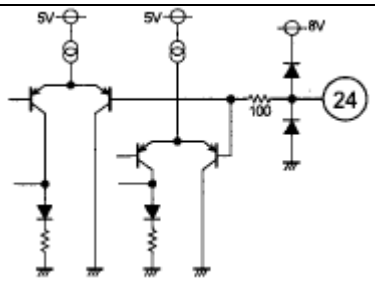
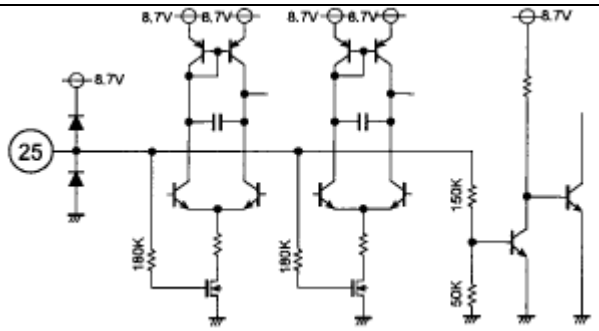
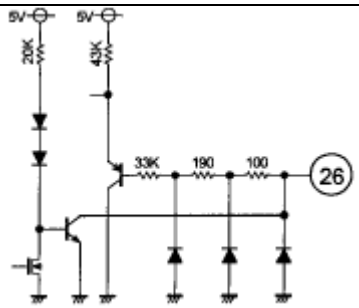
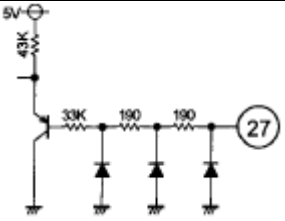
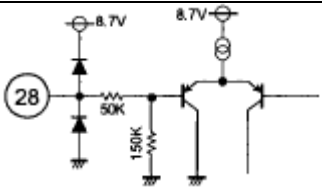


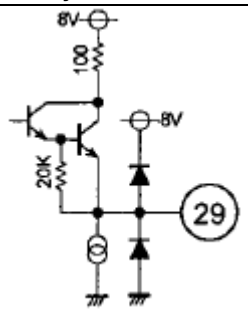
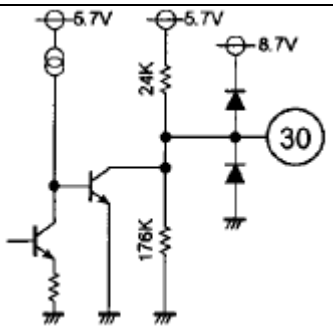
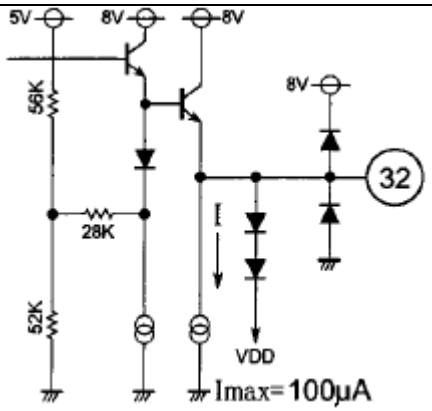
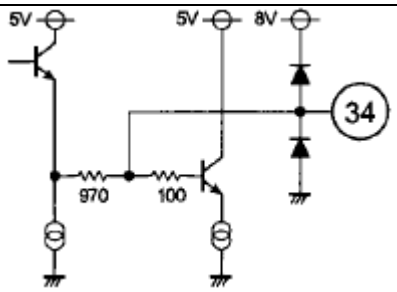
EW Sico1, EW T Sico2 = (measured value) – EWSi

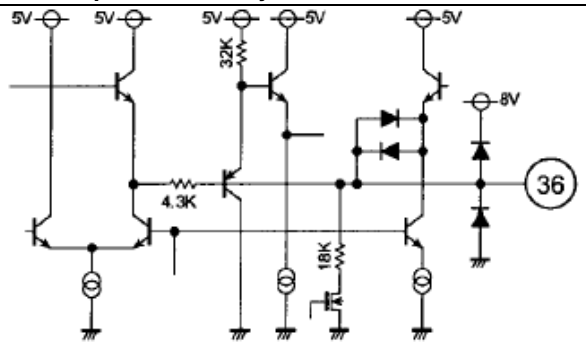
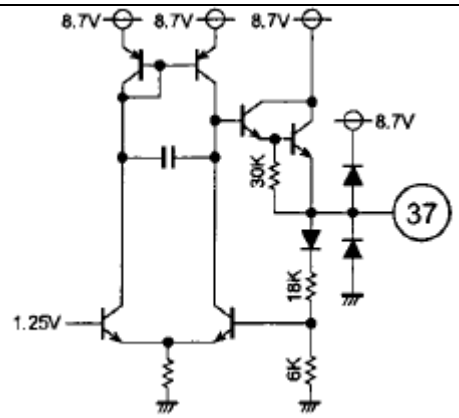
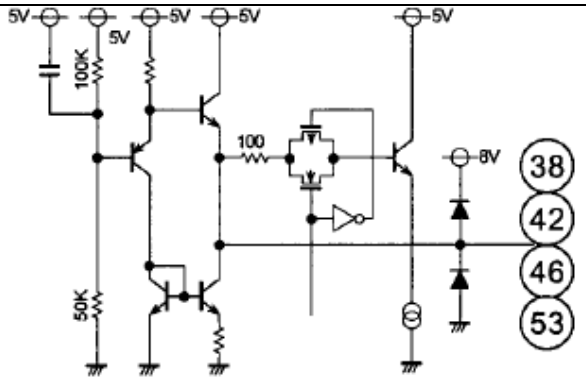
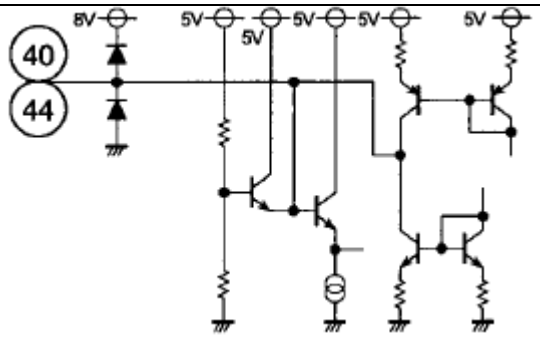
Pin Peripheral Circuit Diagram

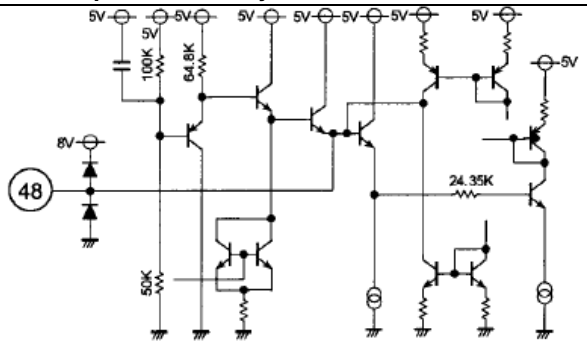
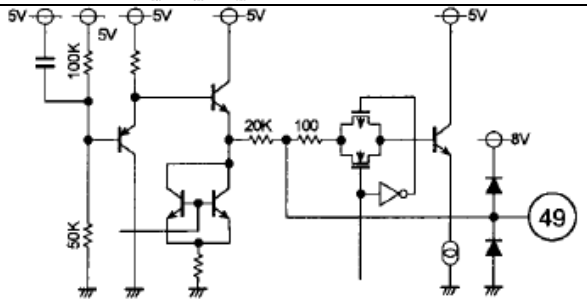
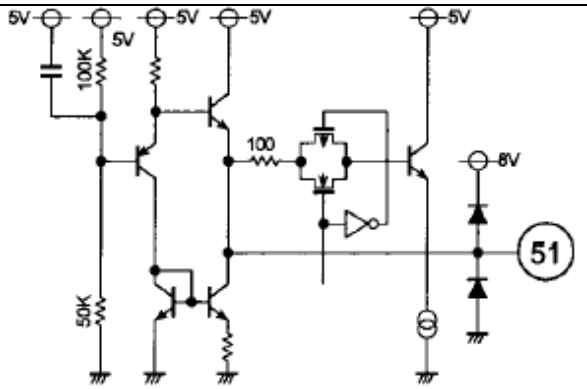
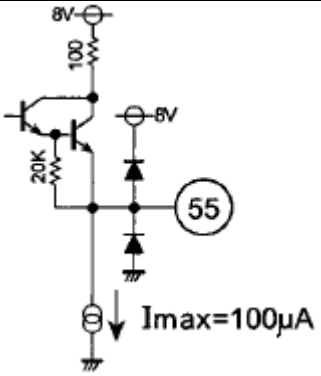
Pin no.	Name	Pin Peripheral Circuitry	Notes
1	H VCO FEEDBACK		3.0 V
2	AFC FILTER		3.5 V
3	LOGIC GND	—	0 V
4	DEF GND1	—	0 V
5	DEF GND2	—	0 V
6	FBP IN		V_{TH}: 1.0 V
7 9 11 12	NC	—	—
8	H OUT		Open collector output. Maximum inflow current must be 4 mA or less.

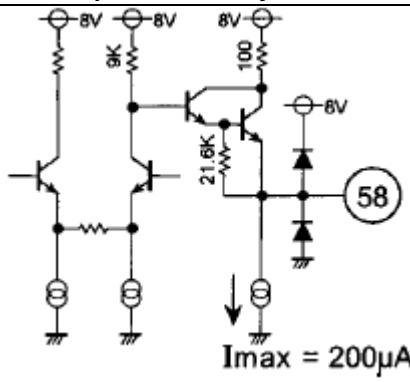
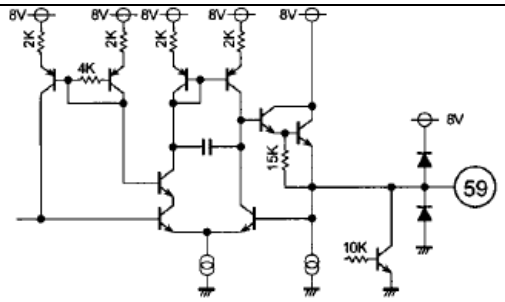
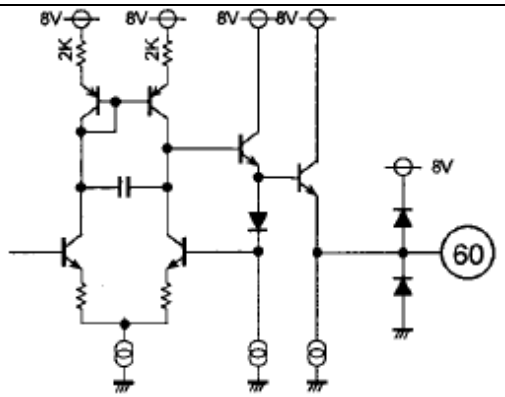
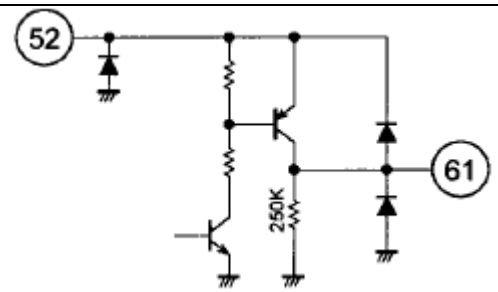
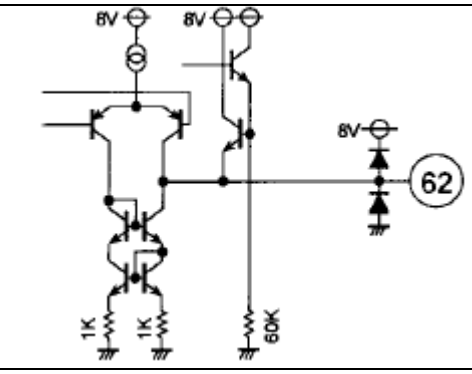
Pin no.	Name	Pin Peripheral Circuitry	Notes
10	DEF VCC	—	8 V
13	HI VCC	—	8 V
14 15 16	R OUT G OUT B OUT		—
17	ACL/ABCL		—
18	INTELLIGENT MONITOR		Maximum outflow current = 100 μA
19	HD OUT		V_{OL}: 0.0 V V_{OH}: 5.0 V
20	VD OUT		V_{OL}: 0.0 V V_{OH}: 5.0 V

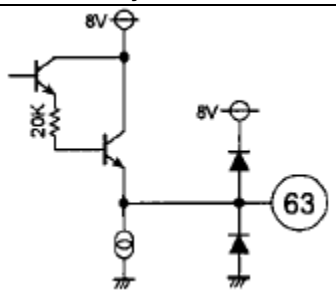
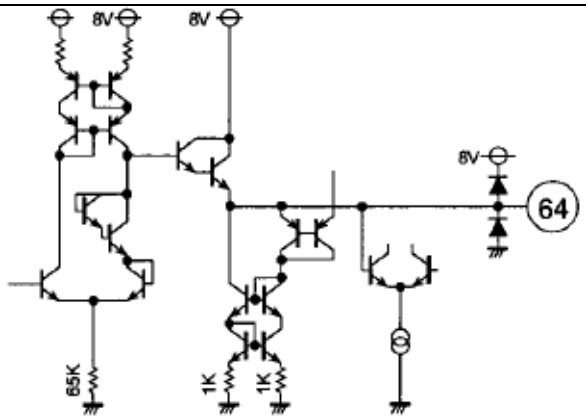
Pin no.	Name	Pin Peripheral Circuitry	Notes
21 22 23	OSD B IN OSD G IN OSD R IN		Digital OSD V_{IL}: 0.0 V V_{IH}: 3.0 V
24	FAST BLK		0.0-0.5 V: INT RGB 1.5-3.0 V: H TONE 4.0-5.0 V: EXT RGB
25	CLK CONT		5.0 V
26	SDA		V_{IL}: 0.75 V V_{IH}: 4.25 V
27	SCL		V_{IL}: 0.75 V V_{IH}: 4.25 V
28	P-ON CONT		5.0 V

Pin no.	Name	Pin Peripheral Circuitry	Notes
29	MCU fsc OUT		3.0 V
30	MCU RESET		H: 5.0 V L: 0.0 V
31	NC	—	—
32	Y SW OUT		1.7 V
33	Video/Chroma GND	—	0 V
34	X-TAL		3.3 V
35	NC	—	—

Pin no.	Name	Pin Peripheral Circuitry	Notes
36	CHROMA APC FILTER		3.2 V
37	MCU 5.7 V REG OUT		5.7 V Maximum outflow current = 2.5 mA
38 42 46 53	CVBS IN 3/2/1/4		1.7 V
39	NC	—	—
40 44	Cr IN(YCbCr) Cb IN(YCbCr)		2.8 V
41	Video/Chroma Vcc	—	5.0 V
43 45 47 50	NC	—	—

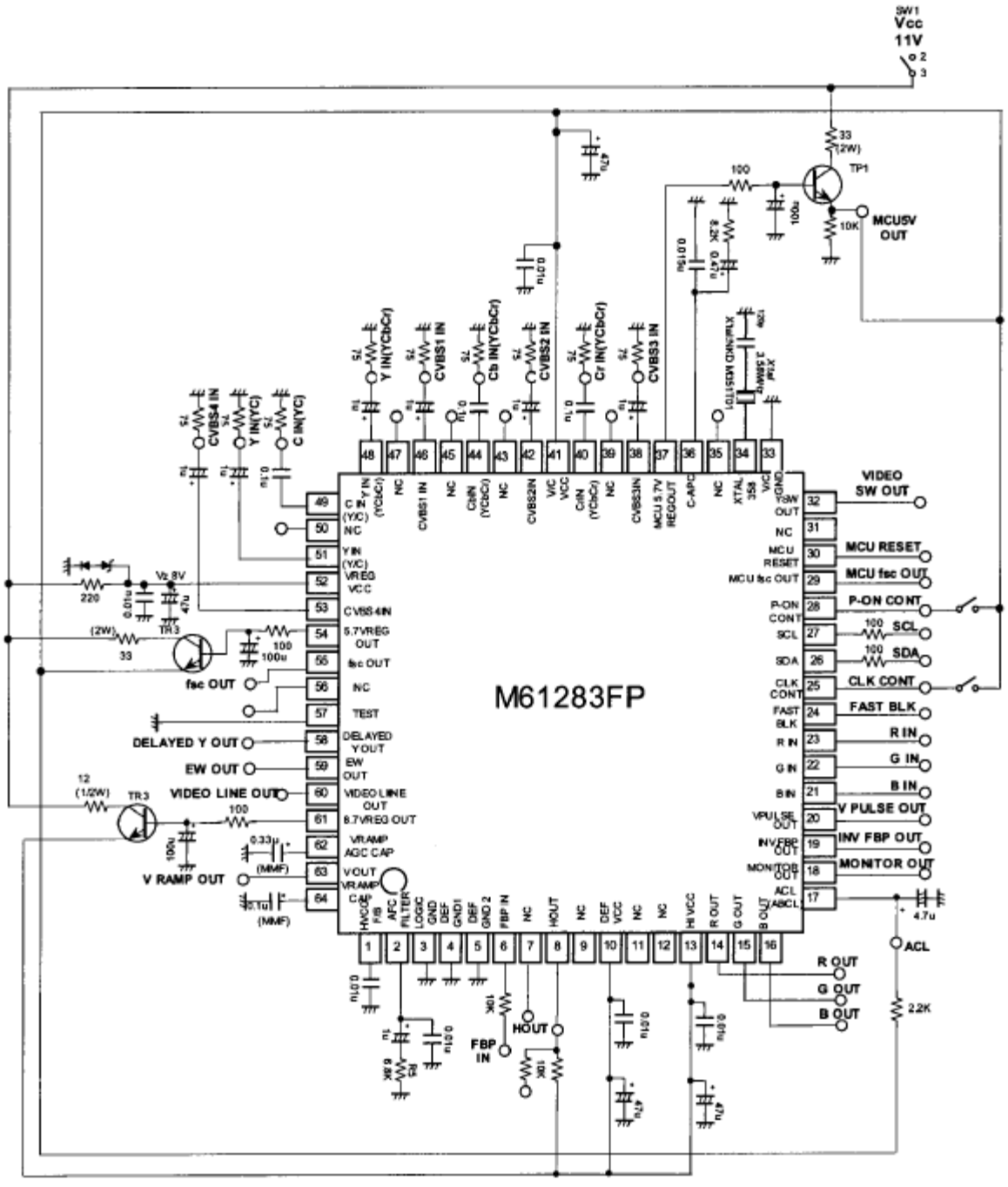
Pin no.	Name	Pin Peripheral Circuitry	Notes
48	Y IN(YCbCr)		1.7 V
49	C IN(Y/C)		1.7 V
50	NC	—	—
51	Y IN(Y/C)		1.7 V
52	VREG Vcc	—	8.7 V
54	5.7 V REG OUT	—	5.7 V
55	fsc OUT		3.0 V
56	NC	—	—
57	TEST	—	Connect this pin to GND.

Pin no.	Name	Pin Peripheral Circuitry	Notes
58	DELAYED Y OUT		2.3 V
59	E-W OUT		Operating range = 1.2V to 5.2V
60	VIDEO LINE OUT		1.7 V
61	8.7 V REG OUT		8.7 V Maximum outflow current = 1 mA
62	V RAMP AGC CAP		4 V

Pin no.	Name	Pin Peripheral Circuitry	Notes
63	V OUT		Operating range = 1.1V to 5.1V Maximum outflow current = 1 mA
64	V RAMP CAP		2.0 V to 4.0 V

Note: Voltage, current and other values appearing in the Notes column are reference values, and are not guaranteed rated values.

Application Example



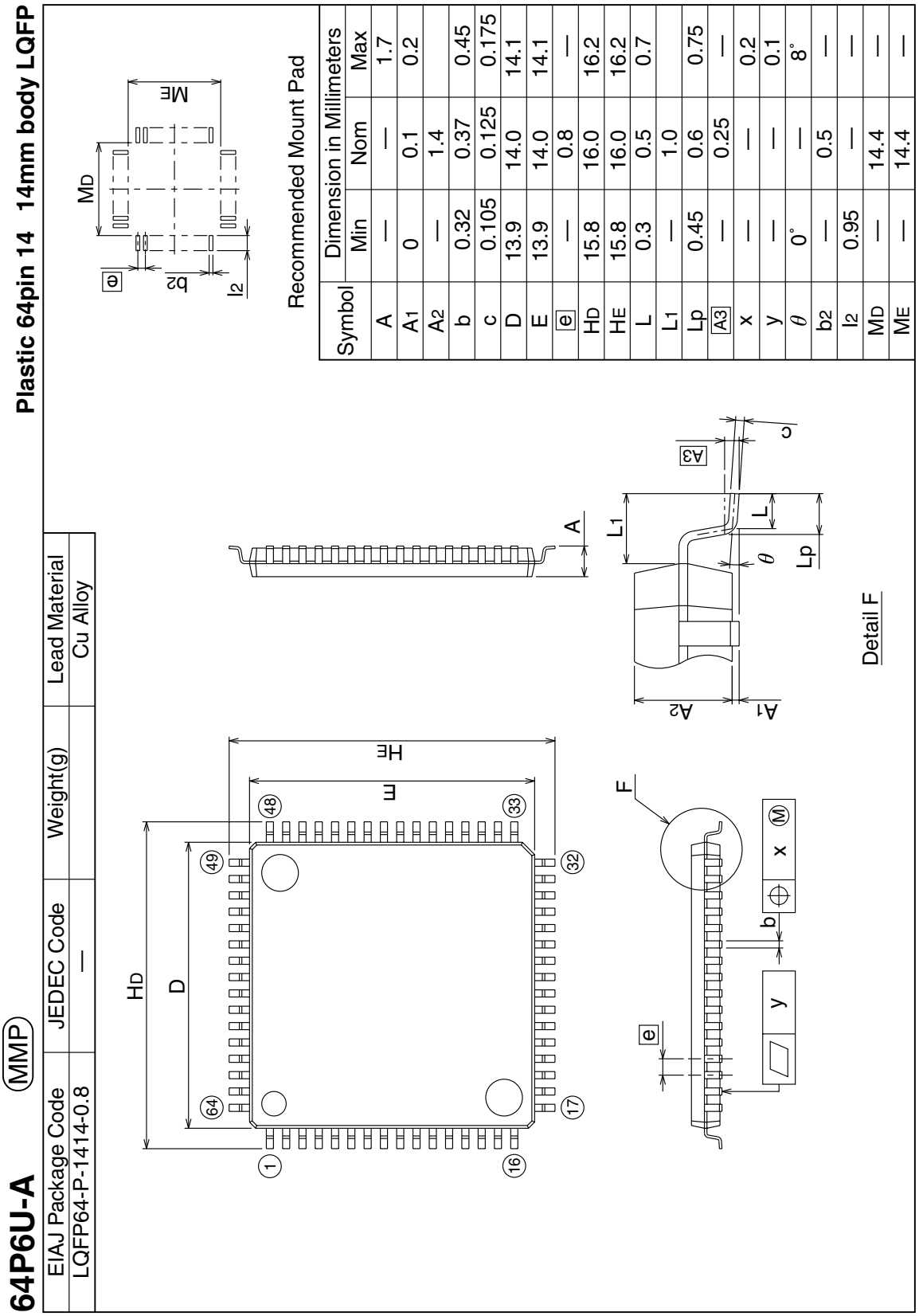
X1: N.K.D M351T01 (3.58MHz)

Note: If a crystal oscillator other than that recommended is used, the capacitance connected to X1 (3.58 MHz Xtal) must be studied.

Important Information

- Each application should be thoroughly studied and evaluated before making a decision.
- 47 μF and higher electrolytic capacitors and 0.01 μF and higher ceramic capacitors should be connected in parallel between each of the power supply pins (10, 13, 41, 52) and ground. In addition, it is recommended that the connections be made as close to the IC power supply pins as possible.
- Since pin37 (MCU5.7 V REG OUT) is weaker weaker electrostatic proof (+120V, -140V, based on the MM standard) than the other pins, an appropriate countermeasure should be taken on each application. (However, according to the HBM standard, + 1000 V or more and – 1000 V or less are assured)
- When purchasing I^2C bus components, a license to use these components within a I^2C bus system is provided under the I^2C patent rights of Philips Corp.
  However, the bus system must conform to the I^2C specifications stipulated by Philips.

Package Dimensions



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Colophon 1.0