QUAD/DUAL N-CHANNEL DEPLETION MODE EPAD® MATCHED PAIR MOSFET ARRAYS

$V_{GS(th)}$= -3.5V

GENERAL DESCRIPTION

ALD114835/ALD114935 are monolithic quad/dual N-Channel MOSFETs matched at the factory using ALD's proven EPAD CMOS technology. These devices are intended for low voltage, small signal applications. They are excellent functional replacements for normally-closed relay applications, as they are normally on (conducting) without any power applied, but could be turned off or modulated when system power supply is turned on. These MOSFETs have the unique characteristics of, when the gate is grounded, operating in the resistance mode for low drain voltage levels and in the current source mode for higher voltage levels and providing a constant drain current.

ALD114835/ALD114935 MOSFETs are designed for exceptional device electrical characteristics matching. As these devices are on the same monolithic chip, they also exhibit excellent temperature tracking characteristics. They are versatile as design components for a broad range of analog applications such as basic building blocks for current sources, differential amplifier input stages, transmission gates, and multiplexer applications. Besides matched pair electrical characteristics, each individual MOSFET also exhibits well controlled parameters, enabling the user to depend on tight design limits. Even units from different batches and different date of manufacture have correspondingly well matched characteristics.

These depletion mode devices are built for minimum offset voltage and differential thermal response, and they are designed for switching and amplifying applications in single 5V to +/-5V systems where low input bias current, low input capacitance and fast switching speed are desired. These devices exhibit well controlled turn-off and sub-threshold charactersitics and therefore can be used in designs that depend on sub-threshold characteristics.

The ALD114835/ALD114935 are suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. A sample calculation of the DC current gain at a drain current of 3mA and gate input leakage current of 30pA = 100,000,000. It is recommended that the user, for most applications, connect V+ pin to the most positive voltage potential (or left open unused) and V- and N/C pins to the most negative voltage potential in the system. All other pins must have voltages within these voltage limits.

FEATURES

- Depletion mode (normally ON)
- Precision Gate Threshold Voltages: -3.50V +/- 0.05V
- Nominal $R_{DS(ON)}$ @V_{GS}=0.0V of 540Ω
- Matched MOSFET to MOSFET characteristics
- Tight lot to lot parametric control
- Low input capacitance
- $V_{GS(th)}$ match (V_{OS}) — 20mV
- High input impedance — 10^{12}Ω typical
- Positive, zero, and negative $V_{GS(th)}$ temperature coefficient
- DC current gain >10^8
- Low input and output leakage currents

ORDERING INFORMATION

Operating Temperature Range* 0°C to +70°C		0°C to +70°C	
16-Pin Plastic Dip Package	16-Pin SOIC Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD114835PC	ALD114835SC	ALD114935PA	ALD114935SA

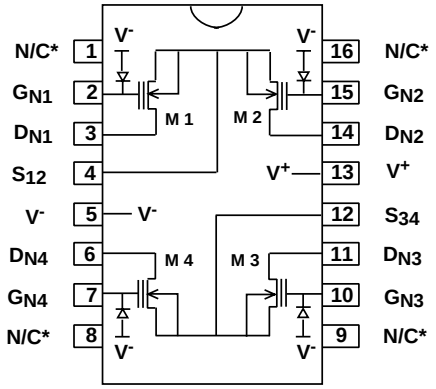
* Contact factory for industrial temp. range or user-specified threshold voltage values

APPLICATIONS

- Functional replacement of Form B (NC) relay
- Zero power fail safe circuits
- Backup battery circuits
- Power failure detector
- Fail safe signal detector
- Source followers and buffers
- Precision current mirrors
- Precision current sources
- Capacitives probes
- Sensor interfaces
- Charge detectors
- Charge integrators
- Differential amplifier input stage
- High side switches
- Peak detectors
- Sample and Hold
- Alarm systems
- Current multipliers
- Analog switches
- Analog multiplexers
- Voltage comparators
- Level shifters

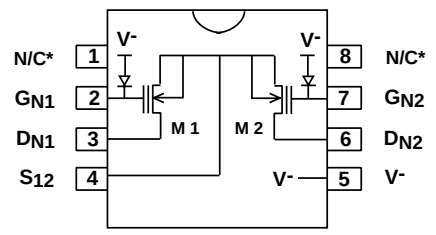
PIN CONFIGURATION

ALD114835



PC, SC PACKAGES

ALD114935



PA, SA PACKAGES

*N/C pins are internally connected.
Connect to V- to reduce noise

ABSOLUTE MAXIMUM RATINGS

Drain-Source voltage, V_{DS} ——— 10.6V
Gate-Source voltage, V_{GS} ——— 10.6V
Power dissipation ——— 500 mW
Operating temperature range PA, SA, PC, SC package ——— 0°C to +70°C
Storage temperature range ——— -65°C to +150°C
Lead temperature, 10 seconds ——— +260°C

OPERATING ELECTRICAL CHARACTERISTICS

V+ = +5V (or open) V- = -5V TA = 25°C unless otherwise specified

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

Parameter	Symbol	ALD114835 / ALD114935 Min	Typ	Max	Unit	Test Conditions
Gate Threshold Voltage	$V_{GS(th)}$	-3.55	-3.50	-3.45	V	I_{DS} =1μA V_{DS} = 0.1V
Offset Voltage $V_{GS(th)1}$ - $V_{GS(th)2}$	V_{OS}		7	20	mV	
Offset Voltage Tempco	TCV_{OS}		5		μV/ °C	V_{DS1} = V_{DS2}
GateThreshold Voltage Tempco	$TCV_{GS(th)}$		-1.7 0.0 +1.6		mV/ °C	I_D = 1μA, V_{DS} = 0.1V I_D = 20μA, V_{DS} = 0.1V I_D = 40μA, V_{DS} = 0.1V
On Drain Current	$I_{DS\ (ON)}$		12.0 3.0		mA	V_{GS} = +6.0V, V_{DS} =+5V V_{GS} = +0.5V, V_{DS} =+5V
Forward Transconductance	G_{FS}		1.4		mmho	V_{GS} = +0.5V V_{DS} = +5.5V
Transconductance Mismatch	ΔG_{FS}		1.8		%	
Output Conductance	G_{OS}		68		μmho	V_{GS} =+0.5V V_{DS} = +5.5V
Drain Source On Resistance	$R_{DS\ (ON)}$		540		Ω	V_{DS} = +0.1V V_{GS} = +0.0V
Drain Source On Resistance Tolerance	$\Delta R_{DS\ (ON)}$		5		%	
Drain Source On Resistance Mismatch	$\Delta R_{DS\ (ON)}$		0.5		%	
Drain Source Breakdown Voltage	BV_{DSX}	10			V	I_{DS} = 1.0μA V_{GS} = -4.5V
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$		10	100 4	pA nA	V_{GS} = -4.5V, V_{DS} =+5V T_A = 125°C
Gate Leakage Current[1]	I_{GSS}		3	30 1	pA nA	V_{DS} = 0V V_{GS} = +10V T_A =125°C
Input Capacitance	C_{ISS}		2.5		pF	
Transfer Reverse Capacitance	C_{RSS}		0.1		pF	
Turn-on Delay Time	t_{on}		10		ns	V^+ = 5V R_L= 5KΩ
Turn-off Delay Time	t_{off}		10		ns	V^+ = 5V R_L= 5KΩ
Crosstalk			60		dB	f = 100KHz

Notes: [1] Consists of junction leakage currents