

The AP9050 is available in a low-profile U-DFN2020-6 package.

U-DFN2020-6

- Input Supply Range from 3V to 30V
- Lower Power Dissipation and Higher Efficiency as compared to a Zener Shunt Regulator
- LDO is stable without a bypass capacitor on the output and operates across the temperature range
- Available in a U-DFN2020-6 package with a typical height of 0.575mm

- Power Interface for New Generation PMICs
- Charger Front End Protection
- Smartphone
- Cell Phone
- Ultra Mobile PC
- Tablets

Figure 1. Typical Application Circuit

Pin Descriptions

Pin #	Name	Description
1	Source	Source of the n-channel power FET. Pass-switch's output pin.
2	Gate	Gate of the FET switch. Pass-switch's control pin.
3, 7	V_{IN}	Input voltage to the internal LDO.
4	Ground	LDO ground connection.
5	V_{OUT}	Output of the LDO.
6, 8	Drain	Drain of the power FET. Pass-switch's input pin.

Functional Block Diagram

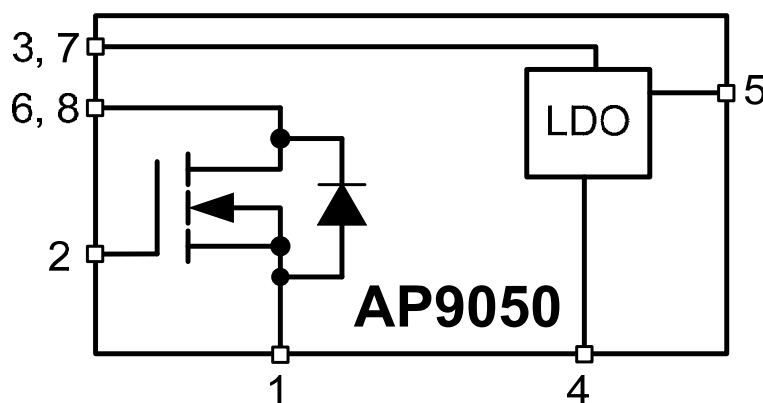


Figure 2. Functional Block Diagram

Absolute Maximum Ratings (Note 2, 3)

Symbol	Parameter	Rating	Unit
V_{IN}	Supply Voltage	-0.3 to 30	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_{Dpk}	Drain Current, Peak (10 μ s pulse)	19	A
I_D	Drain Current, Continuous (Note 4, Steady-State) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	3.7 2.7	A
P_{max}	Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 3, 4)	750	mW
T_J	Junction Temperature Range	-40 to +125	$^\circ\text{C}$
T_J	Non-operating Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes	260	$^\circ\text{C}$

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

- Notes:
- Exceeding these ratings may damage the device.
 - Mounted on FR4 Board using 30 mm², 2 oz Cu.
 - Dual die operation (equally-heated).

Thermal Resistance

Symbol	Parameter	Rating	Unit
θ_{JA}	Junction to Ambient (Note 5)	132	$^\circ\text{C/W}$
θ_{JC}	Junction to Case	13	$^\circ\text{C/W}$

Note: 5. Test condition for DFN2020-6: Mounted on FR4 Board using 30 mm², 2 oz Cu.

Recommended Operating Conditions (Note 6)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	3	30	V
T_A	Operating Ambient Temperature Range	-40	+85	$^\circ\text{C}$

Note: 6. The device function is not guaranteed outside of the recommended operating conditions.

**PROTECTION INTERFACE for PMICs with
 INTEGRATED OVP CONTROL**
Electrical Characteristics (V_{IN} (OVP_SENSE) = 5.0V, T_J = +25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Power FET						
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24V, V _{GS} = 0V T _J = 85°C			1.0 10	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0V, V _{GS} = ±8V			80	nA
V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250μA	0.62	0.9	1.2	V
R _{DS(on)}	Drain-to-Source On-Resistance (Note 7)	V _{GS} = 4.5V, I _D = 2.0A V _{GS} = 2.5V, I _D = 2.0A		41 55	53 68	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 5V, I _D = 2.0A		8		S
C _{ISS}	Input Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz		500		pF
C _{OSS}	Output Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz		65		pF
C _{RSS}	Reverse Transfer Capacitance	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz		50		pF
LDO (unless otherwise noted, T _J = 25°C, V _{IN} = 5.0V)						
V _{OUT}	Regulated Output Voltage	V _{IN} = 5.5V, I _{OUT} = 1mA	4.6	5.0	5.3	V
V _{head}	Headroom	V _{IN} - V _{OUT} , I _{OUT} = 1.2mA, V _{IN} = 4.6V			150	mV
		V _{IN} - V _{OUT} , I _{OUT} = 10mA, V _{IN} = 4.8V, T _J = -40 to +125°C			1000	mV
Response to Input Transient						
t _{pulse}	Time signal is above 5.5V	V _{IN} 0 to 30V, < 1μs rise time, 5.0kΩ resistive load (Note 8)			5.0	μs
V _{pk}	Peak Voltage	V _{IN} 0 to 30V, < 1μs rise time, 5.0kΩ resistive load (Note 8)			9.0	V
Total Device						
I _{bias}	Input Bias Current	V _{IN} = 5.5V		110	850	μA
V _{IN_min}	Minimum Operating Voltage				3.0	V

Notes: 7. Pulse test width 300 μs , duty cycle 2%
 8. Guaranteed by design

Typical Performance Characteristics

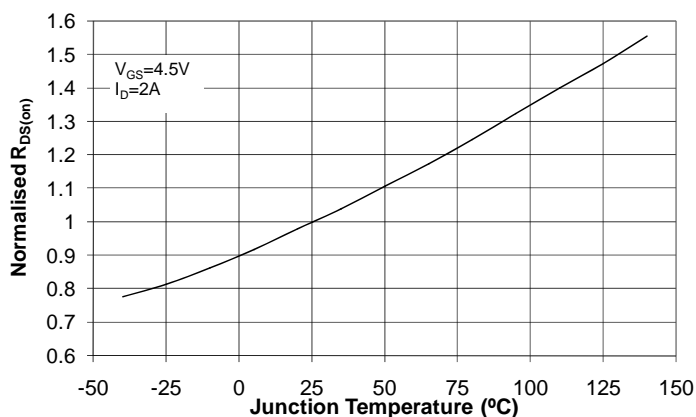


Figure 3. $R_{DS(on)}$ variation over junction temperature

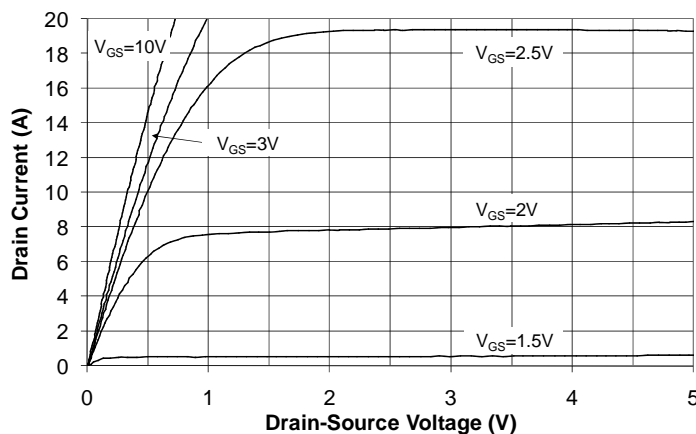


Figure 4. $R_{DS(on)}$ Characteristics

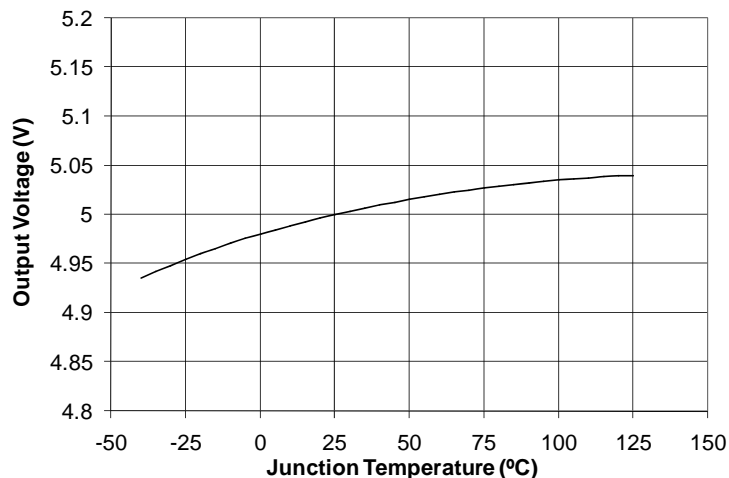


Figure 5. Output voltage variation over junction temperature

Applications Information

Theory of Operation

The AP9050 was designed to work in close relationship with a PMIC (Power Management IC). To protect the PMIC from an overvoltage situation the AP9050 powers up a detection circuit within the connected PMIC. (See Figure 2 as reference)

This detection circuit determines if a valid input source is connected (ex. $V_{IN} < 8V$). If a valid input source is detected the power MOSFET will be turned on and the supply current to the PMIC will be turned on. The overvoltage detection is continuous, if an overvoltage occurs at a later state the Power MOSFET will be turned off.

External Capacitors

AP9050 was specified to reduce board space and external component count, by designing the LDO to be stable without an external bypass capacitor.

A low ESR 1nF to 10nF external capacitor can be used to improve behavior with fast ac transients or other switching currents that might be present.

To improve noise immunity and ac impedance from long input traces a 1nF capacitor can be added to the input V_{IN} of the LDO.

PCB Layout

The AP9050 was designed utilizing two process technologies to provide best performance and a cost effective solution.

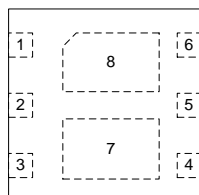
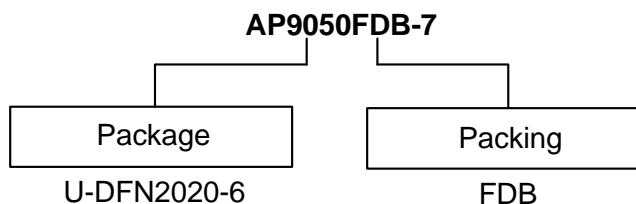


Figure 6. Package Pin Out

Both die are packaged side by side in the U-DFN2020-6 package and are mounted on two separate exposed pads. These pads are not required for electrical functionality, but to aid with the thermal performance of AP9050.

Attention should be paid in the layout of the PCB (Printed Circuit Board) that PAD7 is connected to V_{IN} of the LDO, pin 3, while PAD8 is connected to the Drain of the Power MOSFET, pin 6 of the package. For best thermal performance large copper areas connected to the two exposed pads should be used to transfer heat away from the AP9050.

Ordering Information



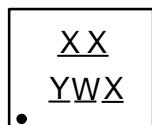
Device	Package Code	Packaging (Note 10)	7" Tape and Reel	
			Quantity	Part Number Suffix
AP9050FDB-7	FDB	U-DFN2020-6	3000/Tape & Reel	-7

Note: 10. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

Marking Information

U-DFN2020-6

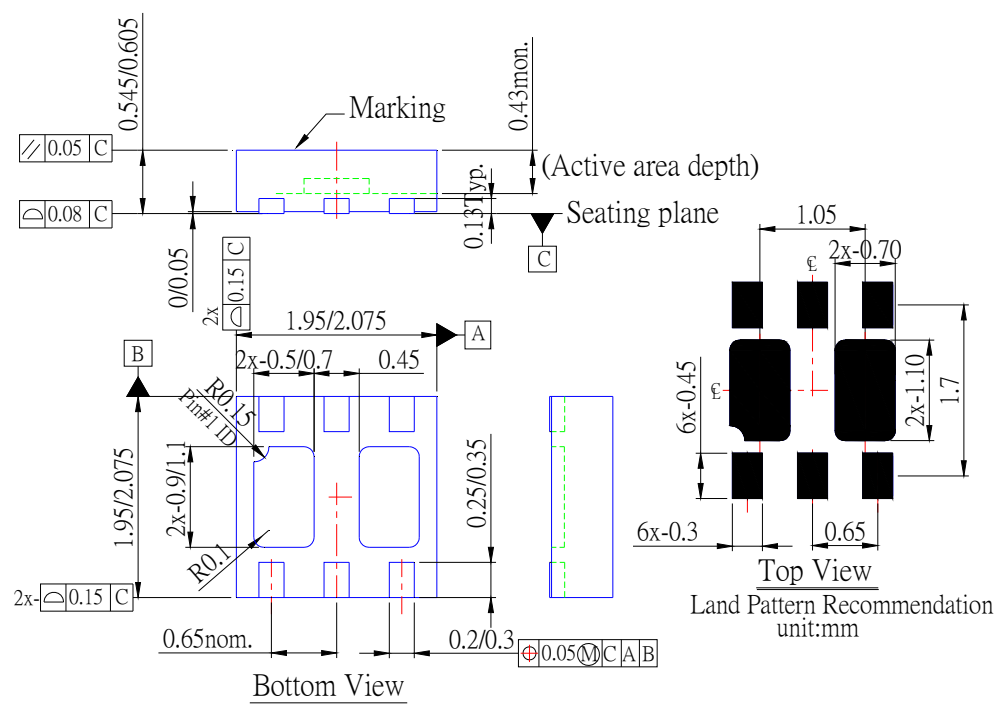
(Top View)



XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : A~Z : Internal code

Device	Package	Identification Code
AP9050FDB	U-DFN2020-6	BZ

U-DFN2020-6



**PROTECTION INTERFACE for PMICs with
INTEGRATED OVP CONTROL****IMPORTANT NOTICE**

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

Copyright © 2011, Diodes Incorporated

www.diodes.com