

TCM8210MD (A)

TENTATIVE

VGA CAMERA MODULE

The TCM8210MD(A) is a camera module which includes area color image sensor embedded with camera signal processor that meets with VGA format. In the sensor area 492 vertical and 660 horizontal signal pixels, and the image size meets with 1/4 inch optical Format. Use of the CMOS process enables low power consumption operations. It also provides excellent color reproduction through its primary color filter, and embedded camera signal processor enables small and simple camera system. And this module can be assembled by the socket which is suitable for the reflow soldering. So it is fit to use as an image input device for digital still cameras, PC cameras and mobile devices.

Features

1. General

- Module size : 10(W) x 10(D) x 5.8(H) mm
- Many kinds of clock frequency is available by PLL operation
- Sleep mode operation is available (It can be controlled by the command)
- Built-in IIC BUS I/F
- Power supply : 2.8+/-0.2V

2. Sensor

- Optical size : 1/4 inch optical format
- Total pixel numbers : 698(H)x502(V)
- Signal pixel numbers : 660(H)x492(V)
- Pixel pitch : 5.4um(H)x5.4um(V) (square pixel)
- Image size : 3.564mm(H) x 2.657mm(V)
- Color filter : Primary color filter, Bayer arrangement (GR line and GB line are arranged alternately.)
- Frame frequency : Max 30fps
- Raw data bit precision : 10bit
- Built-in feed back clamp

3. Camera signal processing

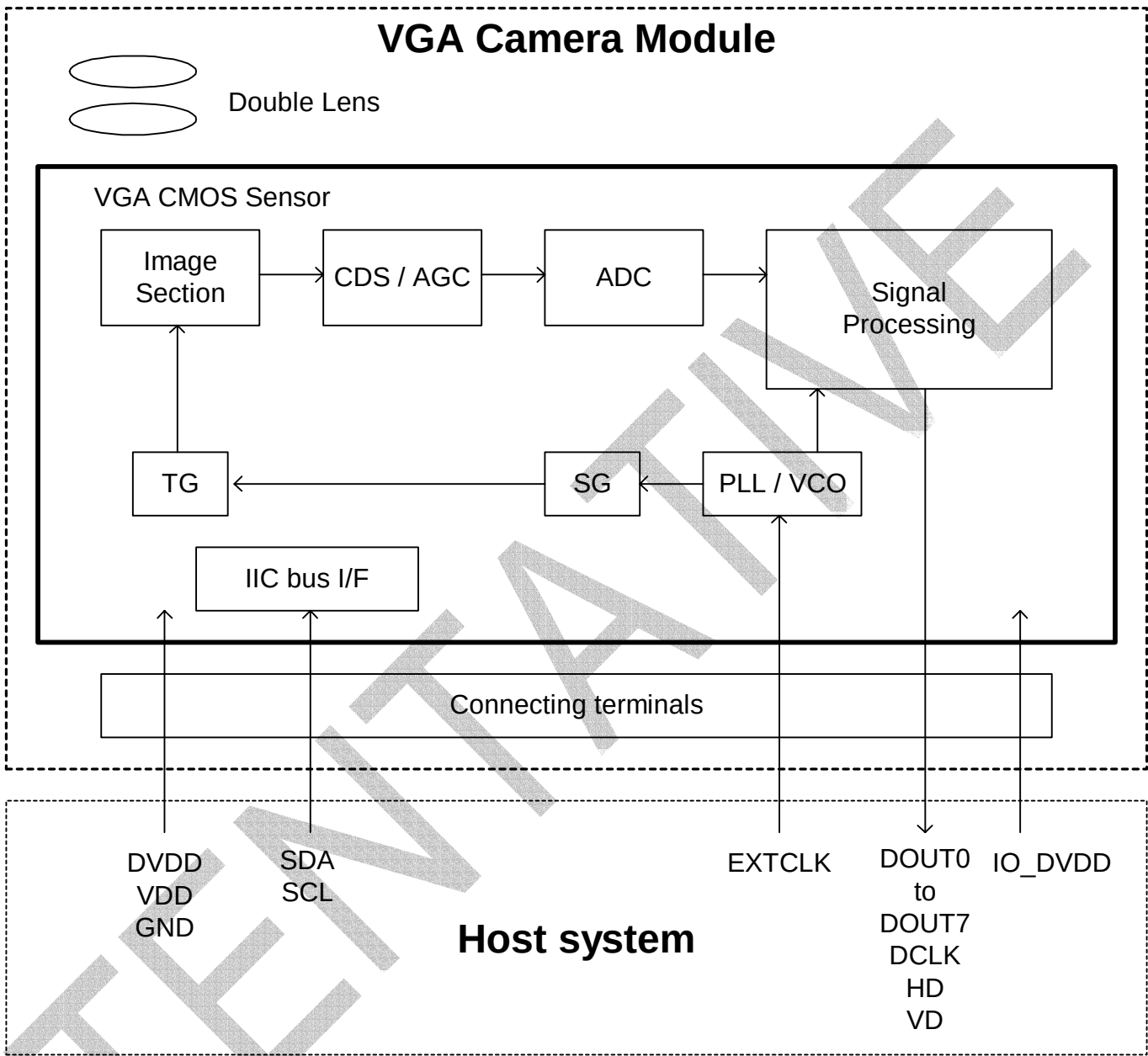
- Built-in PLL circuit and timing controller
- Long exposure mode until 15 times period of normal operation are available
- Digital outputs are selectable
YUV=4:2:2 or RGB=5:6:5 (8bit parallel output)
- Many kinds of picture size are available
VGA, QVGA, QQVGA, CIF, QCIF, subQCIF (Sub-sampling , Windowing)
- Some kinds of internal parameter can be read
Sensor gain setting, Electrical shutter exposure period, ALC and AWB reference value
Built-in auto electrical shutter control (AES), auto gain control (AGC) and auto white balance (AWB) circuit
Flickerless auto luminance control (ALC=AES+AGC) and auto flicker detection circuit for AC 50Hz / 60Hz fluorescent light
- Built-in automatically blemish correction
- Vertical and Horizontal reverse are available

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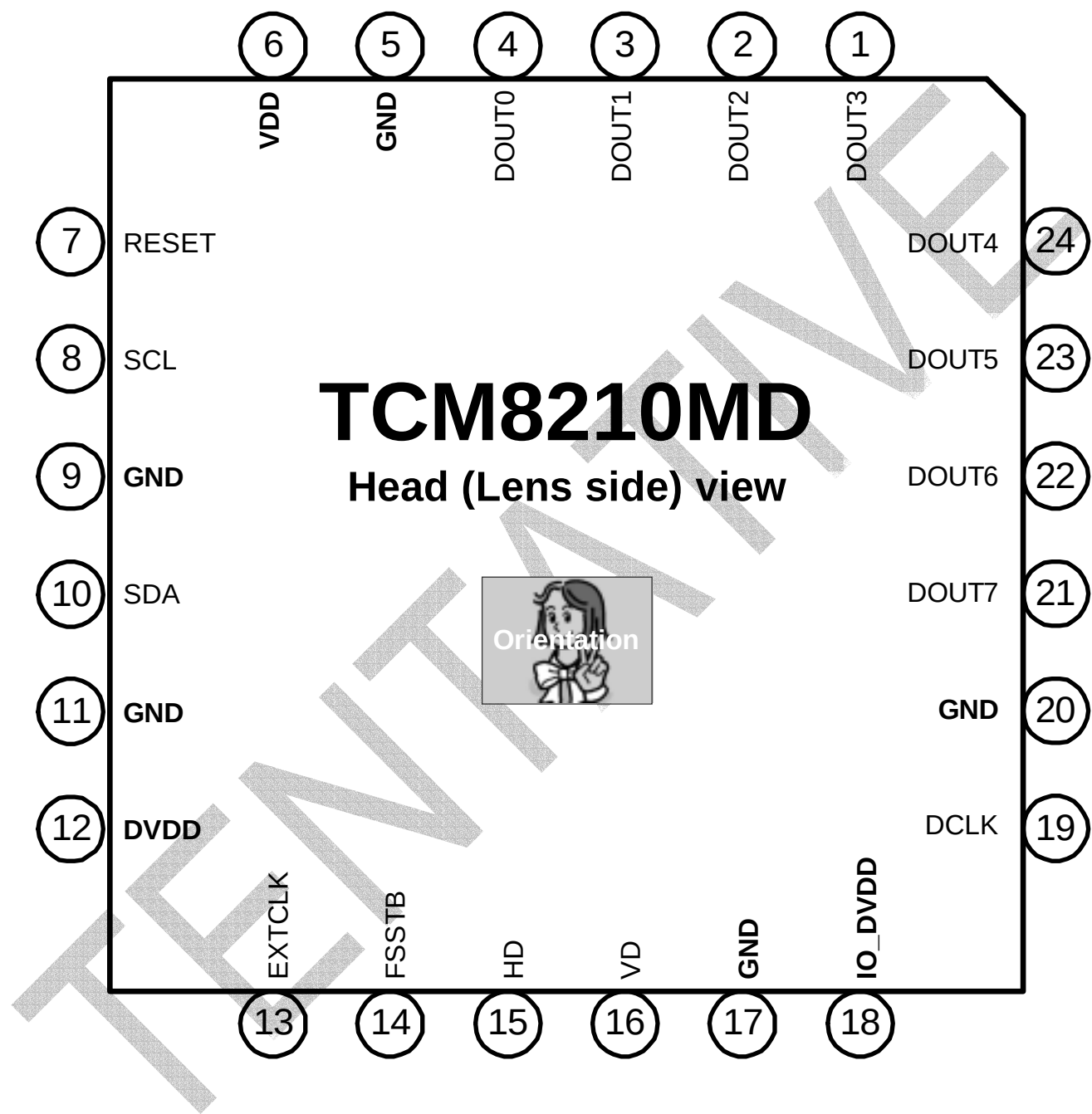
UPDATE INFORMATION

Ver. 2.07	Jun-10, 2003
Ver. 2.06	Jun-09, 2003
Ver. 2.05	May-21, 2003
Ver. 2.04	May-20, 2003
Ver. 2.03	May-16, 2003
Ver. 2.02	Apr-04, 2003
Ver. 2.01	Mar-12, 2003
Ver. 2.0	Feb-16, 2003
Ver. 1.0	Dec-24, 2002

BLOCK DIAGRAM



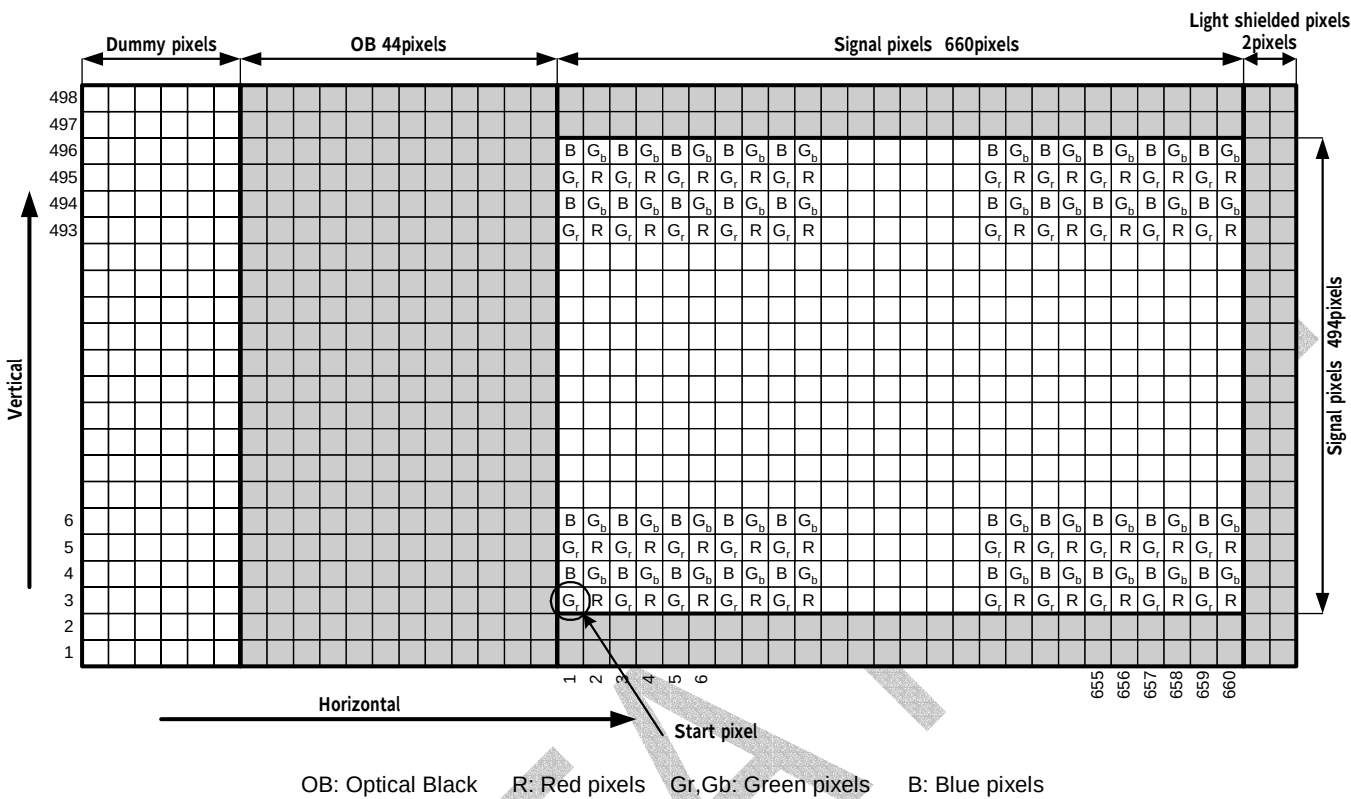
PIN LAYOUT



PIN FUNCTIONS

NO.	SYMBOL	I/O	FUNCTION
1	DOUT3	DO	Data Output
2	DOUT2	DO	Data Output
3	DOUT1	DO	Data Output
4	DOUT0	DO	Data Output (LSB)
5	GND	-	GND
6	VDD	-	VDD for the Sensor and PLL(2.8+/-0.2V)
7	RESET	DI	RESET terminal
8	SCL	-	Clock for IIC bus Command
9	GND	-	GND
10	SDA	-	Data for IIC bus Command
11	GND	-	GND
12	DVDD	-	VDD for the Digital Circuit (2.8+/-0.2V)
13	EXTCLK	DI	External Clock Input
14	FSSTB	DO	Strobe Pulse for Flash
15	HD	DO	Horizontal Synchronization Pulse Output
16	VD	DO	Vertical Synchronization Pulse Output
17	GND	-	GND
18	IO_DVDD	-	VDD for I/O (from 2.3V to 3.0V Typ: 2.8V)
19	DCLK	DO	Clock for Output Data
20	GND	-	GND
21	DOUT7	DO	Data Output (MSB)
22	DOUT6	DO	Data Output
23	DOUT5	DO	Data Output
24	DOUT4	DO	Data Output

PIXEL ARRANGEMENT



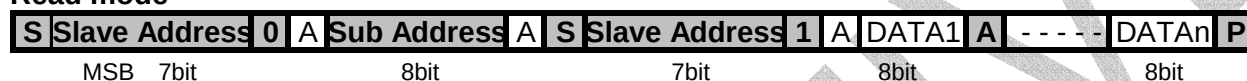
CONTROL I/F

TCM8210MD(A) control interface configuration is based on fast mode IIC bus.
Register setting can be changed via IIC bus.

Write mode



Read mode



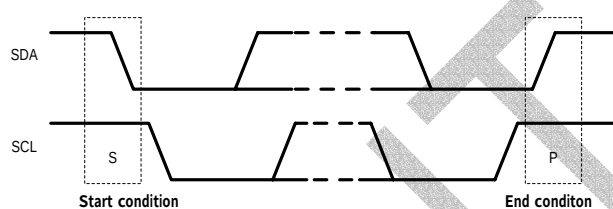
: Host Command



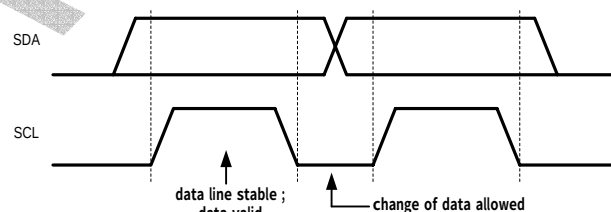
: TCM8210MD (A)

S : Start condition , P : End condition , A : Acknowledge

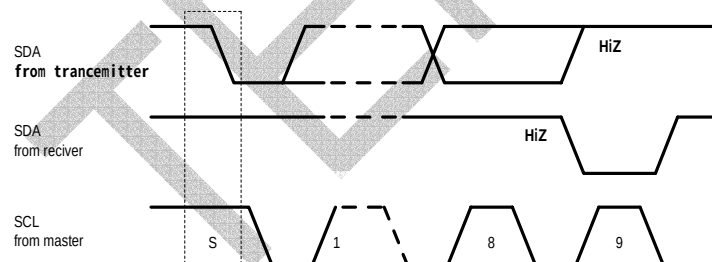
Start condition , End condition



Bit Transfer



Acknowledge



Slave address

A6	A5	A4	A3	A2	A1	A0	R/W
0	1	1	1	1	0	0	1/0

* TCM8210MD(A) use 7bit Slave address

Purchase of TOSHIBA IIC components conveys a license under the Philips IIC Patent Rights to use these components in an IIC system, provided that the system conforms to the IIC Standard Specification as defined by Philips.

INTERNAL REGISTER

ADDRESS	fast							last	Default (ROM Data)											
HEX	BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)	B7	B6	B5	B4	B3	B2	B1	B0	HEX			
00									0	0	0	0	0	0	0	0	00			
01	VNUM[3:0]								0	0	1	1	0	0	0	0	30			
02	FPS 0:30fps 1:15fps	ACF 0:50Hz 1:60Hz	ECK[3:0] 0h: PLLoff 2h: 13MHz 3h: 6.5MHz 4h: 19.2MHz 5h: 9.6MHz 6h: 16.8MHz 7h: 8.4MHz 8h: 19.44MHz 9h: 9.72MHz				DCLKP 0: normal 1: reverse	ACFDET 0: AUTO 1: MANUAL	1	1	0	0	0	0	0	0	C0			
03	DOUTSW 0:ON 1:OFF	DATAHZ 0:OUT 1:Hi-Z	PICSIZ[3:0] 0h:VGA 1h:QVGA(f) 2h:QVGA(z) 3h:QQVGA(f) 4h:QQVGA(z) 5h:CIF(f) 6h:QCIF(f) 7h:QCIF(z) 8h:subQCIF(f) 9h:subQCIF(z)				PICFMT 0:YUV422 1:RGB565	CM 0:COLOR 1:B/W	1	0	0	0	0	0	0	0	80			
04	V_INV 0:normal 1:invert	H_INV 0:normal 1:invert	ESRLSW[1:0] 0h: Short 1h: Long 2h & 3h: Extra long		V_LENGTH[3:0]						0	0	0	0	1	1	1	0F		
05	ALCSW 0:AUTO 1:MANUAL	ESRLIM[1:0]		ESRSPD[12:8]							0	0	0	0	0	1	0	02		
06	ESRSPD[7:0]											0	0	0	0	1	1	0	1	0D
07	AG[7:0]											1	1	0	0	0	0	0	0	C0
08			ALCMODE[1:0] 0h: Center Weight 1h: Average 2h: Center Only 3h: Backlight		ALCH[3:0]						0	0	1	1	1	0	0	0	38	
09	ALCL[7:0]											0	1	0	0	0	0	0	0	40
0A	AWBSW 0:AUTO 1:MANUAL											0	0	0	0	0	0	0	0	00
0B	MRG[7:0]											0	1	0	0	0	0	0	0	40
0C	MBG[7:0]											0	1	0	0	0	0	0	0	40
0D	GAMSW 0:ON 1:OFF											0	0	0	0	0	0	0	0	00
0E	HDTG[7:0]											0	0	1	0	1	1	1	1	2F
0F	VDTG[7:0]											0	0	0	0	0	1	0	0	04
10	HDTCORE[3:0]				VDTCORE[3:0]							0	0	1	0	0	0	1	0	22
11	CONT[7:0]											1	0	0	1	1	0	1	0	9A
12	BRIGHT[7:0]											0	0	0	0	1	1	0	0	0C
13		VHUE[6:0]									0	0	0	0	1	0	1	0	0A	
14		UHUE[6:0]									0	0	0	0	1	0	0	0	08	
15			VGAIN[5:0]							0	0	1	1	1	0	0	0	0	38	
16			UGAIN[5:0]							0	0	1	1	1	0	0	0	0	38	
17					UVCORE[3:0]							0	0	0	0	0	0	0	1	01
18			SATU[5:0]							0	0	1	0	0	1	1	1	1	27	
19	MHMODE 0: 1:	MHLPFSEL 0: 1:	YMODE[1:0]				MIXHG[2:0]					0	0	0	0	0	1	0	0	04
1A			LENS[5:0]							0	0	1	0	0	0	0	0	0	0	20
1B	AGLIM[2:0]			LENSRPOL 0:Gain up 1:Gain down		LENSRGAIN[3:0]						0	1	0	0	0	1	1	0	46
1C	ES100S[7:0]											1	0	0	1	1	1	1	0	9E
1D	ES120S[7:0]											1	0	0	0	0	0	1	1	83
1E	D_MASK[1:0]		CODESW 0:OFF 1:OUT	CODESEL 0: original 1: ITU656	HSYNCSSEL 0: normal 1: h_blanking	TESPIC 0:Not out 1:Out	PICSEL[1:0] 0h: Colorbar 1h: Ramp1 2h: Ramp2 3h: Unsupported					0	1	1	0	1	0	0	0	68
1F	SLEEPW 0:ACTIVE 1:SLEEP	SRST 0:OFF 1:reset									0	0	0	0	0	0	0	0	0	00

ADDRESS	fast							last	Default (ROM Data)								
HEX	BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)	B7	B6	B5	B4	B3	B2	B1	B0	HEX
20	HNUM[7:0]								0	0	0	0	0	0	0	0	00
21	HPPH[7:0]								0	0	0	0	0	0	0	1	01
22	HPPH[8]	VRRPH[6:0]							0	0	1	0	0	1	1	0	26
23	HDSPPH[7:0]								0	1	0	0	0	0	0	0	40
24	HDSPPH[8]	VDSPPH[6:0]							0	0	1	0	0	1	1	1	27
25	HAPRPH[7:0]								0	1	0	1	1	1	1	1	5F
26	HAPRPH[8]								0	0	0	0	0	0	0	0	00
27	HOUTPH[7:0]								0	0	0	1	0	1	1	0	16
28	HOUTPH[8]	VOUTPH[6:0]							0	0	1	0	0	0	1	1	23
29	FSSTBSW 0 : NOT OUT 1 : OUT	FSSTBPOL 0 : normal 1 : invert				FSSTBPH[3:0]			0	0	0	0	1	0	0	0	08
2A								FSSTBW[3:0]	0	0	0	0	1	0	0	0	08
2B								SCMD[19:16]	0	0	0	0	0	0	0	0	00
2C	SCMD[15:8]								0	0	0	0	0	0	0	0	00
2D	SCMD[7:0]								0	0	0	0	0	0	0	0	00
2E	TCSB1L 0: 1:	TCPEROSW [2:0]			TCSBIN 0: 1:	TCRAM 0: 1:	TROM[1:0]		0	0	0	0	0	0	0	0	00
2F	TCRAMS 0: 1:	TSPCHK 0: 1:	TCPERAGC	TALCRST	TWBS	TWBG	TACDET[1:0]		0	0	0	0	0	0	0	0	00
30	PCMODE 0: normal 1: DAFC	TGAMROM 0: 1:			TCSB[3:0]				0	0	0	0	0	0	0	0	00
31	TALCDISP 0: 1:	TALCOSW[2:0]			PBDISP[1:0]		TDISP[1:0]		0	0	0	0	0	0	0	0	00
32	ESROUT[14:8]								0	0	0	0	0	0	0	0	00
33	ESROUT[7:0]								0	0	0	0	0	0	0	0	00
34	AGOUT[7:0]								0	0	0	0	0	0	0	0	00
35						DGOUT[5:0]			0	0	0	0	0	0	0	0	00
36	ALCDATA[7:0]								0	0	0	0	0	0	0	0	00
37	AWBRYDA[7:0]								0	0	0	0	0	0	0	0	00
38	AWBBYDA[7:0]								0	0	0	0	0	0	0	0	00
39	AGSLOW1[1:0]		FLLSMODE[1:0]		FLLSLIM[3:0]			1	0	0	0	1	1	0	0	0	8C
3A	DETSEL[3:0]					ACDETNC[3:0]			1	1	0	0	1	1	1	1	CF
3B	AGSLOW2[1:0]		DG[5:0]						1	0	0	0	0	0	0	0	80
3C	REJHLEV[7:0]								0	0	0	0	0	0	0	0	00
3D	ALCLOCK 0: 1:	FPSLNKSW 0: 1:	ALCSPD[1:0]		ALCSTEP[1:0]		REJH[1:0]		0	0	0	1	0	1	1	1	17
3E	SHESRSW 0:Disable 1:Enable	ESLIMSEL 0: 1:	SHESRSPD[1:0]		ELSTEP[1:0]		ELSTART[1:0]		1	0	0	0	0	1	0	1	85
3F	AGMIN[7:0]								1	1	0	0	0	0	0	0	C0

ADDRESS	fast								last	Default (ROM Data)								
HEX	BIT7(MSB)	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)	B7	B6	B5	B4	B3	B2	B1	B0	HEX	
40	LI1POL 0: 1:	CS1POL 0: 1:	LI3POL 0: 1:	CS3POL 0: 1:					DINCKSW 0: 1:	0	0	0	0	0	0	0	00	
41	JAMP 0: 1:	JAMG[6:0]								0	0	0	0	0	0	0	00	
42			PREGRG[5:0]							0	0	0	0	0	0	0	00	
43			PREGBG[5:0]							0	0	0	0	0	0	0	00	
44			PRERG[5:0]							0	0	0	1	0	1	0	15	
45			PREBG[5:0]							0	0	0	1	1	1	1	1F	
46										0	0	0	0	0	0	0	00	
47			MSKBR[6:0]							0	1	0	0	0	1	0	44	
48			MSKGR[6:0]							0	1	0	0	0	1	0	44	
49			MSKRB[6:0]							0	0	1	0	0	0	0	20	
4A			MSKGB[6:0]							0	1	0	0	0	1	0	45	
4B			MSKRG[6:0]							0	1	1	0	0	1	1	66	
4C			MSKBG[6:0]							0	0	1	1	0	0	0	30	
4D	HDTCW 0: 1:	VDTCW 0: 1:	DTCYLV[5:0]						1	1	1	0	0	0	0	E0		
4E	HDTPW 0: 1:	VDTPW 0: 1:	DTCGAIN[5:0]						0	0	1	0	0	0	0	20		
4F	LI12POL 0: 1:	CS12POL 0: 1:		DTLLIMSW 0: 1:	DTLYLIM [3:0]					0	0	0	0	1	0	0	09	
50	YLCUTLSK 0: 1:		YLCUTL[5:0]						0	0	0	0	0	1	1	1	07	
51	YLCUTHMSK 0: 1:		YLCUTH[5:0]						0	0	1	0	1	1	1	1	2F	
52			UVSKNC[6:0]						0	0	0	0	0	0	1	0	02	
53			UVLJ[6:0]						0	0	0	0	0	0	0	0	00	
54	WBGMIN[7:0]									0	0	1	0	1	0	1	1	2B
55	WBGMAX[7:0]									0	1	1	0	0	0	0	0	60
56	AWBCSPOLE 0: 1:	WBDIVCLP 0: 1:	WBNOLJ[1:0]		WBNOLJSC 0: 1:	WB2IM 0: 1:	WBSPDUP[1:0]			0	1	0	0	0	0	0	40	
57										0	0	0	0	0	1	1	0	06
58			ALLAREA 0: 1:	WBLOCK 0: 1:	WB2SP [3:0]					0	0	1	0	0	0	1	0	22
59			KIZUSW 0:OFF 1:ON	PBRDSW				ABCSW[1:0]		0	0	1	0	0	0	1	1	23
5A	PBDLV[7:0]									0	0	0	0	1	0	0	0	08
5B	PBC1LV[7:0]									0	0	0	0	0	1	0	0	04
5C	PBC2LV[7:0]									0	0	0	0	1	0	0	0	08
5D	PBC3LV[7:0]									0	0	0	0	1	0	0	0	08
5E	PBC4LV[7:0]									0	0	0	0	1	0	0	0	08
5F	PBC5LV[7:0]									0	0	0	0	1	0	0	0	08

OUTLINE OF INTERNAL REGISTER

- * Frame rate setting (30fps, 15fps)
- * Picture size setting of digital output (VGA, QVGA, CIF, QCIF, subQCIF)
- * Selection of digital data output format (8bit RGB565, YUV422)
- * Sync. code setting (ON/OFF, 2 mode)
- * Color signal adjustment (Masking, color axis correction, saturation, etc.)
- * Luminance signal adjustment (Contrast, Brightness, Gamma, H,V edge enhancement)
- * ALC ON/OFF
- * ALC mode setting (area selection, speed selection, flicker reduction mode setting)
- * AWB ON/OFF
- * Some kinds of correction setting (Lens shading correction etc.)

8bit parallel image data

	YUV mode				RGB mode	
	first	second	third	fourth	first	second
D0	U0 (n)	Y0 (n)	V0 (n)	Y0 (n+1)	B0	G3
D1	U1 (n)	Y1 (n)	V1 (n)	Y1 (n+1)	B1	G4
D2	U2 (n)	Y2 (n)	V2 (n)	Y2 (n+1)	B2	G5
D3	U3 (n)	Y3 (n)	V3 (n)	Y3 (n+1)	B3	R0
D4	U4 (n)	Y4 (n)	V4 (n)	Y4 (n+1)	B4	R1
D5	U5 (n)	Y5 (n)	V5 (n)	Y5 (n+1)	G0	R2
D6	U6 (n)	Y6 (n)	V6 (n)	Y6 (n+1)	G1	R3
D7	U7 (n)	Y7 (n)	V7 (n)	Y7 (n+1)	G2	R4

Image size format

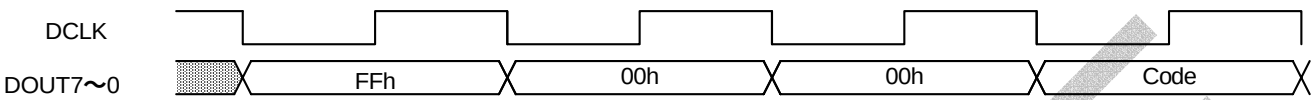
Image size	Display mode	Pixels per H	Effective H lines	Start point (H, V)	End point (H, V)	DCLK mode	Operation mode	Resizing method
VGA	Full	640	480	(1, 1)	(640, 480)	1	Normal	-
QVGA	Full	320	240	(1, 1)	(639, 479)	1/2	Low power	Sub-sampling from VGA
	Zoom x 2			(161, 121)	(480, 360)	1	Normal	Windowing from VGA
QQVGA	Full	160	120	(1, 1)	(637, 477)	1/2	Low power	Sub-sampling from QVGA(f)
	Zoom x 2			(161, 121)	(479, 359)			Sub-sampling from VGA
CIF	Full	352	288	(21, 1)	(608, 478)	1	Normal	3/5 filtering from VGA
QCIF	Full	176	144	(21, 1)	(608, 478)	1/2	Low power	3/5 filtering from QVGA(f)
	Zoom x 2			(173, 121)	(466, 360)	1	Normal	Windowing from CIF
subQCIF	Full	128	96	(1, 1)	(636, 476)	1/2	Low Power	4/5 filtering from QVGA(f)
	Zoom x 2			(161, 121)	(479, 359)			1st: 3/5 filtering from QVGA(f) 2nd: Sub-sampling from "1st"

QVGA(f) means QVGA full.

QQVGA(f) means QVGA full.

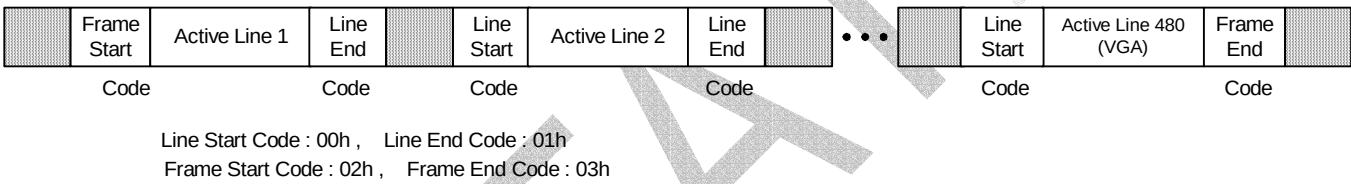
SYNCHRONIZATION CODE

Code output format

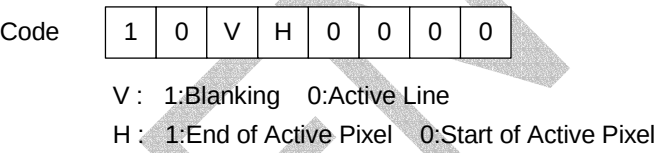


Code output mode

Mode1 (These codes only exists in active lines)



Mode2 (These codes exists in every lines)

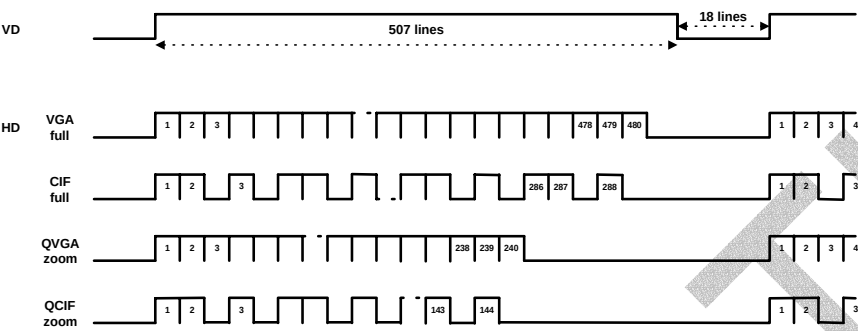


DATA OUTPUT TIMING CHART

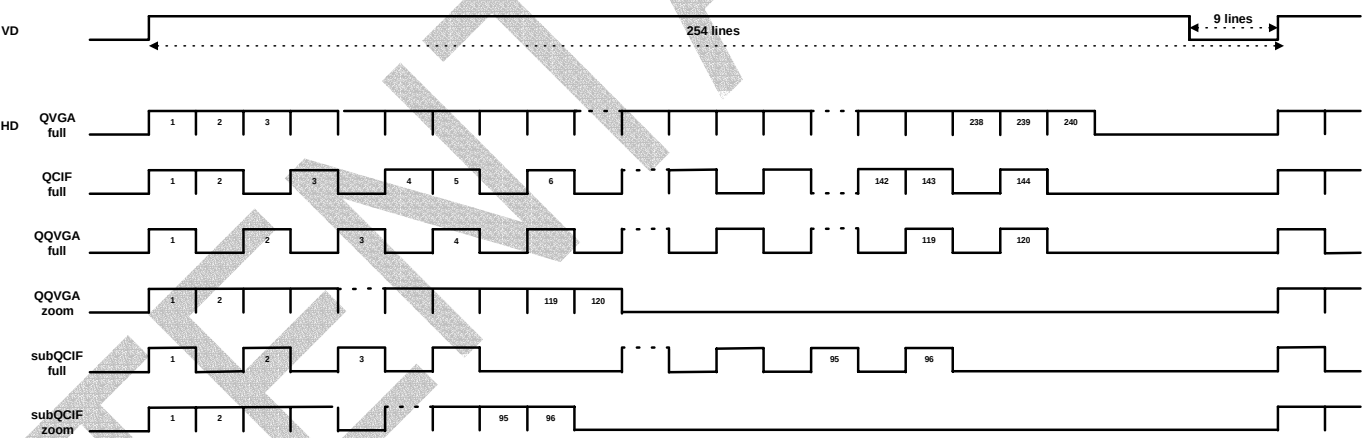
Pixel Size mode

Vertical

Normal operation mode
(VGA, CIF(full), QVGA(zoom), QCIF(zoom))



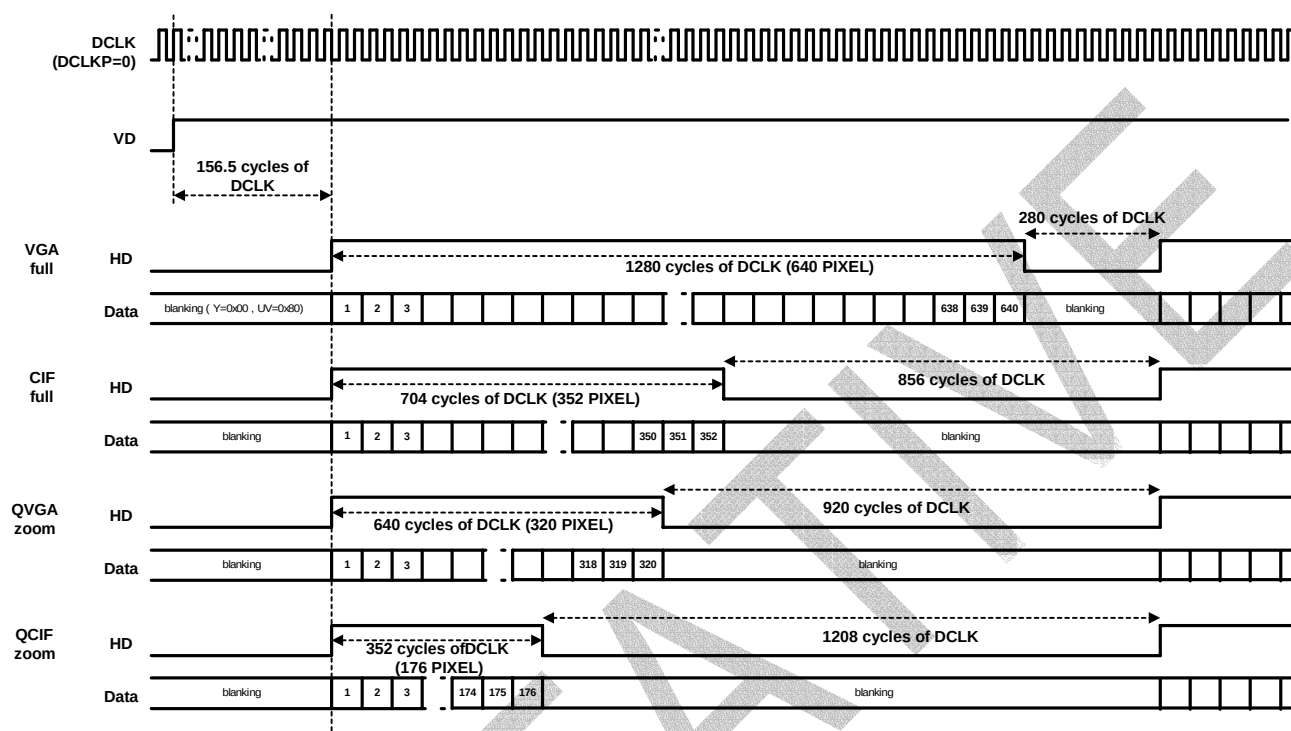
Low power operation mode
(QVGA(full), QQVGA(full), QQVGA(zoom), QCIF(full), subQCIF(full), subQCIF(zoom))



Horizontal

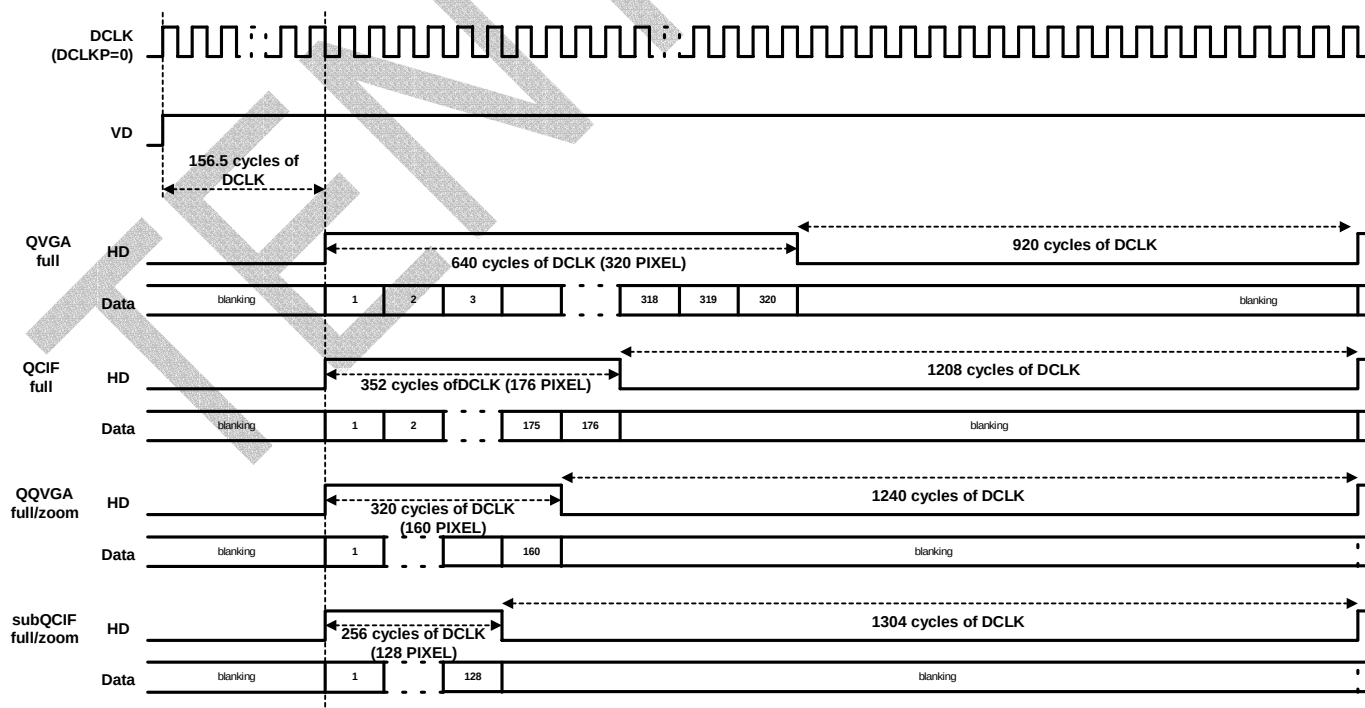
Normal operation mode

(VGA, CIF (full), QVGA (zoom), QCIF (zoom))



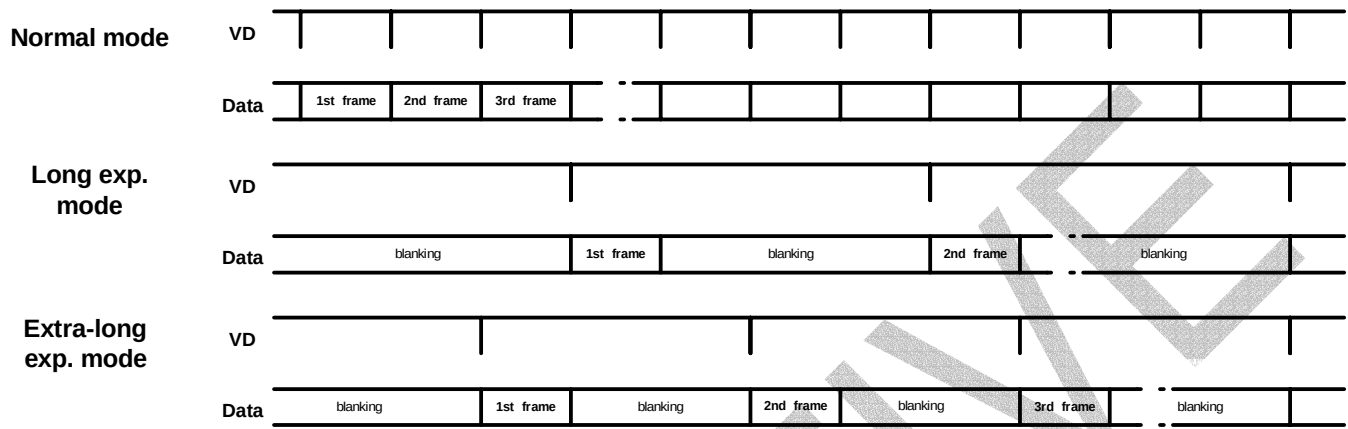
Low power operation mode

(QVGA(full), QQVGA(full), QQVGA(zoom), QCIF(full), subQCIF(full), subQCIF(zoom))

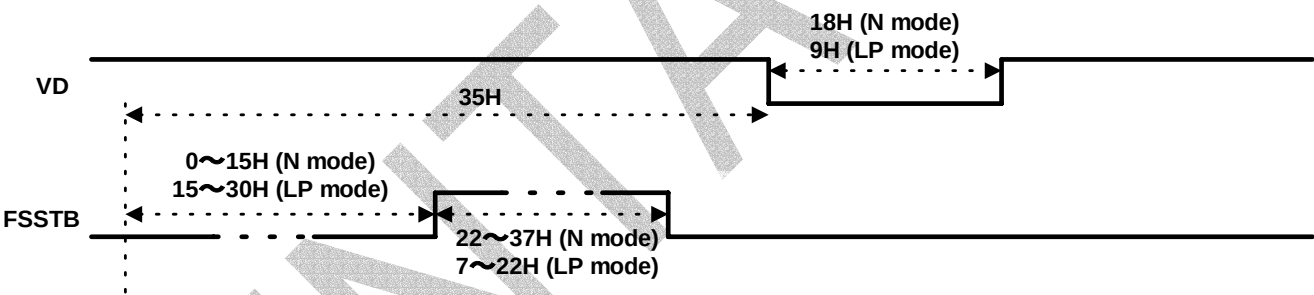


Exposure mode

Vertical



Flash Trigger Pulse



“N mode” means “Normal operation mode”
“LP mode” means “Low power operation mode”

MAXIMUM RATING

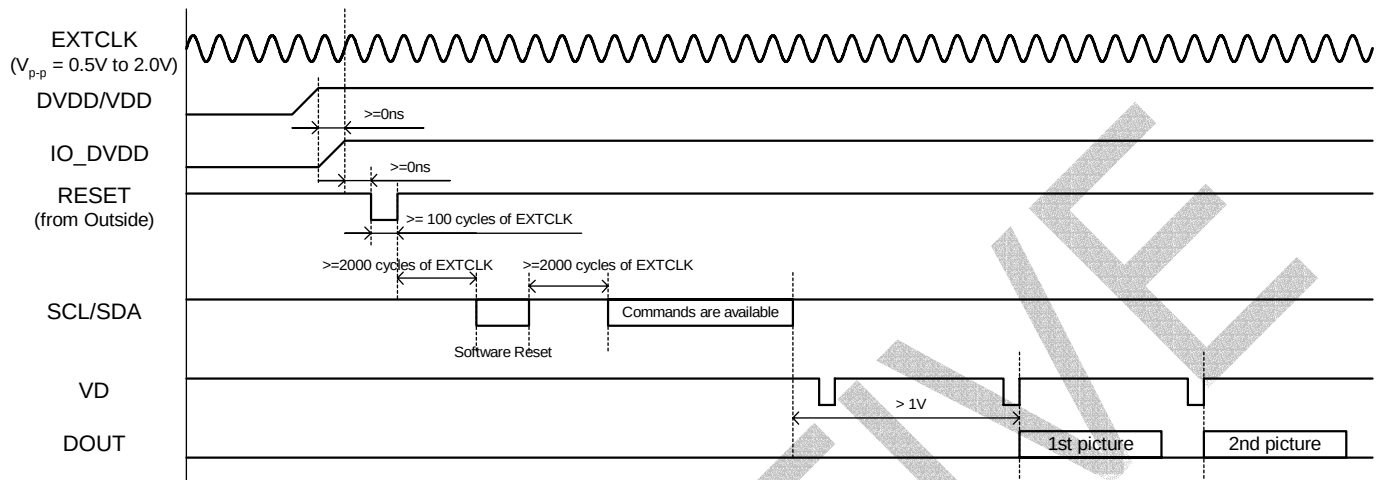
	RATING	UNITS
Power supply voltage	-0.3 to 3.6	V
Storage temperature	-30 to 85	Degree C

RECOMMENDED OPERATING CONDITION

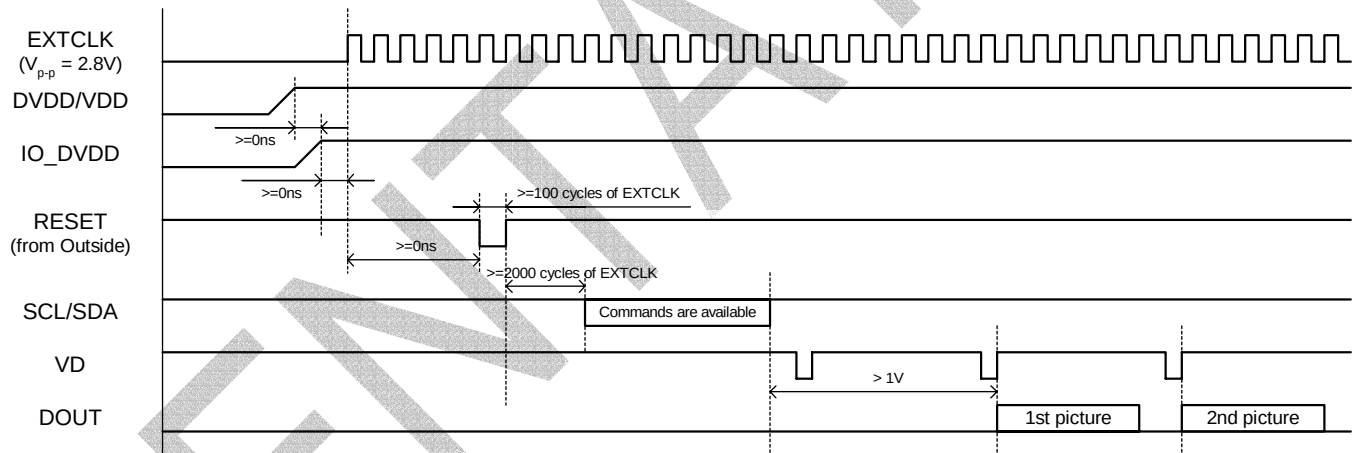
	MIN	TYP	MAX	UNITS
Power supply voltage (VDD)	2.6	2.8	3.0	V
Operational temperature	-20	-	60	Degree C

POWER ON SEQUENCE

1. Sine wave into EXTCLK



2. Rectangular shape into EXTCLK



ELECTRICAL CHARACTERISTICS

DC Characteristic (Ta=25 degree C, VDD=2.8V)

1. POWER

ITEM	CONDITION	MIN	TYP	MAX	UNITS
POWER	VGA(15fps) (Normal operation mode)	-	35	50	mA
	QVGA(Full) (15fps) (Low power mode)	-	25	TBD	mA
	VDD peak	-	-	100	mA
	Sleep mode	-	-	10	uA

2. EXTCLK

ITEM	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Sine wave	$V_{pp,EXTCLK}$	0.5	-	2.0	V_{p-p}	
Rectangular shape	LOW level input voltage	$V_{IL,EXTCLK}$	-0.3	-	$VDD*0.2$	V
	HIGH level input voltage	$V_{IH,EXTCLK}$	$VDD*0.8$	VDD	3.0	V
	DUTY	-	45/55	50/50	55/45	% *1

1) Duty referred to 50% level of input EXTCLK

3. SCL and SDA

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTES
SCL	LOW level input voltage	$V_{IL,SCL}$	0.0	-	0.4	V
	HIGH level input voltage	$V_{IH,SCL}$	$VDD*0.7$	VDD	3.6	V
SDA	LOW level input voltage	$V_{IL,SDA}$	0.0	-	0.4	V
	HIGH level input voltage	$V_{IH,SDA}$	$VDD*0.7$	VDD	3.6	V
	LOW level output voltage (IOL=4mA)	$V_{OL,SDA}$	0.0	-	0.4	V

4. DOUT0 to DOUT7, DCLK, HD and VD

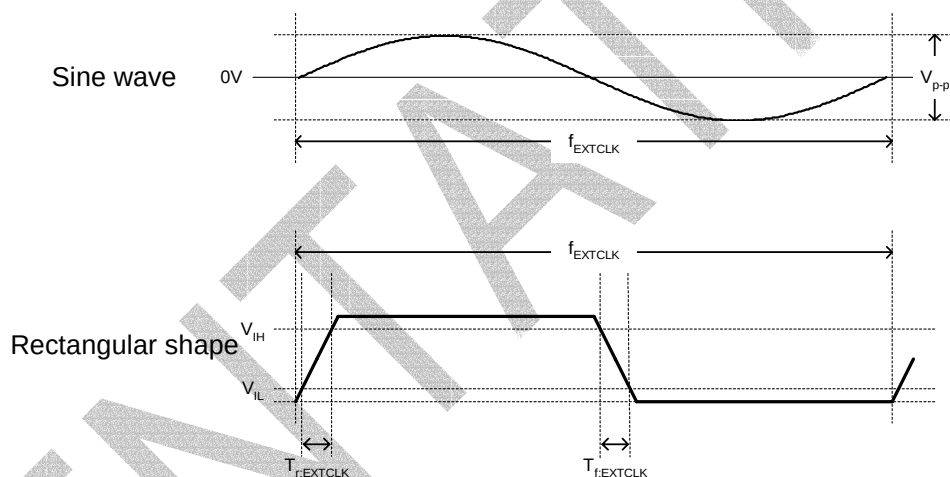
ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTES
DOUT0 to DOUT7, DCLK, HD and VD	HIGH level output voltage (IOH=-2mA)	$V_{OH,DATA}$	2.4	VDD	-	V
	LOW level output voltage (IOL=2mA)	$V_{OL,DATA}$	0.0	-	0.4	V

AC Characteristic ($T_a=25$ degree C, $V_{DD}=2.8V$)

1. EXTCLK

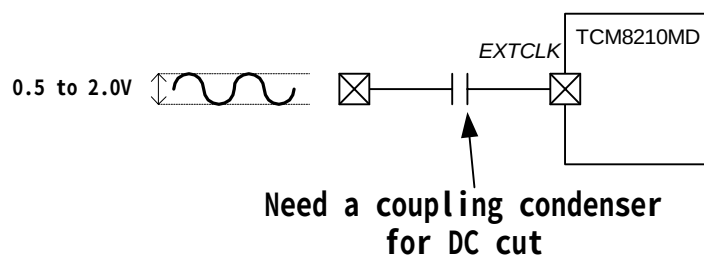
ITEM	CONDITION	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock frequency	PLL OFF(ECK=0)	f_{EXTCLK}	-	24.54	27.00	MHz	
	13MHz(ECK=2)		12.9	13.0	13.1	MHz	
	6.5MHz(ECK=3)		6.4	6.5	6.6	MHz	
	19.2MHz(ECK=4)		19.1	19.2	19.3	MHz	
	9.6MHz(ECK=5)		9.5	9.6	9.7	MHz	
	16.8MHz(ECK=6)		16.7	16.8	16.9	MHz	
	8.4MHz(ECK=7)		8.3	8.4	8.5	MHz	
	19.44MHz(ECK=8)		19.34	19.44	19.54	MHz	
	9.72MHz(ECK=9)		9.62	9.72	9.82	MHz	
Rise time		$t_{r,EXTCLK}$	-		5	ns	*1
Fall time		$t_{f,EXTCLK}$	-		5	ns	

1) All values referred to V_{IHmin} and V_{ILmax} levels

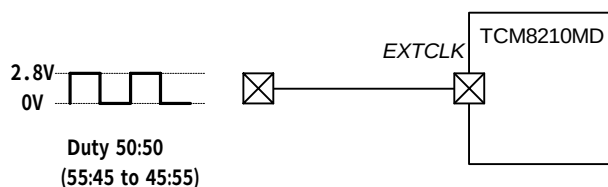


2. EXTCLK input circuit

Sine wave



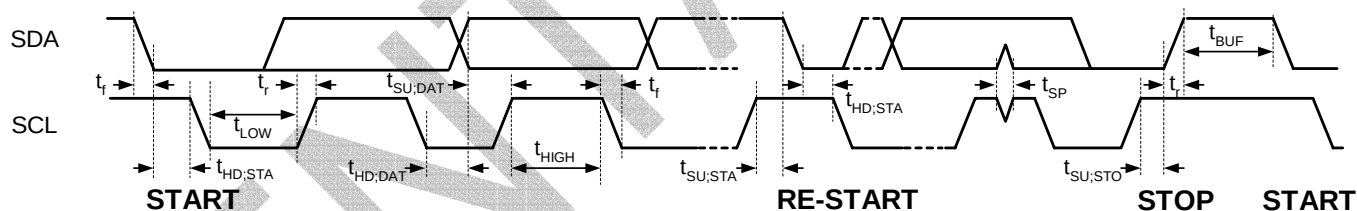
Rectangular shape



3. SCL and SDA

ITEM		SYMBOL	MIN	MAX	UNITS	NOTES
SCL	Clock frequency	f_{SCL}	0	400	KHz	*1
	Low period	$t_{LOW;SCL}$	1.3	-	us	
	High period	$t_{HIGH;SCL}$	0.6	-	us	
	Rise time	$t_{r;SCL}$	-	300	ns	
	Fall time	$t_{f;SCL}$	-	300	ns	
SDA	Rise time	$t_{r;SDA}$	-	300	ns	
	Fall time	$t_{f;SDA}$	-	300	ns	
Hold time(repeated) START condition After this period, the first clock pulse is		$t_{HD;STA}$	0.6	-	us	
Setup time for a repeated START condition		$t_{SU;STA}$	0.6	-	us	
Data hold time		$t_{HD;DAT}$	0	-	ns	
Data setup time		$t_{SU;DAT}$	100	-	ns	
Setup time for STOP condition		$t_{SU;STO}$	0.6	-	us	
Width of spike pulse	Normal	t_{SP1}	0	50	ns	
	Wake-up from sleep mode	t_{SP2}	0	20	ns	

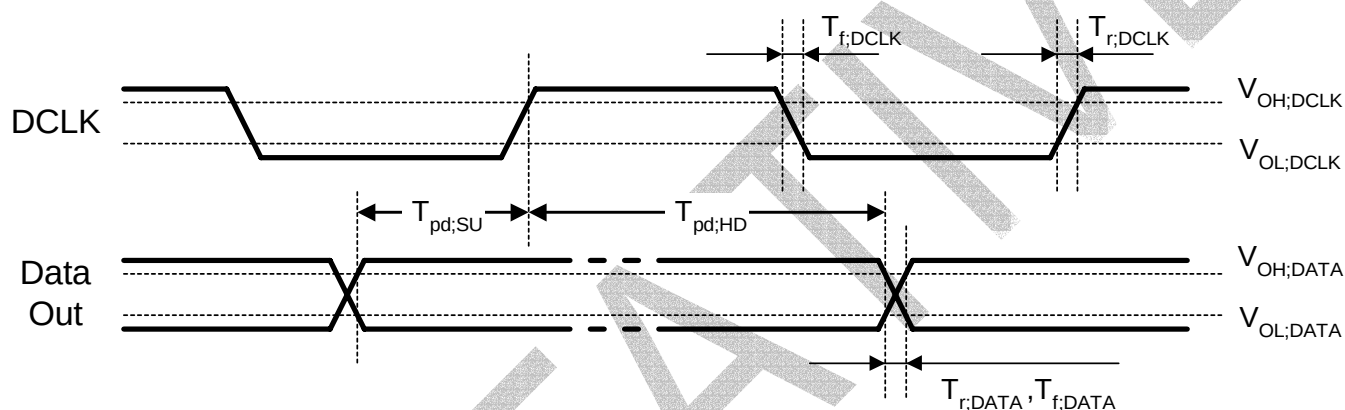
1) All values referred to V_{IHmin} and V_{ILmax} levels



4. DOUT0 to DOUT7, DCLK, HD and VD

ITEM	SYMBOL	MIN	MAX	UNITS	NOTES
DCLK	Rise time	$t_{r,DCLK}$	-	6	*1
	Fall time	$t_{f,DCLK}$	-	6	
DOUT0 to DOUT7, HD, and VD	Rise time	$t_{r,DATA}$	-	6	
	Fall time	$t_{f,DATA}$	-	6	
Setup time of data	$t_{pd,SU}$	10	-	ns	
Hold time of data	$t_{pd,HD}$	10	-	ns	

1) All values referred to V_{OHmin} and V_{OLmax} levels



CHARACTERISTICS OF LENS

ITEM	VALUE	UNITS
Optical format	1/4	inch
Field of view	Horizontal	46 degree
	Vertical	38 degree
	Diagonal	62 degree
F number	F2.8	-
TV distortion	-2	%
Relative illumination	44	%
Focusing area	20 to infinity	cm
Manual focusing	Not available	-
Structure	Double lens	-

[illegible]

Appendix 2: Socket drawing

