TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

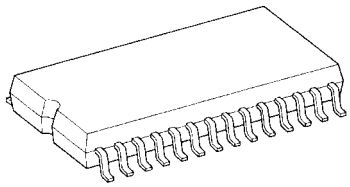
TC9237BF,TC9237BN

Σ-Δ Modulation System DA Converter with Built-In Digital Filter

TC9237BF, TC9237BN are a 2'nd order Σ-Δ modulation system 1 bit DA converter with a built-in 8 times over-sampling FIR type digital filter developed for digital audio equipment.

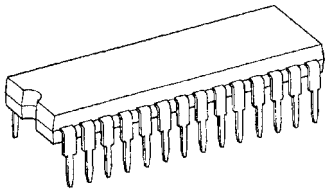
As the de-emphasis function has been incorporation, it is possible to configure the system for digital filtering through analogue output at a low price.

TC9237BF



SOP28-P-450-1.27

TC9237BN



SDIP28-P-400-1.78

Weight
SOP28-P-450-1.27: 0.8 g (typ.)
SDIP28-P-400-1.78: 2.2 g (typ.)

Features

- Built-in 8 times over-sampling FIR type digital filter.
- Over-sampling ratio (OSR) is 192 fs.
- Built-in digital de-emphasis filter.
- Simultaneous outputs to L-ch and R-ch.
- Compatible with fs = 32 k, 44.1 k, 48 kHz.
- Compatible with double speed operation.
- Characteristics of the digital filter and DA converter are as follows:

Digital Filter (fs = 44.1 kHz)

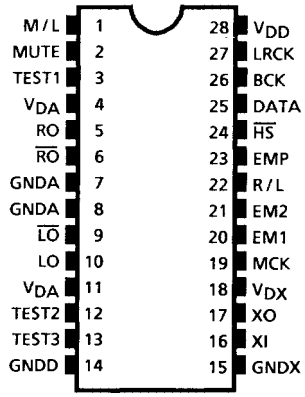
	DIGITAL FILTER	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP-BAND SUPPRESSION
Standard operation	8fs	±0.041dB	20k~23.5kHz	−55dB
Double speed operation	4fs	±0.026dB	20k~24.1kHz	−49dB

DA Converter

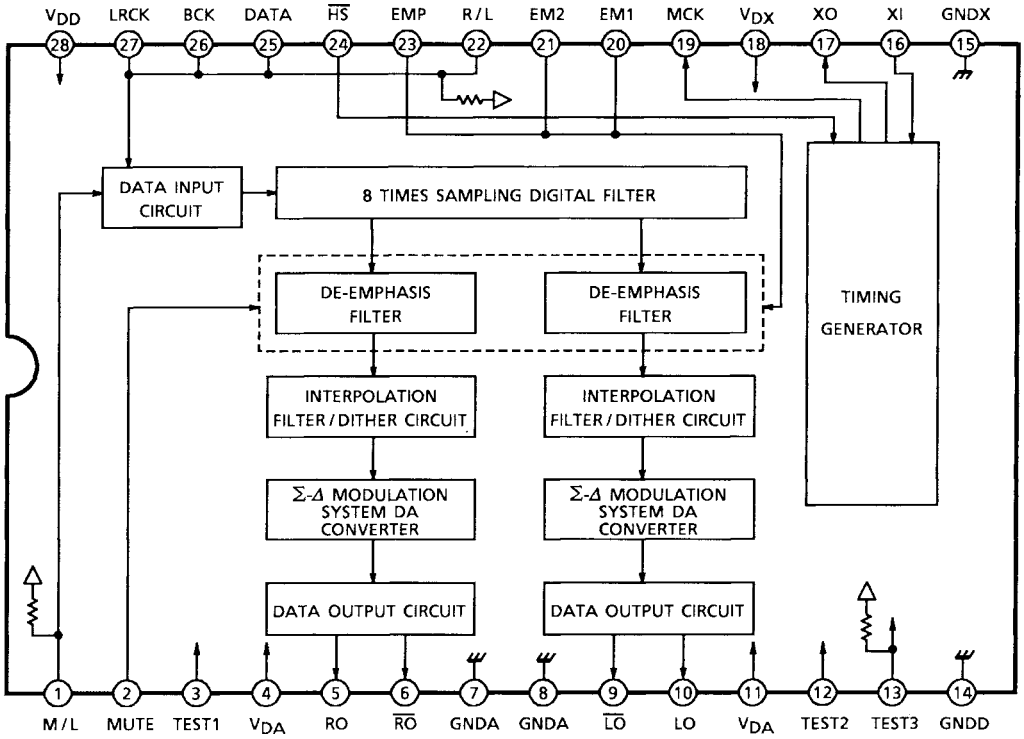
	OSR	NOISE DISTORTION	S/N RATIO
Standard operation	192fs	−87dB (Typ.)	98dB (Typ.)
Double speed operation	96fs	−87dB (Typ.)	98dB (Typ.)

- 2 kinds of package, 28-pin flat package and 28-pin DIP shrunk package.
- It is possible to construct a system in simple structure using the filter IC (TA2009P, TA2009F) dedicated to +5 V single power supply operation.

Pin Assignment (top view)



Block Diagram



Description of Pin Function

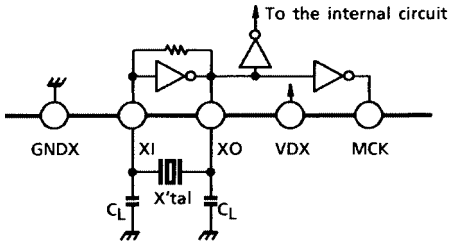
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Function&Operation</th><th>Remarks</th></tr>
<tr><td>1</td><td>M/L</td><td>I</td><td>Input data MSB First/LSB First selection pin.
MSB First at “H” and LSB First at “L”</td><td>With a pull-up resistor</td></tr>
<tr><td>2</td><td>MUTE</td><td>I</td><td>Soft mute control pin. Mute ON at “H”.</td><td></td></tr>
<tr><td>3</td><td>TEST1</td><td>I</td><td>TEST pin. Normally, use at “H”.</td><td></td></tr>
<tr><td>4</td><td>V_{DA}</td><td>—</td><td>Analog power supply pin.</td><td></td></tr>
<tr><td>5</td><td>RO</td><td>O</td><td>R channel data forward output pin.</td><td></td></tr>
<tr><td>6</td><td>$\overline{RO}$</td><td>O</td><td>R channel data reverse output pin.</td><td></td></tr>
<tr><td>7</td><td>GNDA</td><td>—</td><td>Analog ground pin.</td><td></td></tr>
<tr><td>8</td><td>GNDA</td><td>—</td><td>Analog ground pin.</td><td></td></tr>
<tr><td>9</td><td>$\overline{LO}$</td><td>O</td><td>L channel data reverse output pin.</td><td></td></tr>
<tr><td>10</td><td>LO</td><td>O</td><td>L channel data forward output pin.</td><td></td></tr>
<tr><td>11</td><td>V_{DA}</td><td>—</td><td>Analog power supply pin.</td><td></td></tr>
<tr><td>12</td><td>TEST2</td><td>I</td><td>TEST pin. Normally, use at “L”.</td><td></td></tr>
<tr><td>13</td><td>TEST3</td><td>I</td><td>TEST pin. Normally, use at “H” or open.</td><td>With a pull-up resistor</td></tr>
<tr><td>14</td><td>GNDD</td><td>—</td><td>Digital ground pin.</td><td></td></tr>
<tr><td>15</td><td>GNDX</td><td>—</td><td>Crystal oscillator ground pin.</td><td></td></tr>
<tr><td>16</td><td>XI</td><td>I</td><td rowspan="2">Crystal oscillator connecting pin.
Connecting a crystal oscillator, generates clock needed for the system. (384 fs)</td><td rowspan="2"></td></tr>
<tr><td>17</td><td>XO</td><td>O</td></tr>
<tr><td>18</td><td>V_{DX}</td><td>—</td><td>Crystal oscillator power supply pin.</td><td></td></tr>
<tr><td>19</td><td>MCK</td><td>O</td><td>Master clock output pin. (384 fs)</td><td></td></tr>
<tr><td>20</td><td>EM1</td><td>I</td><td rowspan="2">De-emphasis filter mode select pin.
<table>
<tr><td>EM1</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>EM2</td><td>L</td><td>H</td><td>H</td><td>L</td></tr>
<tr><td>MODE (fs selection)</td><td colspan="2">44.1 kHz</td><td>32 kHz</td><td>48 kHz</td></tr>
</table></td><td rowspan="2"></td></tr>
<tr><td>21</td><td>EM2</td><td>I</td></tr>
<tr><td>22</td><td>R/L</td><td>I</td><td>LRCK polarity switching pin.
<table>
<tr><td rowspan="2">R/L Input</td><td colspan="2">LRCK</td></tr>
<tr><td>L</td><td>H</td></tr>
<tr><td>L</td><td>R channel data</td><td>L channel data</td></tr>
<tr><td>H</td><td>L channel data</td><td>R channel data</td></tr>
</table></td><td>With a pull-up resistor</td></tr>
<tr><td>23</td><td>EMP</td><td>I</td><td>De-emphasis filter control pin.
ON at “H” and OFF at “L”.</td><td></td></tr>
<tr><td>24</td><td>$\overline{HS}$</td><td>I</td><td>Standard/double speed operation mode control pin.
Standard operation at “H” and double speed operation at “L”.</td><td></td></tr>
<tr><td>25</td><td>DATA</td><td>I</td><td>Data input pin.</td><td></td></tr>
<tr><td>26</td><td>BCK</td><td>I</td><td>Bit clock input pin.</td><td></td></tr>
<tr><td>27</td><td>LRCK</td><td>I</td><td>LR clock input pin.</td><td></td></tr>
<tr><td>28</td><td>V_{DD}</td><td>—</td><td>Logic power supply pin.</td><td></td></tr>
</table>

Description of Block Operation

1. Crystal Oscillation Circuit and Timing Generator

Clock required for internal operation can be generated when crystal and capacitors are connected as shown in Figure 1.

Further, this converter is also operable when system clock is input from the outside through XI pin (pin 16). However, a through consideration is required in this case because noise distortion and S/N ratio of the DA converter are largely affected by qualities of wave form such as jitter, rising and falling characteristics, etc. of system clock.



C_L = 10~33 pF

Use a crystal with a low CI value and quick response.

Figure 1 Configuration of Crystal Oscillation Circuit

The timing generator generates clock required for the digital filter, de-emphasis filter, interpolation filter and process timing signal.

2. Data Input Circuit

DATA and LRCK are taken in the shift register in the LSI at the rising edge of BCK. As shown in the falling timing example, it is therefore necessary to input DATA and LRCK in synchronism with the following edge of BCK. Further, because DATA has been so designed that 16 bits before the change point of LRCK are made effective data, it is necessary to data when BCK is 48 fs or 64 fs.

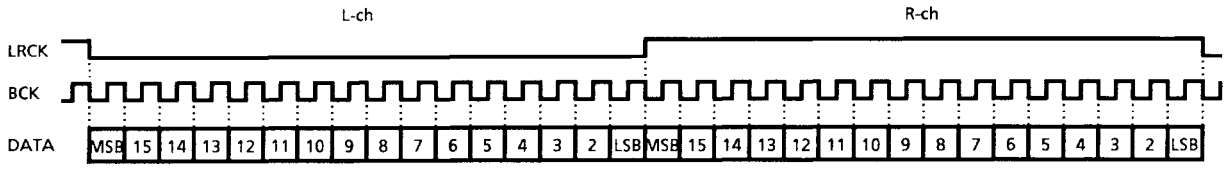


Figure 2 Example of Input Timing Chart (when R/L = M/L = "H")

Polarity of LRCK and input data modes are set using the R/L and M/L pin.

Table 1 Channel Data Correspondence

R/L Input	LRCK	
	L	H
L	R channel data	L channel data
H	L channel data	R channel data

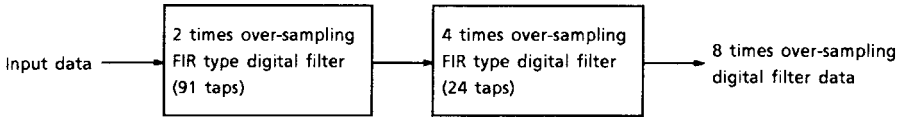
Table 2 Input Data Setting

M/L Input	Input Data (data)
L	LSB data first-in
H	MSB data first-in

3. Digital Filter

Foldover noise component outside the band is removed by the 8 times over-sampling FIR type digital filter. The construction and basic characteristic of the digital filter are changed by the standard and double speed operations. The contents of this change as shown below. (in the case of fs = 44.1 kHz/88.2 kHz (at the double speed operation).)

- Standard operation



- Double speed operation

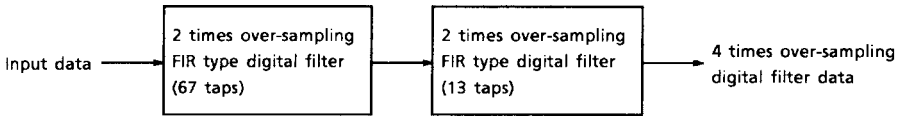


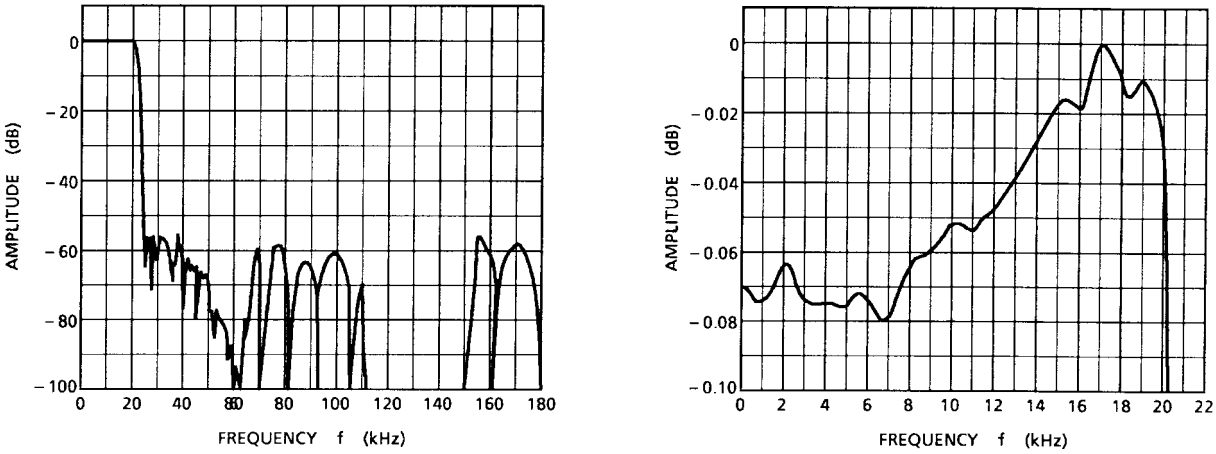
Figure 3 Construction of Digital Filter

Table 3 Basic Characteristics of Digital Filter

Setting Mode	Pass-Band Ripple	Transient Bandwidth	Stop-Band Suppression
Standard operation	±0.041dB	20.0 k~23.5 kHz	−55dB
Double speed operation	±0.026dB	20.0 k~24.1 kHz	−49dB

Frequency characteristics of the digital filter are as follows:

- Standard operation



- Double speed operation

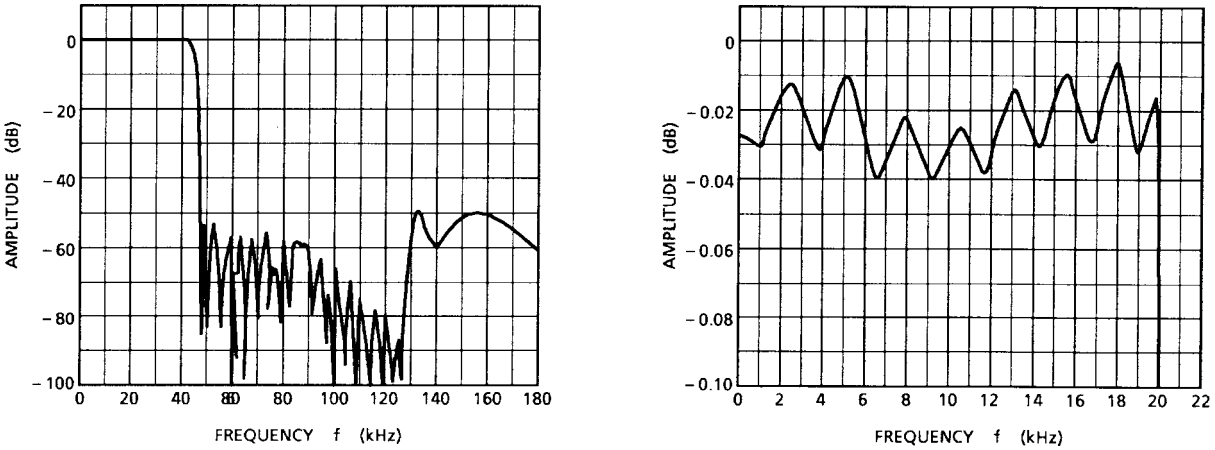


Figure 4 Digital Filter Frequency Characteristics (fs = 44.1 kHz)

4. De-Emphasis Filter

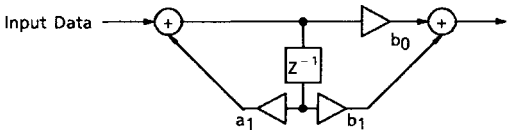
The TC9237BF, TC9237BN has a built-in IIR type digital de-emphasis circuit and is capable of copying with 3 kinds of frequency (32 kHz, 44.1 kHz, 48 kHz) by setting respective modes. These frequencies are set by 2 pins of EM1 and EM2 and the de-emphasis ON/OFF is switched by the EMP pin.

Table 4 fs Setting of De-Emphasis Filter

EM1	L	L	H	H
EM2	L	H	H	L
Mode (fs selection)	44.1 kHz		32 kHz	48 kHz

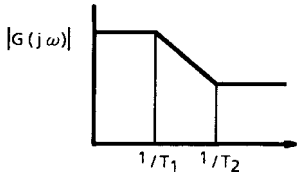
Digitization of the de-emphasis filter has eliminated the necessity for external parts such as resistor, capacitor, analogue switch, etc. Further, to reduce the characteristic error of the de-emphasis filter, coefficients have been adjusted.

The construction and characteristics of the de-emphasis filter are shown below.



Transfer function: $H(Z) = \dfrac{(b_0 + b_1 Z^{-1})}{(1 - a_1 Z^{-1})}$

Figure 5 Construction of IIR Type Digital De-Emphasis Filter



$T_1 = 50\ \mu s$, $T_2 = 15\ \mu s$

Figure 6 Filter Characteristic

Table 5 Typ. Example of De-Emphasis Frequency Characteristic

Standard Operation

(unit: dB)

Sampling Frequency fs	f = 3 kHz			f = 10 kHz			Maximum Error Value (absolute value)
	Theoretical Value	Design Value	Error	Theoretical Value	Design Value	Error	
44.1 kHz	−2.426	−2.453	−0.027	−7.601	−7.626	−0.025	0.04
32 kHz	−2.426	−2.291	+0.135	−7.601	−7.456	+0.145	0.19
48 kHz	−2.426	−2.420	+0.006	−7.601	−7.572	+0.029	0.05

Double Speed Operation:

(unit: dB)

Sampling Frequency fs	f = 3 kHz			f = 10 kHz			Maximum Error Value (absolute value)
	Theoretical Value	Design Value	Error	Theoretical Value	Design Value	Error	
44.1 kHz	−2.426	−2.348	+0.078	−7.601	−7.486	+0.115	0.12
32 kHz	−2.426	−2.521	−0.095	−7.601	−7.641	−0.040	0.12
48 kHz	−2.426	−2.475	−0.049	−7.601	−7.664	−0.063	0.07

5. Interpolation Filter and Dither Circuit

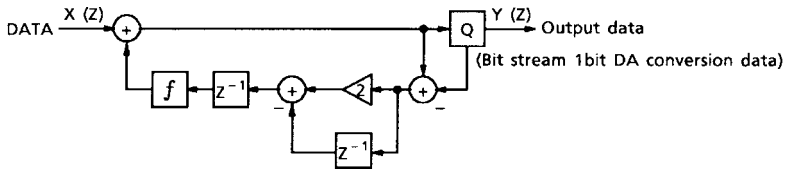
The interpolation filter linearly interpolates 8 fs (at the double speed operation: 4 fs) after the de-emphasis filter to times and over samples to 16 fs (at the double speed operation: 8 fs)

Further, in the dither circuit, DC offset and dither have been added to data in order to prevent noise by the idling pattern peculiar to the Σ-Δ modulation DA converter.

After adding the dither, 192 fs (at the double speed operation: 96 fs) is over sampled in the sample hold circuit.

6. DA Conversion Circuit

The 2'nd order ∑-Δ modulation DA converter for 2 channels (simultaneous output type) has been incorporated in the TC9237BF, TC9237BN.



2'nd order ∑-Δ modulator: $Y(Z) = X(Z) + (1 - Z^{-1})^{-2} Q(Z)$

Figure 7 Construction of Σ-Δ Modulation DA Converter

It was been so designed that clock for the ∑-Δ modulator is a half of master clock (MCK: crystal oscillation clock) and the converter operates at 192 fs at the standard operation while at 96 fs at the double speed operation (as a clock, the same as that at the standard operation).

The noise shaping characteristic is shown below.

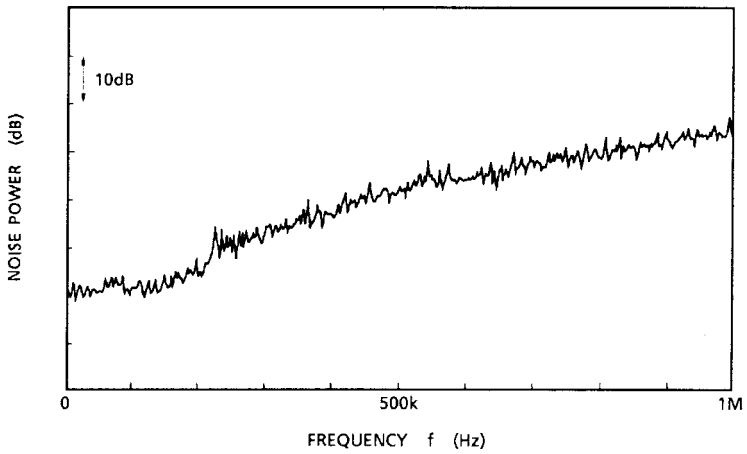


Figure 8 Noise Shaping Characteristic

7. Data Output Circuit

In this circuit, output data waveform is shaped and forward and reverse signals of bit stream data are output to the outside through a buffer.

By differentiating these forward signal and the reverse signal in the external analogue circuit, DA conversion output of low distortion factor and high S/N ratio can be obtained.

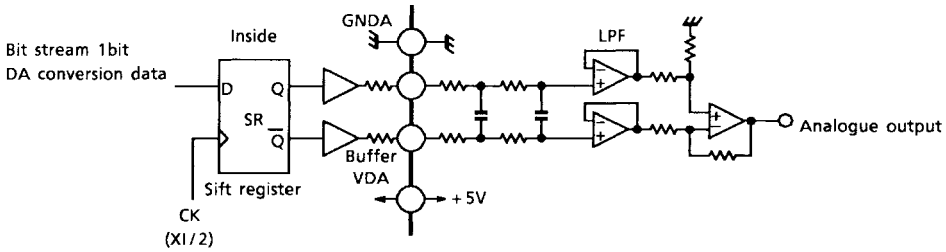


Figure 9 Construction of Data Output Circuit

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{DD}	−0.3~6.0	V
		V_{DX}		
		V_{DA}		
Input voltage		Vin	−0.3~V_{DD} + 0.3	V
Power dissipation	TC9237BF	P_D	600	mW
	TC9237BN		800	
Operating temperature		T_{opr}	−35~85	°C
Storage temperature		T_{stg}	−55~150	°C

Electrical Characteristics (unless otherwise specified, Ta = 25°C, V_{DD} = V_{DX} = V_{DA} = 5 V)

DC Characteristics

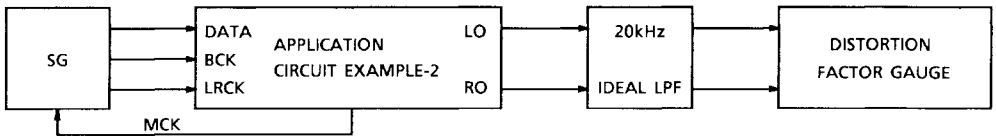
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage		V_{DD}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DX}			4.5	5.0	5.5	
		V_{DA}			4.5	5.0	5.5	
Power dissipation		I_{DD}	—	XI = 16.9 MHz	—	25	45	mA
Input voltage	"H" level	V_{IH}	—	—	V_{DD} × 0.7	—	V_{DD}	V
	"L" level	V_{IL}			0	—	V_{DD} × 0.3	
Input current	"H" level	I_{IH}	—	—	−10	—	10	μA
	"L" level	I_{IL}						
Pull-up resistor		RUP	—	TEST3, M/L, R/L pins	—	130	—	kΩ

AC Characteristics

Standard Operation (over-sampling ratio = 192 fs)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Noise distortion	THD	1	1 kHz sine wave, full-scale input	—	−87	−78	dB
S/N ratio	S/N	1	—	88	98	—	dB
Dynamic range	DR	1	1 kHz sine wave, −60dB input conversion	88	95	—	dB
Cross-talk	CT	1	1 kHz sine wave, full-scale input	—	−95	−88	dB
Operating frequency	f_{opr}	—	—	10	16.9344	19.2	MHz
Input frequency	f_{LR}	—	LRCK duty cycle = 50%	30	44.1	100	kHz
	f_{BCK}		BCK duty cycle = 50%	0.96	1.4112	6.2	MHz
Rise time	t_r	—	LRCK, BCK (10~90%)	—	—	15	ns
Fall time	t_f			—	—	15	ns
Delay time	t_d	—	BCK ↓ edge → LRCK, DATA	—	—	40	ns

Test Circuit-1: Application Circuit Example-2 is Used.



SG: ANRITSU MG-22A or equivalent

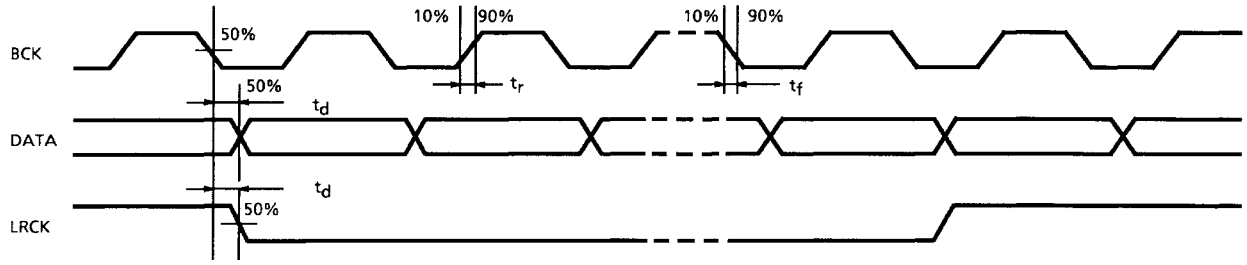
LPF: MURATA SEISAKUSHO AFL89FB20000A2 or equivalent

Distortion factor gauge: SIBASOKU 725B or equivalent

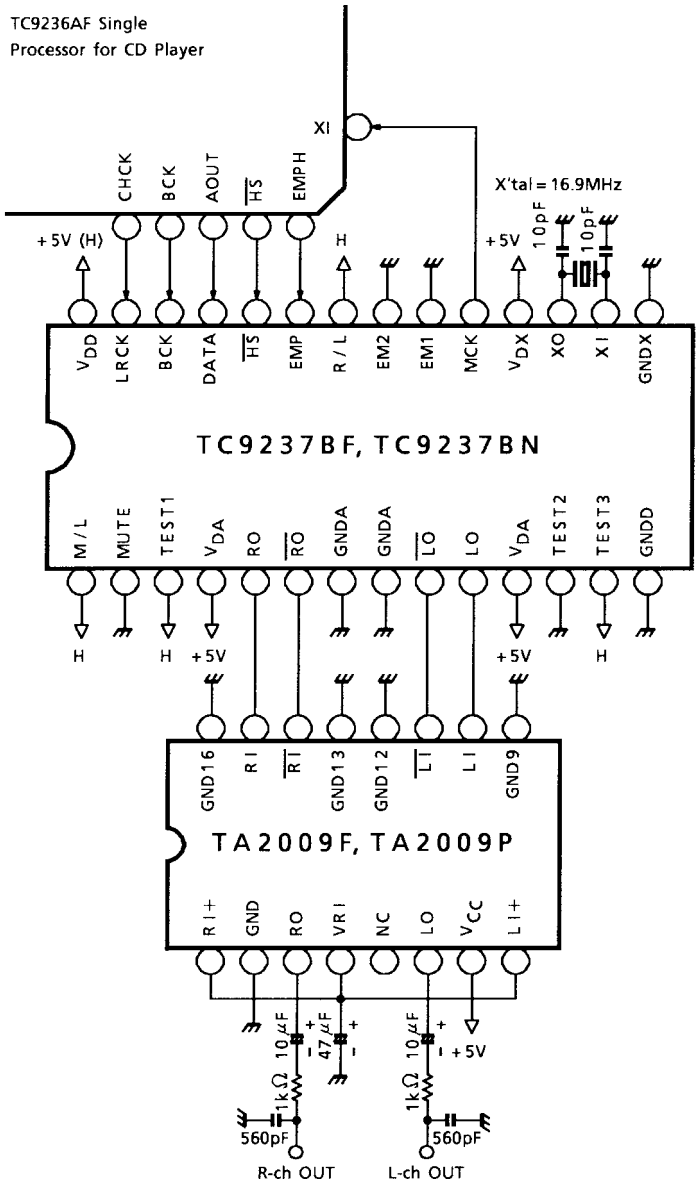
Measuring Item	Distortion Factor Gauge Filter Setting a Weight
THD + N, CT	OFF
S/N, DR	ON

A weight: IEC-A or equivalent

AC Characteristic Point (input signal: LRCK, BCK, DATA)



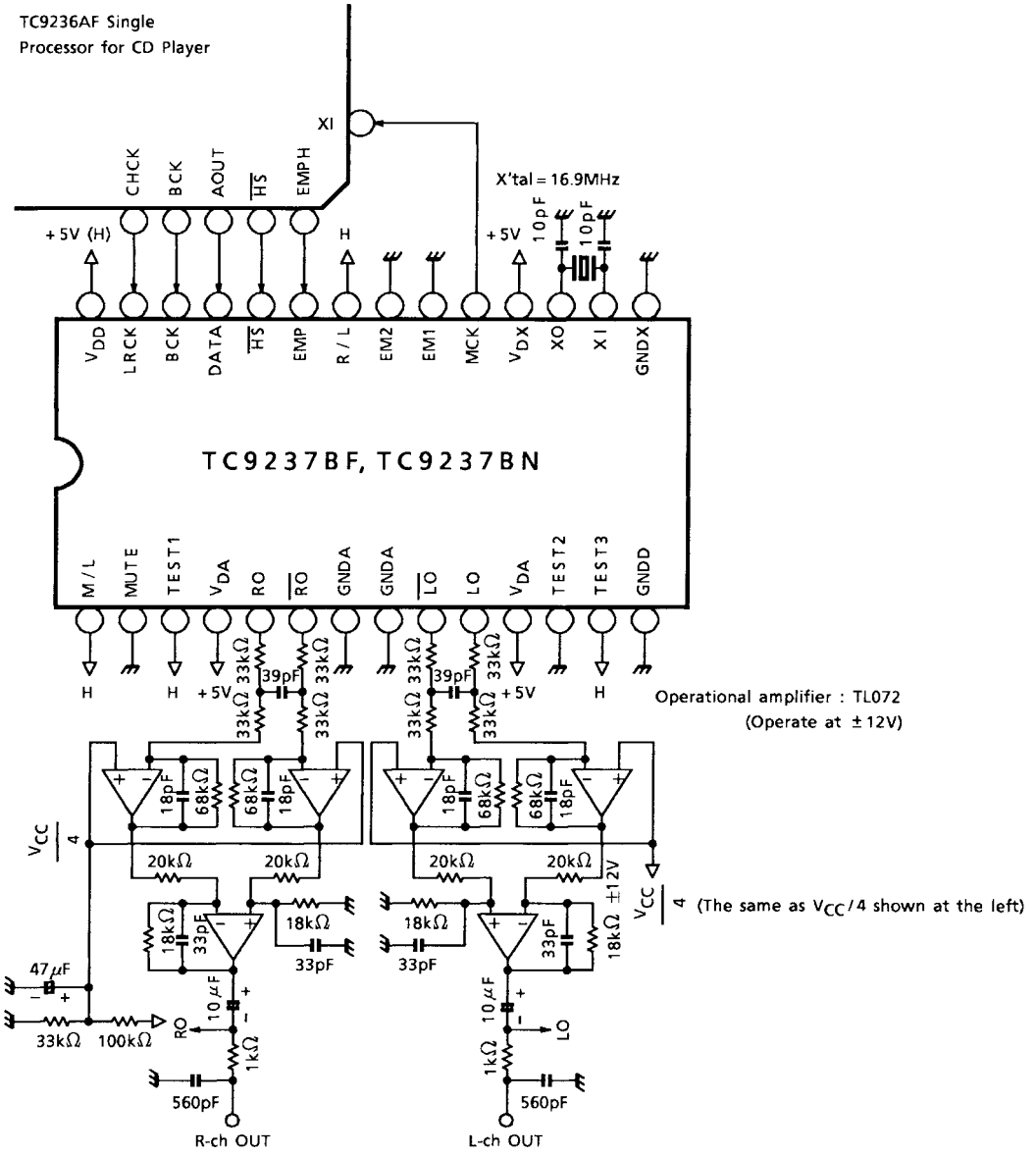
Application Circuit Example-1 (+5 V single power supply used)



Cautions

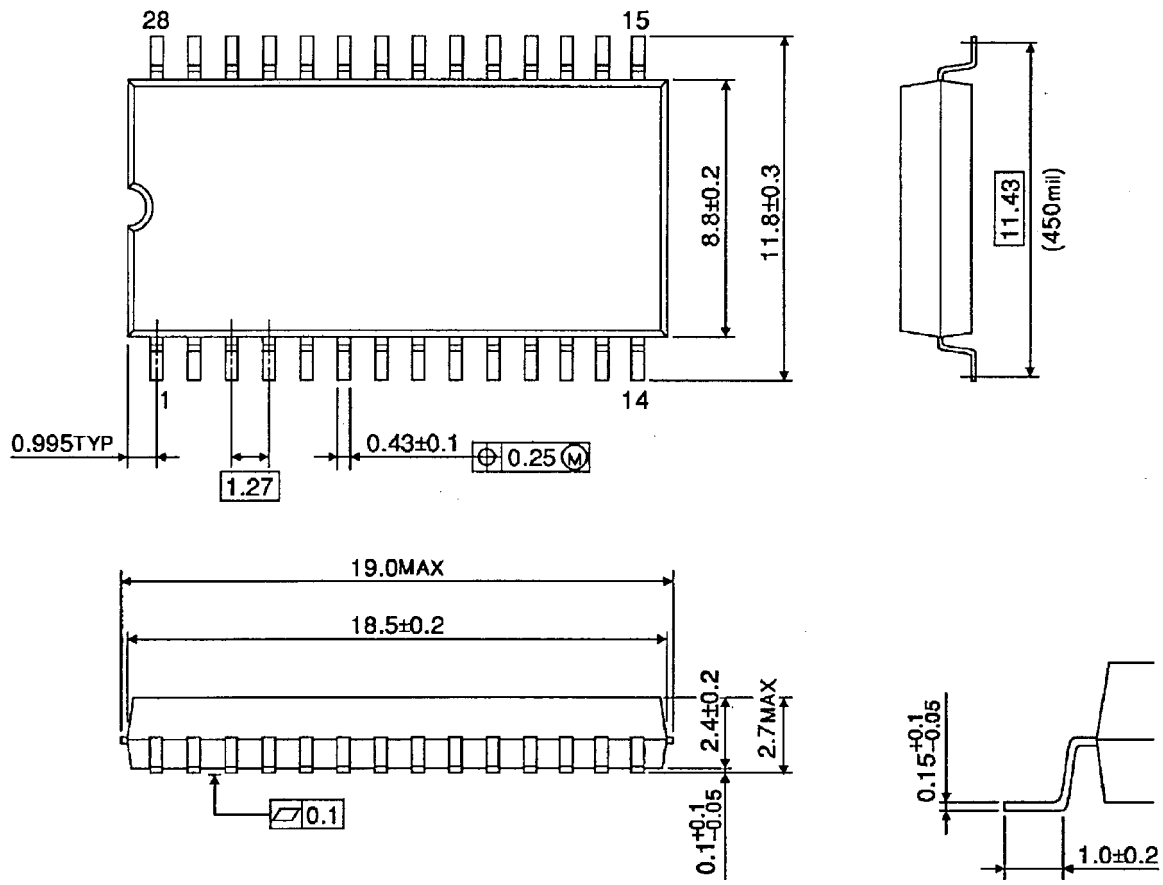
- Quality of crystal oscillation waveform largely affects S/N ratio.
  Further, this is also true when system clock is input externally through the XI pin of pin 16.
- Suppress of input signals (LRCK, BCK, DATA) as could as possible.
- The wiring between the TC9237BF, TC9237BN output and the analogue filter amplifier input must be made the shortest.
- The capacitor between V_{DA} and GNDA shall be connected as close to the pin as possible.

Application Circuit Example-2 (+5 V two power supply used)



Package Dimensions

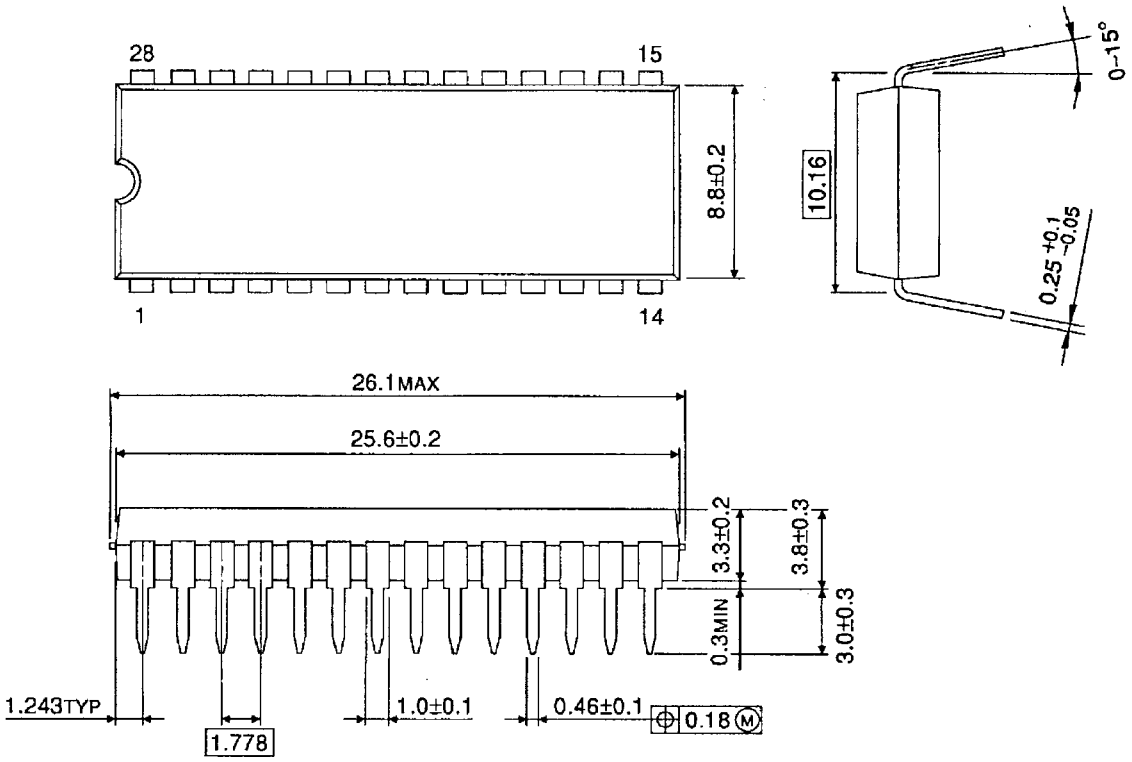
SOP28-P-450-1.27 Unit : mm



Weight: 0.8 g (typ.)

Package Dimensions

SDIP28-P-400-1.78 Unit : mm



Weight: 2.2 g (typ.)

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