



---

The following document contains information on Cypress products. Although the document is marked with the name "Spansion" and "Fujitsu", the company that originally developed the specification, Cypress will continue to offer these products to new and existing customers.

#### **Continuity of Specifications**

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

#### **Continuity of Ordering Part Numbers**

Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

#### **For More Information**

Please contact your local sales office for additional information about Cypress products and solutions.

#### **About Cypress**

Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

### ***Colophon***

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for any use that includes fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for any use where chance of failure is intolerable (i.e., submersible repeater and artificial satellite). Please note that Spansion will not be liable to you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the US Export Administration Regulations or the applicable laws of any other country, the prior authorization by the respective government entity will be required for export of those products.

### ***Trademarks and Notice***

The contents of this document are subject to change without notice. This document may contain information on a Spansion product under development by Spansion. Spansion reserves the right to change or discontinue work on any product without notice. The information in this document is provided as is without warranty or guarantee of any kind as to its accuracy, completeness, operability, fitness for particular purpose, merchantability, non-infringement of third-party rights, or any other warranty, express, implied, or statutory. Spansion assumes no liability for any damages of any kind arising out of the use of the information in this document.

Copyright © 2013 Spansion Inc. All rights reserved. Spansion®, the Spansion logo, MirrorBit®, MirrorBit® Eclipse™, ORNAND™ and combinations thereof, are trademarks and registered trademarks of Spansion LLC in the United States and other countries. Other names used are for informational purposes only and may be trademarks of their respective owners.

## 32-bit Microcontroller

CMOS

# FR60 MB91460E Series

## MB91F467EA

### ■ DESCRIPTION

MB91460E series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family\* of CPUs.

This series contains the LIN-USART and CAN controllers.

\* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Semiconductor Limited.

### ■ FEATURES

#### 1. FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support  
    Signed 32-bit multiplication : 5 cycles  
    Signed 16-bit multiplication : 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)

(Continued)

For the information for microcontroller supports, see the following web site.

This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevice.fujitsu.com/micom/en-support/>

(Continued)

- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

## 2. Internal peripheral resources

- General-purpose ports : Maximum 170 ports
- DMAC (DMA Controller)
  - Maximum of 5 channels able to operate simultaneously. (External to external : 1 channel)
  - 3 transfer sources (external pin/internal peripheral/software)
  - Activation source can be selected using software.
  - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  - Transfer data size selectable from 8/16/32-bit
  - Multi-byte transfer enabled (by software)
  - DMAC descriptor in I/O areas (200<sub>H</sub> to 240<sub>H</sub>, 1000<sub>H</sub> to 1024<sub>H</sub>)
- A/D converter (successive approximation type)
  - 10-bit resolution: 24 channels
  - Conversion time: minimum 1  $\mu$ s
- External interrupt inputs : 14 channels
  - 8 channels shared with CAN RX or I<sup>2</sup>C pins
- Bit search module (for REALOS)
  - Function to search from the MSB (most significant bit) for the position of the first "0", "1", or changed bit in a word
- LIN-USART (full duplex double buffer): 5 channels
  - Clock synchronous/asynchronous selectable
  - Sync-break detection
  - Internal dedicated baud rate generator
- I<sup>2</sup>C\* bus interface (supports 400 kbps): 3 channels
  - Master/slave transmission and reception
  - Arbitration function, clock synchronization function
- CAN controller (C-CAN): 2 channels
  - Maximum transfer speed: 1 Mbps
  - 32 transmission/reception message buffers
- Stepper motor controller : 6 channels
  - 4 high current output to each channel
  - 2 synchronized PWMs per channel (8/10-bit)
- Sound generator : 1 channel
  - Tone frequency : PWM frequency divide-by-two (reload value + 1)
- Alarm comparator : 1 channel
  - Monitor external voltage
  - Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
- 16-bit PPG timer : 12 channels
- 16-bit PFM timer : 1 channel
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: 8 channels (operates in conjunction with the free-run timer)
- Output compare: 4 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 3 channels (3\*8-bit or 1\*16-bit + 1\*8-bit)
- Watchdog timer

(Continued)

(Continued)

- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Supply Supervisor: Low voltage detection circuit for external  $V_{DD5}$  and internal 1.8V core voltage
- Clock supervisor  
Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
- Clock monitor
- Sub-clock calibration  
Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer  
Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer  
Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

### 3. Shutdown mode

- In low leakage shutdown mode, the internal main power supply is switched off. Only the following resources and memories remain active:
  - Standby RAM (16 KByte)
  - Real Time Clock
  - 4 MHz oscillator, 32 kHz oscillator, RC oscillator
  - Power management logic
  - Hardware Watchdog and Clock Supervisor

### 4. Package and technology

- Package : LQFP-208 (low profile QFP)
- CMOS 0.18  $\mu$ m technology
- Power supply range 3 V to 5 V (1.9V/1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between  $-40^{\circ}\text{C}$  and  $+105^{\circ}\text{C}$

# MB91460E Series

## ■ PRODUCT LINEUP

Feature	MB91FV460B	MB91F467DA MB91F467DB	MB91F467EA
Max. core frequency (CLKB)	100MHz	96MHz	100MHz
Max. resource frequency (CLKP)	50MHz	48MHz	50MHz
Max. external bus freq. (CLKT)	50MHz	48MHz	50MHz
Max. CAN frequency (CLKCAN)	50MHz	48MHz	50MHz
Technology	0.18um	0.18um	0.18um
Software-Watchdog	yes	yes	yes
Hardware-Watchdog (RC osc. based)	yes (disengageable), can be activated in SLEEP/STOP	yes	yes, can be activated in SLEEP/STOP
Bit Search	yes	yes	yes
Reset input (INITX)	yes	yes	yes
Clock Modulator	yes	yes	yes
Clock Monitor	yes	yes	yes
Low Power Mode	yes	yes	yes
Shutdown Mode	no, emulation by software	no	yes
DMA	5 ch	5 ch	5 ch
MMU/MPU	MPU (16 ch) <sup>1)</sup>	MPU (8 ch) <sup>1)</sup>	MPU (8 ch) <sup>1)</sup>
Flash memory	2112 KByte or external emulation SRAM	1088 KByte	1088 KByte
Flash Protection	yes	yes	yes
D-RAM	64 KByte	32 KByte	64 KByte
ID-RAM	64 KByte	32 KByte	48 KByte
Standby RAM	no	no	16 KByte
Flash-Cache (F-cache)	16 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	16 KByte Boot Flash	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch
Free Running Timer	8 ch	8 ch	8 ch
ICU	8 ch	8 ch	8 ch
OCU	8 ch	4 ch	4 ch
Reload Timer	8 ch	8 ch	8 ch
PPG 16-bit	16 ch	12 ch	12 ch
PFM 16-bit	1 ch	1 ch	1 ch

# MB91460E Series

Feature	MB91FV460B	MB91F467DA MB91F467DB	MB91F467EA
Sound Generator	1 ch	1 ch	1 ch
Up/Down Counter (8/16-bit)	4 ch (8-bit) / 2 ch (16-bit)	3 ch (8-bit) / 1 ch (16-bit)	3 ch (8-bit) / 1 ch (16-bit)
C_CAN	6 ch (128msg)	3 ch (32msg)	2 ch (32msg)
LIN-USART	16 ch FIFO	1 ch + 4 ch FIFO	1 ch + 4 ch FIFO
I2C (400k)	8 ch	3 ch	3 ch
FR external bus	yes (32bit addr, 32bit data)	yes (26bit addr, 32bit data)	yes (26bit addr, 32bit data)
External Interrupts	32 ch	14 ch	14 ch
SMC	6 ch	6 ch	6 ch
ADC (10 bit)	32 ch, with Range Comparator	24 ch	24 ch, with Range Comparator
Alarm Comparator	2 ch	1 ch	1 ch
Supply Supervisor (low voltage detection)	yes	yes	yes
Clock Supervisor	yes	yes	yes
Main clock oscillator	4MHz	4MHz	4MHz
Sub clock oscillator	32kHz	32kHz	32kHz
RC Oscillator	100kHz / 2MHz	100kHz / 2MHz	100kHz / 2MHz
PLL	x 25	x 24	x 25
DSU4	yes	-	-
EDSU	yes (32 BP) *1	yes (16 BP) *1	yes (16 BP) *1
Supply Voltage	1.8V + 3V / 5V	3V / 5V	3V / 5V
Regulator	no	yes	yes
Power Consumption	n.a.	< 2 W	< 1.3 W
Temperatur Range (Ta)	0..70 C	-40..105 C	-40..105 C
Package	BGA896	QFP208	LQFP208

# MB91460E Series

Feature	MB91FV460B	MB91F467DA MB91F467DB	MB91F467EA
Power on to PLL run	< 20 ms	< 20 ms	< 20 ms
Flash Download Time	< 8 sec typical	< 6 sec typical	< 6 sec typical

\*1 : MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

## ■ PIN ASSIGNMENT

### 1. MB91F467EA

(TOP VIEW)

VSS5	1
P01_0/D16	2
P01_1/D17	3
P01_2/D18	4
P01_3/D19	5
P01_4/D20	6
P01_5/D21	7
P01_6/D22	8
P01_7/D23	9
P00_0/D24	10
P00_1/D25	11
P00_2/D26	12
P00_3/D27	13
P00_4/D28	14
P00_5/D29	15
P00_6/D30	16
P00_7/D31	17
P07_0/A0	18
P07_1/A1	19
P07_2/A2	20
P07_3/A3	21
P07_4/A4	22
P07_5/A5	23
P07_6/A6	24
P07_7/A7	25
VDD35	26
VSS5	27
P06_0/A8	28
P06_1/A9	29
P06_2/A10	30
P06_3/A11	31
P06_4/A12	32
P06_5/A13	33
P06_6/A14	34
P06_7/A15	35
P05_0/A16	36
P05_1/A17	37
P05_2/A18	38
P05_3/A19	39
P05_4/A20	40
P05_5/A21	41
P05_6/A22	42
P05_7/A23	43
P04_0/A24	44
P04_1/A25	45
P08_0/WRX0	46
P08_1/WRX1	47
P08_2/WRX2	48
P08_3/WRX3	49
P08_4/FDX	50
P08_5/BGNTX	51
VDD35	52

QFP-208

VSS	3
P08_6/BDY	4
P08_7/CS0	5
P19_0/CS0	6
P19_1/CS1	7
P19_2/CS2	8
P19_3/CS3	9
P19_4/CS4	10
P19_5/CS5	11
P19_6/CS6	12
P19_7/CS7	13
P10_1/ASX	14
P10_2/BAX	15
P10_3/MAX	16
P10_4/MLO	17
P10_5/MOL	18
P10_6/MOLC	19
VSS	20
MD_1	21
MD_0	22
INTX	23
XIA	24
XOA	25
XOB	26
MD_2	27
INTO	28
VDD5	29
VSS	30
VCC18C	31
VDD5R	32
VDD5R	33
P24_0/INT1	34
P24_1/INT2	35
P24_2/INT3	36
P24_3/INT4	37
P24_4/INT5	38
P24_5/INT6	39
P24_6/INT7	40
P24_7/INT8	41
P23_0/ER0/INT0	42
P23_1/INT1	43
P23_2/ER1/INT0	44
P23_3/INT1	45
P23_4/INT0	46
P22_0/INT12	47
P22_1/INT13	48
P22_2/INT14	49
P22_3/SDA0/INT4	50
P22_4/SDA1/INT4	51
P20_0/SIN2/AIN0	52
P20_1/SIN2/AIN0	53
P20_2/SIN2/AIN0	54
VDD5	55
VSS5	56
VDD35	57
P13_0/DO	58
P13_1/DACK0	59
P13_2/DETOX0/DEPO	60
P13_3/DEPO	61
P13_4/DHE0	62
P25_3/SMC2P4	63
P25_4/SMC2P4	64
P25_5/SMC1P5	65
P25_6/SMC1P5	66
P25_7/SMC2P3/AN31	67
P26_1/SMC1P2/AN30	68
P26_2/SMC2P2/AN29	69
P26_3/SMC2P2/AN27	70
P26_4/SMC1P4	71
P26_5/SMC1P4	72
P26_6/SMC2P1/AN26	73
P26_7/SMC2P1/AN25	74
P26_8/SMC2P1/AN24	75
P26_9/SMC2P1/AN23	76
P27_0/SMC1P1/AN22	77
P27_1/SMC1P1/AN21	78
P27_2/SMC2P0/AN19	79
P27_3/SMC1P0/AN18	80
P27_4/SMC1P0/AN17	81
HVSS	82
HVSS	83
HVSS	84
HVSS	85
HVSS	86
HVSS	87
HVSS	88
HVSS	89
HVSS	90
HVSS	91
HVSS	92
HVSS	93
HVSS	94
HVSS	95
HVSS	96
HVSS	97
HVSS	98
HVSS	99
HVSS	100
HVSS	101
HVSS	102
HVSS	103
HVSS	104
HVSS	105

FPT-208P-M06

Note: Difference versus MB91460D series: At pins 95+96, RX2 and TX2 of CAN2 are removed.

# MB91460E Series

## ■ PIN DESCRIPTION

### 1. MB91F467EA

Pin no.	Pin name	I/O	I/O circuit type *1	Function
2 to 9	P01_0 to P01_7	I/O	A	General-purpose input/output ports
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
10 to 17	P00_0 to P00_7	I/O	A	General-purpose input/output ports
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
18 to 25	P07_0 to P07_7	I/O	A	General-purpose input/output ports
	A0 to A7			Signal pins of external address bus (bit0 to bit7)
28 to 35	P06_0 to P06_7	I/O	A	General-purpose input/output ports
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
36 to 43	P05_0 to P05_7	I/O	A	General-purpose input/output ports
	A16 to A23			Signal pins of external address bus (bit16 to bit23)
44, 45	P04_0, P04_1	I/O	A	General-purpose input/output ports
	A24, A25			Signal pins of external address bus (bit24, bit25)
46 to 49	P08_0 to P08_3	I/O	A	General-purpose input/output ports
	WRX0 to WRX3			External write strobe output pins
50	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
51	P08_5	I/O	A	General-purpose input/output port
	BGRNTX			External bus release reception output pin
54	P08_6	I/O	A	General-purpose input/output port
	BRQ			External bus release request input pin
55	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
56 to 59	P09_0 to P09_3	I/O	A	General-purpose input/output ports
	CSX0 to CSX3			Chip select output pins
60, 61	P09_6, P09_7	I/O	A	General-purpose input/output ports
	CSX6, CSX7			Chip select output pins
62	P10_1	I/O	A	General-purpose input/output port
	ASX			Address strobe output pin
63	P10_2	I/O	A	General-purpose input/output port
	BAAX			Burst address advance output pin
64	P10_3	I/O	A	General-purpose input/output port
	WEX			Write enable output pin
65	P10_4	I/O	A	General-purpose input/output port
	MCLKO			Clock output pin for memory

(Continued)

(Continued)

Pin no.	Pin name	I/O	I/O circuit type <sup>*1</sup>	Function
66	P10_5	I/O	A	General-purpose input/output port
	MCLKI			Clock input pin for memory
67	P10_6	I/O	A	General-purpose input/output port
	MCLKE			Clock enable signal pin for memory
68	MONCLK	O	M	Clock monitor pin
70	MD_2	I	G	Mode setting pins
71	MD_1	I	G	
72	MD_0	I	G	
73	INITX	I	H	External reset input pin
74	X1A	—	J2	Sub clock (oscillation) output
75	X0A	—	J2	Sub clock (oscillation) input
76	X1	—	J1	Clock (oscillation) output
77	X0	—	J1	Clock (oscillation) input
83 to 86	P24_0 to P24_3	I/O	A	General-purpose input/output ports
	INT0 to INT3			External interrupt input pins
87	P24_4	I/O	C	General-purpose input/output port
	INT4			External interrupt input pin
	SDA2			I <sup>2</sup> C bus DATA input/output pin
88	P24_5	I/O	C	General-purpose input/output port
	INT5			External interrupt input pin
	SCL2			I <sup>2</sup> C bus clock input/output pin
89	P24_6	I/O	C	General-purpose input/output port
	INT6			External interrupt input pin
	SDA3			I <sup>2</sup> C bus DATA input/output pin
90	P24_7	I/O	C	General-purpose input/output port
	INT7			External interrupt input pin
	SCL3			I <sup>2</sup> C bus clock input/output pin
91	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pin
92	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0
93	P23_2	I/O	A	General-purpose input/output port
	RX1			RX input pin of CAN1
	INT9			External interrupt input pin

(Continued)

# MB91460E Series

(Continued)

Pin no.	Pin name	I/O	I/O circuit type <sup>*1</sup>	Function
94	P23_3	I/O	A	General-purpose input/output port
	TX1			TX output pin of CAN1
95 <sup>*2</sup>	P23_4	I/O	A	General-purpose input/output port
	INT10			External interrupt input pin
96 <sup>*2</sup>	P23_5	I/O	A	General-purpose input/output port
97	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
98	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
99	P22_4	I/O	C	General-purpose input/output port
	SDA0			I <sup>2</sup> C bus data input/output pin
	INT14			External interrupt input pin
100	P22_5	I/O	C	General-purpose input/output port
	SCL0			I <sup>2</sup> C bus clock input/output pin
101	P20_0	I/O	A	General-purpose input/output port
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
102	P20_1	I/O	A	General-purpose input/output port
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
103	P20_2	I/O	A	General-purpose input/output port
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
106	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin of USART4
107	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin of USART4
108	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4

(Continued)

(Continued)

Pin no.	Pin name	I/O	I/O circuit type <sup>*1</sup>	Function
109	P19_4	I/O	A	General-purpose input/output port
	SIN5			Data input pin of USART5
110	P19_5	I/O	A	General-purpose input/output port
	SOT5			Data output pin of USART5
111	P19_6	I/O	A	General-purpose input/output port
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
112	P18_0	I/O	A	General-purpose input/output port
	SIN6			Data input pin of USART6
	AIN2			Up/down counter input pin
113	P18_1	I/O	A	General-purpose input/output port
	SOT6			Data output pin of USART6
	BIN2			Up/down counter input pin
114	P18_2	I/O	A	General-purpose input/output port
	SCK6			Clock input/output pin of USART6
	ZIN2			Up/down counter input pin
	CK6			External clock input pin of free-run timer 6
115	P18_4	I/O	A	General-purpose input/output port
	SIN7			Data input pin of USART7
	AIN3			Up/down counter input pin
116	P18_5	I/O	A	General-purpose input/output port
	SOT7			Data output pin of USART7
	BIN3			Up/down counter input pin
117	P18_6	I/O	A	General-purpose input/output port
	SCK7			Clock input/output pin of USART7
	ZIN3			Up/down counter input pin
	CK7			External clock input pin of free-run timer 7
118 to 121	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
122 to 129	P14_0 to P14_7	I/O	A	General-purpose input/output ports
	ICU0 to ICU7			Input capture input pins
	TIN0 to TIN7			External trigger input pins of reload timer
	TTG8 to TTG11, TTG4/12 to TTG7/15			External trigger input pins of PPG timer

(Continued)

# MB91460E Series

(Continued)

Pin no.	Pin name	I/O	I/O circuit type <sup>*1</sup>	Function
132 to 135	P17_4 to P17_7	I/O	A	General-purpose input/output ports
	PPG4 to PPG7			Output pins of PPG timer
136 to 139	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			PPG timer output pins
140	P16_4	I/O	A	General-purpose input/output port
	PPG12			Output pin of PPG timer
	SGA			SGA output pin of sound generator
141	P16_5	I/O	A	General-purpose input/output port
	PPG13			Output pin of PPG timer
	SGO			SGO output pin of sound generator
142	P16_6	I/O	A	General-purpose input/output port
	PPG14			Output pin of PPG timer
	PFM			Pulse frequency modulator output pin
143	P16_7	I/O	A	General-purpose input/output port
	PPG15			PPG timer output pin
	ATGX			A/D converter external trigger input pin
147	ALARM_0	I	N	Alarm comparator input pin
148 to 155	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins of A/D converter
158	P27_0	I/O	F	General-purpose input/output port
	SMC1P0			Controller output pin of Stepper motor
	AN16			Analog input pin of A/D converter
159	P27_1	I/O	F	General-purpose input/output port
	SMC1M0			Controller output pin of Stepper motor
	AN17			Analog input pin of A/D converter
160	P27_2	I/O	F	General-purpose input/output port
	SMC2P0			Controller output pin of Stepper motor
	AN18			Analog input pin of A/D converter
161	P27_3	I/O	F	General-purpose input/output port
	SMC2M0			Controller output pin of Stepper motor
	AN19			Analog input pin of A/D converter
164	P27_4	I/O	F	General-purpose input/output port
	SMC1P1			Controller output pin of Stepper motor
	AN20			Analog input pin of A/D converter

(Continued)

(Continued)

Pin no.	Pin name	I/O	I/O circuit type <sup>*1</sup>	Function
165	P27_5	I/O	F	General-purpose input/output port
	SMC1M1			Controller output pin of Stepper motor
	AN21			Analog input pin of A/D converter
166	P27_6	I/O	F	General-purpose input/output port
	SMC2P1			Controller output pin of Stepper motor
	AN22			Analog input pin of A/D converter
167	P27_7	I/O	F	General-purpose input/output port
	SMC2M1			Controller output pin of Stepper motor
	AN23			Analog input pin of A/D converter
168	P26_0	I/O	F	General-purpose input/output port
	SMC1P2			Controller output pin of Stepper motor
	AN24			Analog input pin of A/D converter
169	P26_1	I/O	F	General-purpose input/output port
	SMC1M2			Controller output pin of Stepper motor
	AN25			Analog input pin of A/D converter
170	P26_2	I/O	F	General-purpose input/output port
	SMC2P2			Controller output pin of Stepper motor
	AN26			Analog input pin of A/D converter
171	P26_3	I/O	F	General-purpose input/output port
	SMC2M2			Controller output pin of Stepper motor
	AN27			Analog input pin of A/D converter
174	P26_4	I/O	F	General-purpose input/output port
	SMC1P3			Controller output pin of Stepper motor
	AN28			Analog input pin of A/D converter
175	P26_5	I/O	F	General-purpose input/output port
	SMC1M3			Controller output pin of Stepper motor
	AN29			Analog input pin of A/D converter
176	P26_6	I/O	F	General-purpose input/output port
	SMC2P3			Controller output pin of Stepper motor
	AN30			Analog input pin of A/D converter
177	P26_7	I/O	F	General-purpose input/output port
	SMC2M3			Controller output pin of Stepper motor
	AN31			Analog input pin of A/D converter

(Continued)

# MB91460E Series

(Continued)

Pin no.	Pin name	I/O	I/O circuit type <sup>*1</sup>	Function
178	P25_0	I/O	E	General-purpose input/output port
	SMC1P4			Controller output pin of Stepper motor
179	P25_1	I/O	E	General-purpose input/output port
	SMC1M4			Controller output pin of Stepper motor
180	P25_2	I/O	E	General-purpose input/output port
	SMC2P4			Controller output pin of Stepper motor
181	P25_3	I/O	E	General-purpose input/output port
	SMC2M4			Controller output pin of Stepper motor
184	P25_4	I/O	E	General-purpose input/output port
	SMC1P5			Controller output pin of Stepper motor
185	P25_5	I/O	E	General-purpose input/output port
	SMC1M5			Controller output pin of Stepper motor
186	P25_6	I/O	E	General-purpose input/output port
	SMC2P5			Controller output pin of Stepper motor
187	P25_7	I/O	E	General-purpose input/output port
	SMC2M5			Controller output pin of Stepper motor
189	P13_0	I/O	A	General-purpose input/output port
	DREQ0			DMA external transfer request input
190	P13_1	I/O	A	General-purpose input/output port
	DACKX0			DMA external transfer acknowledge output pin
191	P13_2	I/O	A	General-purpose input/output port
	DEOTX0			DMA external transfer EOT (End of Track) output pin
	DEOP0			DMA external transfer EOP (End of Process) output pin
192 to 199	P03_0 to P03_7	I/O	A	General-purpose input/output ports
	D0 to D7			Signal pins of external data bus (bit0 to bit7)
200 to 207	P02_0 to P02_7	I/O	A	General-purpose input/output ports
	D8 to D15			Signal pins of external data bus (bit8 to bit15)

\*1 : For information about the I/O circuit type, refer to "■ I/O CIRCUIT TYPES".

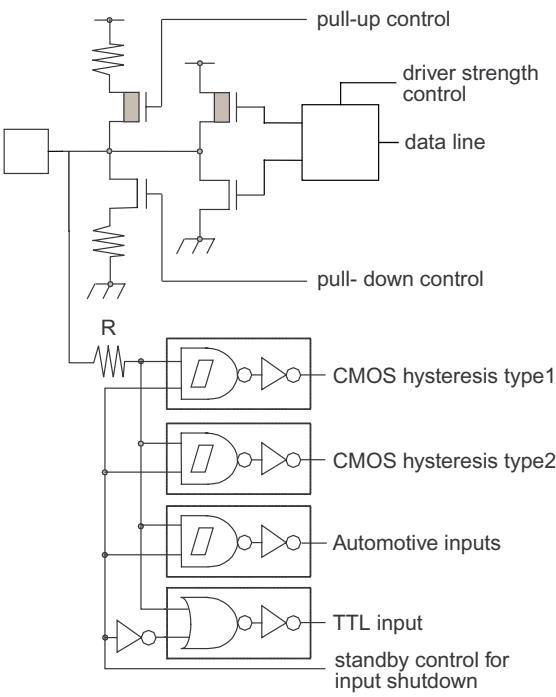
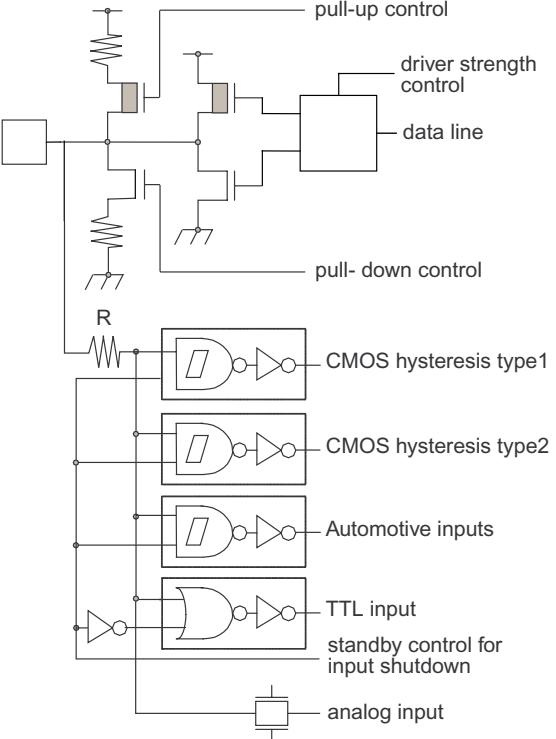
\*2 : Difference versus MB91460D series: At pins 95+96, RX2 and TX2 of CAN2 are removed.

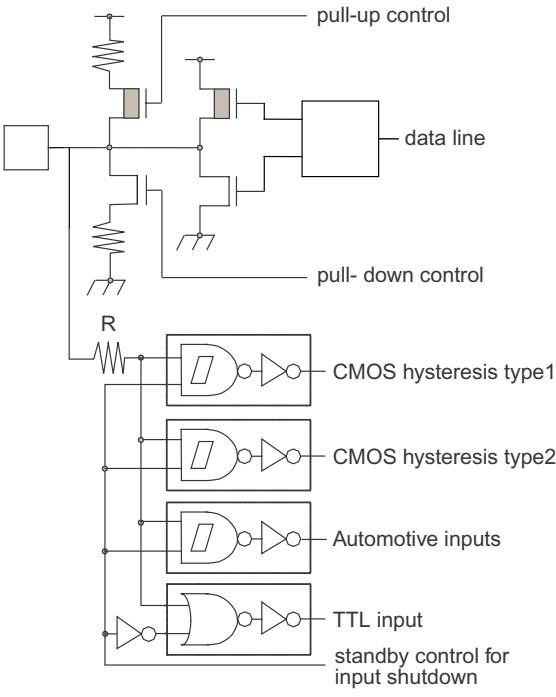
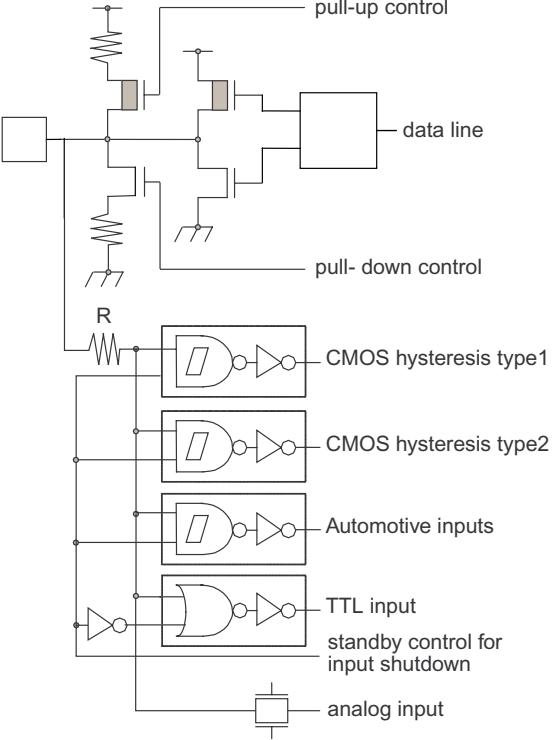
## 2. Power supply/Ground pins

Pin no.	Pin name	I/O	Function
1, 27, 53, 69, 79, 105, 131, 157, 188	VSS5	Supply	Ground pins
163, 173, 183	HVSS5		Ground pins for Stepper motor controller
26, 52, 208	VDD35		Power supply pins for external data bus
78, 104, 130, 156	VDD5		Power supply pins
162, 172, 182	HVDD5		Power supply pins for Stepper motor controller
81, 82	VDD5R		Power supply pins for internal regulator
144	AVSS5		Analog ground pin for A/D converter
146	AVCC5		Power supply pin for A/D converter
145	AVRH5		Reference power supply pin for A/D converter
80	VCC18C		Capacitor connection pin for internal regulator

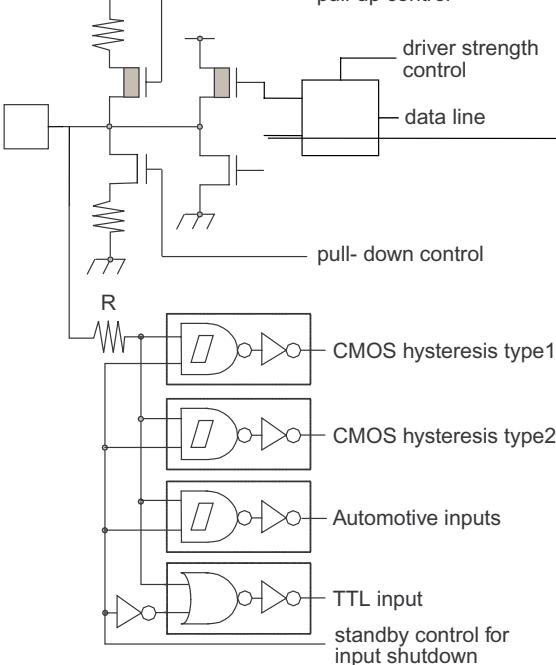
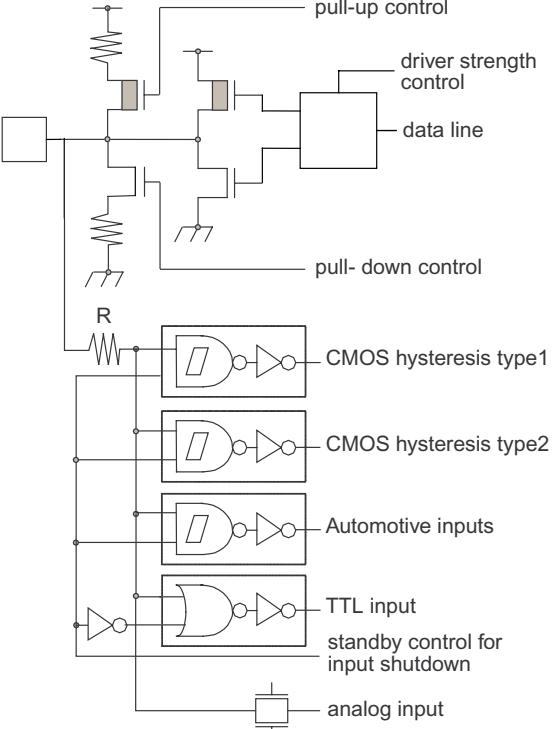
# MB91460E Series

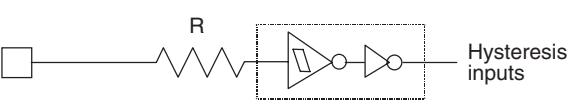
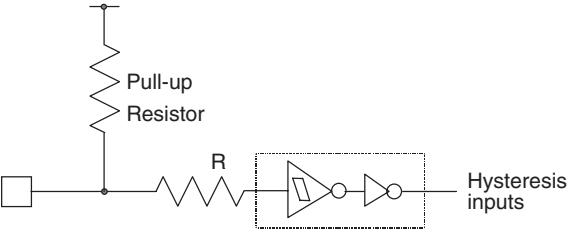
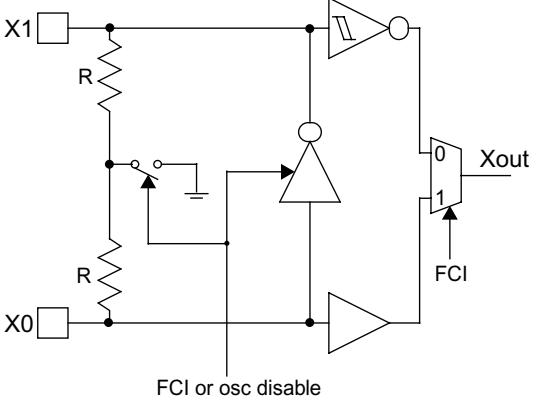
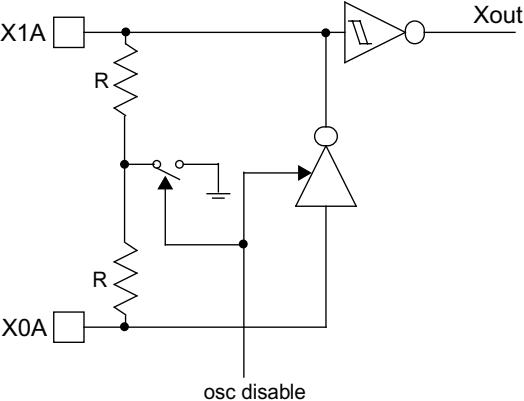
## ■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A	 <p>pull-up control</p> <p>driver strength control</p> <p>data line</p> <p>pull- down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: <math>50\text{k}\Omega</math> approx.</p>
B	 <p>pull-up control</p> <p>driver strength control</p> <p>data line</p> <p>pull- down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p> <p>analog input</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: <math>50\text{k}\Omega</math> approx.</p> <p>Analog input</p>

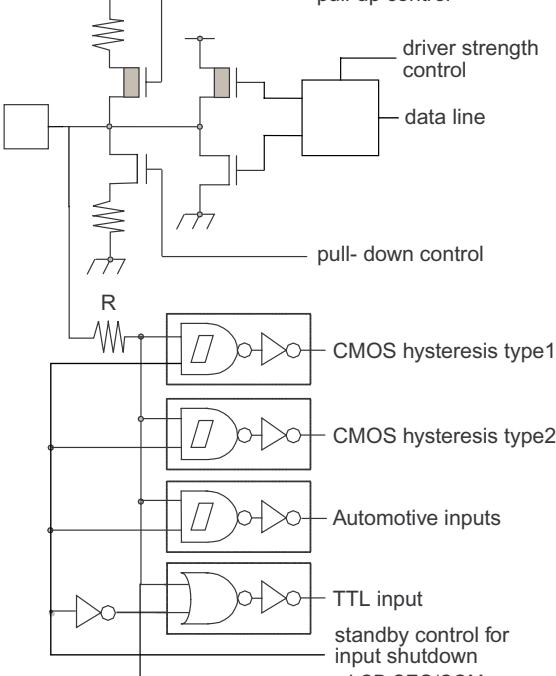
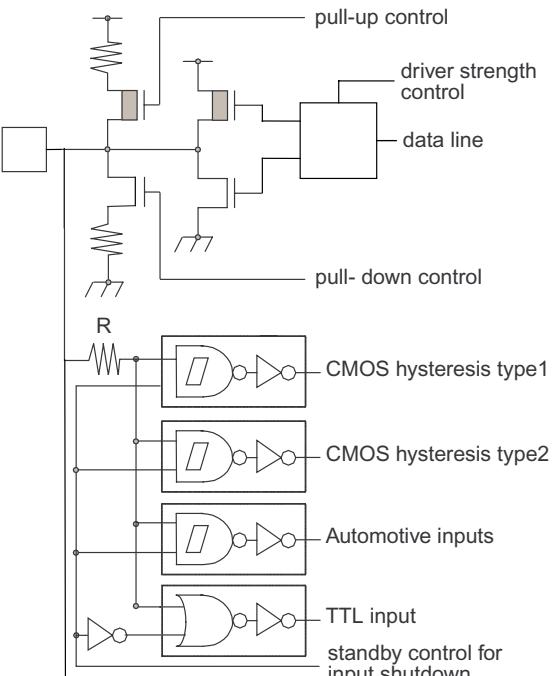
Type	Circuit	Remarks
C	 <p>pull-up control</p> <p>data line</p> <p>pull- down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p>	<p>CMOS level output (<math>I_{OL} = 3mA</math>, <math>I_{OH} = -3mA</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: <math>50k\Omega</math> approx.</p>
D	 <p>pull-up control</p> <p>data line</p> <p>pull- down control</p> <p>R</p> <p>CMOS hysteresis type1</p> <p>CMOS hysteresis type2</p> <p>Automotive inputs</p> <p>TTL input</p> <p>standby control for input shutdown</p> <p>analog input</p>	<p>CMOS level output (<math>I_{OL} = 3mA</math>, <math>I_{OH} = -3mA</math>)</p> <p>2 different CMOS hysteresis inputs with input shutdown function</p> <p>Automotive input with input shutdown function</p> <p>TTL input with input shutdown function</p> <p>Programmable pull-up resistor: <math>50k\Omega</math> approx.</p> <p>Analog input</p>

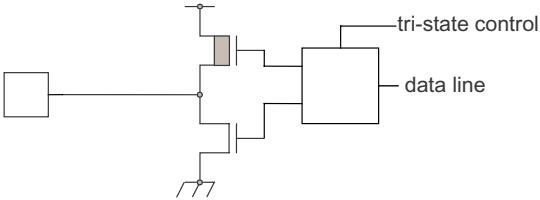
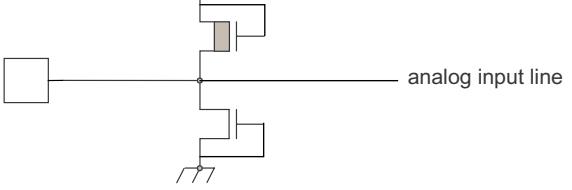
# MB91460E Series

Type	Circuit	Remarks
E	 <p>pull-up control driver strength control data line pull- down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>, and <math>I_{OL} = 30\text{mA}</math>, <math>I_{OH} = -30\text{mA}</math>) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: <math>50\text{k}\Omega</math> approx.</p>
F	 <p>pull-up control driver strength control data line pull- down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown analog input</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>, and <math>I_{OL} = 30\text{mA}</math>, <math>I_{OH} = -30\text{mA}</math>) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: <math>50\text{k}\Omega</math> approx. Analog input</p>

Type	Circuit	Remarks
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
J1		High-speed oscillation circuit: <ul style="list-style-type: none"> <li>Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)</li> <li>Feedback resistor = approx. <math>2 * 0.5 \text{ M}\Omega</math>. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.</li> </ul>
J2		Low-speed oscillation circuit: <ul style="list-style-type: none"> <li>Feedback resistor = approx. <math>2 * 5 \text{ M}\Omega</math>. Feedback resistor is grounded in the center when the oscillator is disabled.</li> </ul>

# MB91460E Series

Type	Circuit	Remarks
K	 <p>pull-up control driver strength control data line pull- down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown LCD SEG/COM</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: <math>50\text{k}\Omega</math> approx. LCD SEG/COM output</p>
L	 <p>pull-up control driver strength control data line pull- down control R CMOS hysteresis type1 CMOS hysteresis type2 Automotive inputs TTL input standby control for input shutdown VLCD</p>	<p>CMOS level output (programmable <math>I_{OL} = 5\text{mA}</math>, <math>I_{OH} = -5\text{mA}</math> and <math>I_{OL} = 2\text{mA}</math>, <math>I_{OH} = -2\text{mA}</math>) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: <math>50\text{k}\Omega</math> approx. Analog input LCD Voltage input</p>

Type	Circuit	Remarks
M	 <p>tri-state control</p> <p>data line</p>	CMOS level tri-state output ( $I_{OL} = 5\text{mA}$ , $I_{OH} = -5\text{mA}$ )
N	 <p>analog input line</p>	Analog input pin with protection

# MB91460E Series

## ■ HANDLING DEVICES

### 1. Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ( $V_{DD5}$ ,  $V_{DD35}$  or  $HV_{DD5}$ ) or less than ( $V_{SS5}$  or  $HV_{SS5}$ ) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

### 2. Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2K $\Omega$  to 10K $\Omega$ ) or enable internal pullup or pulldown resistors (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD\_x can be connected to  $V_{SS5}$  or  $V_{DD5}$  directly. Unused ALARM input pins can be connected to  $AV_{SS5}$  directly.

### 3. Power supply pins

In MB91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460 series must be connected to the current supply source via a low impedance.

It is also recommended to connect a ceramic capacitor of approximately 0.1  $\mu$ F as a bypass capacitor between power supply pin and ground pin near this device.

This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7  $\mu$ F (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

### 4. Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.

It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.

Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

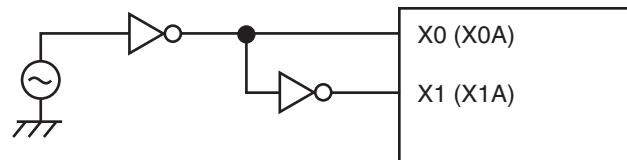
### 5. Notes on using external clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

*(Continued)*

(Continued)

Example of using opposite phase supply



## 6. Mode pins (MD\_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

## 7. Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

## 8. Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

## 9. Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

- **The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:**
  - (a) a user interrupt or NMI is accepted;
  - (b) single-step execution is performed;
  - (c) execution breaks due to a data event or from the emulator menu.
  1. D0 and D1 flags are updated in advance.
  2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
  3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.
- **The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.**
  1. The PS register is updated in advance.
  2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
  3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

## ■ NOTES ON DEBUGGER

### 1. Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

### 2. Break function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

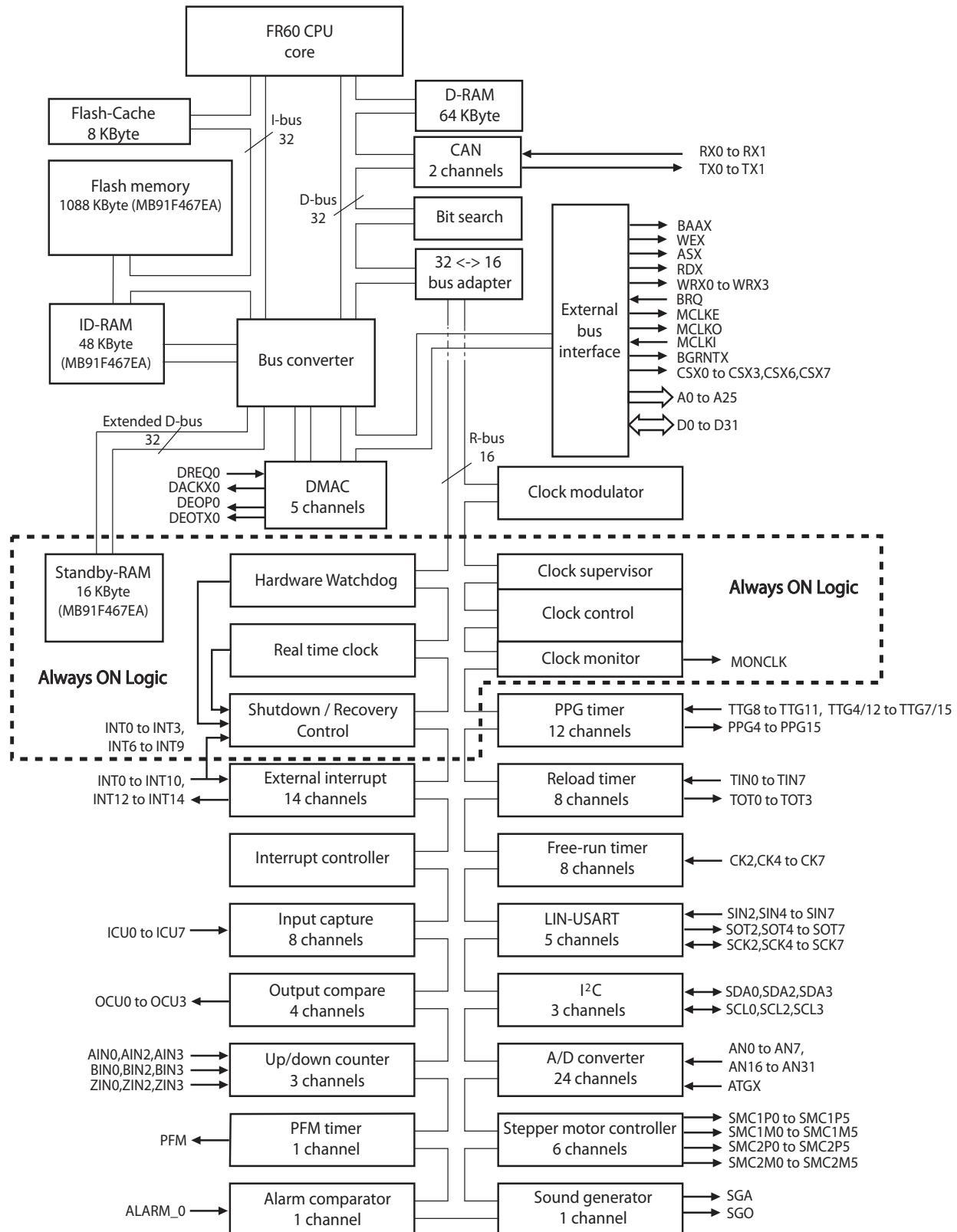
### 3. Operand break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

# MB91460E Series

## ■ BLOCK DIAGRAM

### 1. MB91F467EA



## ■ A/D CONVERTER / RANGE COMPARATOR

The new A/D Converter with Range Comparator is available on MB91FV460B and some new flash devices and is backward compatible to the A/D converter used on older devices. Beside the Range Comparator, 32 separated result data registers, a second interrupt flag and a new behaviour regarding reading the ADCS0.ACH[5:0] bits have been implemented.

There is one software incompatibility: Read-modify-write operation to the register ADCS0 is not allowed. See the description of the ADCS0.ACH[5:0] bits on 35ff.

This chapter provides an overview of the A/D converter, describes the register structure and functions, and describes the operation of the A/D converter.

### 1. Overview of A/D Converter and A/D Range Comparator

The A/D converter converts analog input voltages into digital values and provides the following features. Any ADC channel can be assigned to one of 4 Range Comparators.

#### 1.1. Features of the A/D converter:

- Conversion time: minimum 1us per channel.
- RC type successive approximation conversion with sample & hold circuit
- 10-bit or 8-bit resolution
- Program section analog input from 32 channels
- 1 common result data register and 32 dedicated channel result data registers
- Single conversion mode: Convert the specified channel(s) only once.
- Continuous mode: Repeatedly convert the specified channels.
- Scan conversion mode: Continuous conversion of multiple channels, programmable for up to 32 channels
- Stop mode: Convert one channel, then temporarily halt until the next activation.  
(Enables synchronization of the conversion start timing.)
- A/D conversion can be followed by an A/D conversion interrupt request to CPU. This interrupt, an option that is ideal for continuous processing can be used to start a DMA transfer of the results of A/D conversion to memory.
- A/D conversion of all enabled channels (scan conversion) can be followed by an A/D End of Scan interrupt request to CPU. The data is stored into dedicated channel result registers, which can be read out using DMA transfer.
- Conversion startup may be by software, external trigger (falling edge) or timer (rising edge).

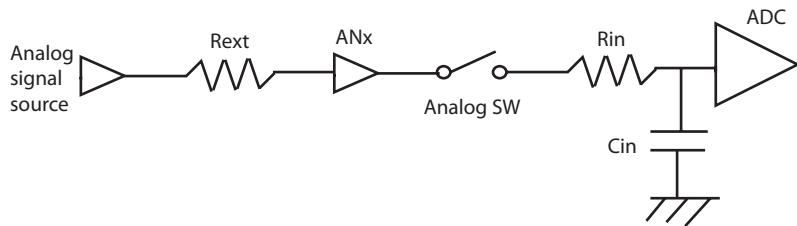
#### 1.2. Features of the A/D Range Comparator (RCO):

- 4 conversion result Range Comparator channels, comparing the upper 8 bit of the conversion result with an upper and a lower threshold. The thresholds are programmable for the 4 comparators independently.
- Any ADC channel can be assigned to one of the 4 range comparators.
- The comparison results will set “overflow” and “interrupt” flags per ADC channel, depending on the configuration. It is possible to configure the comparison for:
  - “out of range”: The flags are set if the A/D result is below the lower OR above the upper threshold.
  - “inside range”: The flags are set if the A/D result is above the lower AND below the upper threshold.
- The configuration can be set individually per ADC channel.
- Range comparison can be followed by an A/D Range Comparator interrupt request to CPU.

# MB91460E Series

## 2. A/D Converter Input Impedance

The following figure shows the sampling circuit of the A/D converter:

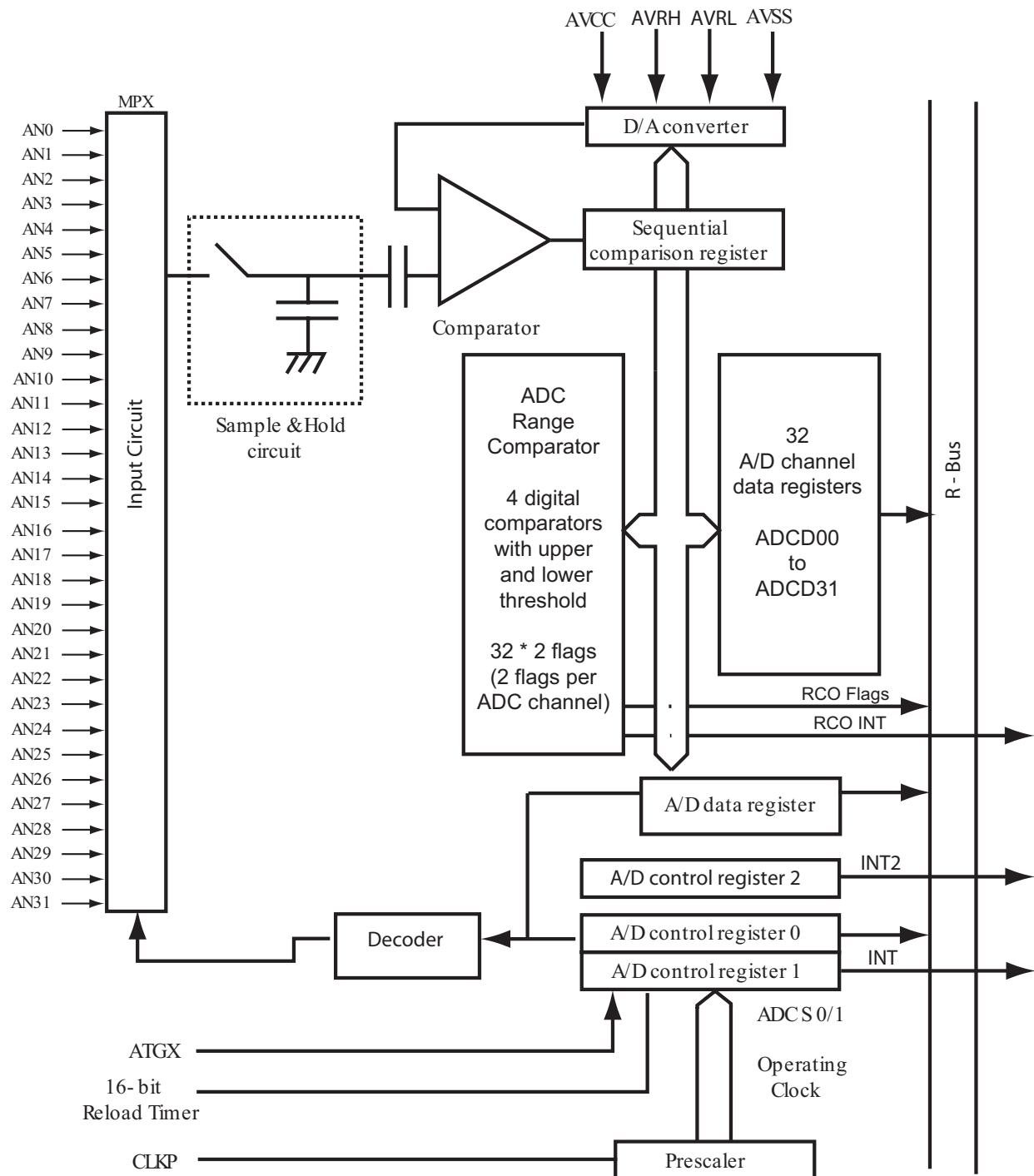


Do not set Rext over maximum sampling time (Tsamp).

$$Rext = Tsamp / (7 \cdot Cin) - Rin$$

### 3. Block Diagram of A/D Converter

The following figure shows block diagram of A/D converter.



# MB91460E Series

## 4. Registers of the A/D Converter

The A/D converter with Range Comparator has the following registers:

Address (ADC0)	Address (ADC1 *1)	x=0 or 1 for ADC0, ADC1 *1 respectively				Register
		+0	+1	+2	+3	
0001A0 <sub>H</sub>	0005E0 <sub>H</sub>	ADxERH		ADxERL		A/D channel Enable register
0001A4 <sub>H</sub>	0005E4 <sub>H</sub>	ADxCS1	ADxCS0	ADxCR1	ADxCR0	A/D Control / Status register 0 + 1, A/D Conversion Result register
0001A8 <sub>H</sub>	0005E8 <sub>H</sub>	ADxCT1	ADxCT0	ADxSCH	ADxECH	Sampling timer setting register, Start Channel setting register, End Channel setting register
0006B0 <sub>H</sub>	0006DC <sub>H</sub>	ADxCS2	-	-	-	A/D Control / Status register 2
000688 <sub>H</sub>	0006B4 <sub>H</sub>	RCOxH0	RCOxL0	RCOxH1	RCOxL1	Range Comparator 0,1 High/Low threshold registers
00068C <sub>H</sub>	0006B8 <sub>H</sub>	RCOxH2	RCOxL2	RCOxH3	RCOxL3	Range Comparator 2,3 High/Low threshold registers
000690 <sub>H</sub>	0006BC <sub>H</sub>	RCOxIRS			Range Comparator Inverted Range Select control	
000694 <sub>H</sub>	0006C0 <sub>H</sub>	RCOxOF			Range Comparator Overflow flags	
000698 <sub>H</sub>	0006C4 <sub>H</sub>	RCOxINT			Range Comparator Interrupt flags	
0006A0 <sub>H</sub>	0006CC <sub>H</sub>	ADxCC0	ADxCC1	ADxCC2	ADxCC3	Channel control for ch 0 to 7
0006A4 <sub>H</sub>	0006D0 <sub>H</sub>	ADxCC4	ADxCC5	ADxCC6	ADxCC7	Channel control for ch 8 to 16
0006A8 <sub>H</sub>	0006D4 <sub>H</sub>	ADxCC8	ADxCC9	ADxCC10	ADxCC11	Channel control for ch 16 to 23
0006AC <sub>H</sub>	0006D8 <sub>H</sub>	ADxCC12	ADxCC13	ADxCC14	ADxCC15	Channel control for ch 24 to 31
0006E0 <sub>H</sub>	000720 <sub>H</sub>	ADCxD0		ADCxD1		ADC Channel Data register, channel 0,1
0006E4 <sub>H</sub>	000724 <sub>H</sub>	ADCxD2		ADCxD3		ADC Channel Data register, channel 2,3
0006E8 <sub>H</sub>	000728 <sub>H</sub>	ADCxD4		ADCxD5		ADC Channel Data register, channel 4,5
0006EC <sub>H</sub>	00072C <sub>H</sub>	ADCxD6		ADCxD7		ADC Channel Data register, channel 6,7
0006F0 <sub>H</sub>	000730 <sub>H</sub>	ADCxD8		ADCxD9		ADC Channel Data register, channel 8,9
0006F4 <sub>H</sub>	000734 <sub>H</sub>	ADCxD10		ADCxD11		ADC Channel Data register, channel 10,11
0006F8 <sub>H</sub>	000738 <sub>H</sub>	ADCxD12		ADCxD13		ADC Channel Data register, channel 12,13
0006FC <sub>H</sub>	00073C <sub>H</sub>	ADCxD14		ADCxD15		ADC Channel Data register, channel 14,15
000700 <sub>H</sub>	000740 <sub>H</sub>	ADCxD16		ADCxD17		ADC Channel Data register, channel 16,17
000704 <sub>H</sub>	000744 <sub>H</sub>	ADCxD18		ADCxD19		ADC Channel Data register, channel 18,19
000708 <sub>H</sub>	000748 <sub>H</sub>	ADCxD20		ADCxD21		ADC Channel Data register, channel 20,21
00070C <sub>H</sub>	00074C <sub>H</sub>	ADCxD22		ADCxD23		ADC Channel Data register, channel 22,23
000710 <sub>H</sub>	000750 <sub>H</sub>	ADCxD24		ADCxD25		ADC Channel Data register, channel 24,25
000714 <sub>H</sub>	000754 <sub>H</sub>	ADCxD26		ADCxD27		ADC Channel Data register, channel 26,27
000718 <sub>H</sub>	000758 <sub>H</sub>	ADCxD28		ADCxD29		ADC Channel Data register, channel 28,29
00071C <sub>H</sub>	00075C <sub>H</sub>	ADCxD30		ADCxD31		ADC Channel Data register, channel 30,31

1. On MB91F467E, ADC1 does not exist.

## 4.1. A/D Input Enable Register (ADER)

This register enables the analog input functions of the A/D converter. On MB91FV460B, additionally the bit **ADCHE** in PORTEN register influences the enabling of analog input.

- **ADERH** : Access: Word, Half-word, Byte

31	30	29	28	27	26	25	24	Bit
<b>ADE31</b>	<b>ADE30</b>	<b>ADE29</b>	<b>ADE28</b>	<b>ADE27</b>	<b>ADE26</b>	<b>ADE25</b>	<b>ADE24</b>	
0	0	0	0	0	0	0	0	Initial value
R/W	Attribute							
23	22	21	20	19	18	17	16	Bit
<b>ADE23</b>	<b>ADE22</b>	<b>ADE21</b>	<b>ADE20</b>	<b>ADE19</b>	<b>ADE18</b>	<b>ADE17</b>	<b>ADE16</b>	
0	0	0	0	0	0	0	0	Initial value
R/W	Attribute							

- **ADERL** : Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
<b>ADE15</b>	<b>ADE14</b>	<b>ADE13</b>	<b>ADE12</b>	<b>ADE11</b>	<b>ADE10</b>	<b>ADE9</b>	<b>ADE8</b>	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute
7	6	5	4	3	2	1	0	Bit
<b>ADE7</b>	<b>ADE6</b>	<b>ADE5</b>	<b>ADE4</b>	<b>ADE3</b>	<b>ADE2</b>	<b>ADE1</b>	<b>ADE0</b>	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

### [ADE31-0]: A/D Input Enable

ADEn	PORSEN. ADCHE	Function
0 [initial]	X	Analog input of A/D channel n is disabled. The ADC will not sample/convert this channel.
1	0 [initial]	Analog input of the channel n is enabled. Additionally, the port function register (PFR,EPFR) of the corresponding port must be set. The PFR/EPFR will switch the port to input direction (output driver = HiZ) and disable the digital input lines.
	1	Analog input of the channel n is enabled. Setting the port function register(s) is not necessary. ADEn will disable the digital input lines of the ports, but it does not change the port's direction.

- Software reset (RST) clears ADEn and PORSEN.ADCHE to 0.
- Be sure to set start channel and end channel to cover all enabled channels.

# MB91460E Series

## 4.1. A/D Control Status Registers (ADCS2, ADCS1, ADCS0)

The A/D control status registers control and show the status of A/D converter. Do not overwrite ADCS0 register during A/D converting.

- **ADCS2** : Access: Byte

15	14	13	12	11	10	9	8	Bit
<b>BUSY</b>	<b>INT</b>	<b>INTE</b>	<b>PAUS</b>	-	-	<b>INT2</b>	<b>INTE2</b>	
0	0	0	0	0	0	0	0	Initial value

R      R      R      R      R0      R0      R/W      R/W      Attribute

### [bits 15:12] BUSY, INT, INTE, PAUS

These bits are a mirror of the corresponding bits in ADCS1, intended to quickly read out all status and interrupt information using only one register access. To write the bits, access them via ADCS1.

### [bits 11:10] -

These bits do not exist. Read operation returns 0.

### [bit 9] INT2 (End of Scan Flag)

The End of Scan flag is set when conversion data of the last channel is stored in ADCR, whereas the last channel is defined by ADECH register setting.

- If bit 8 (INTE2) is "1" when this bit is set, and the ADC runs in continuous conversion mode, an End of Scan interrupt request is generated or, if activation of DMA is enabled, DMA is activated.
- Only clear this bit by writing "0" when A/D conversion is halted.
- Initialized to "0" by a reset.
- If DMA is used, this bit is cleared at the end of DMA transfer.
- Read-modify-write operations read this bit as "1".

### [bit 8] INTE2 (Enable End of Scan Interrupt)

INTE2 enables the End of Scan interrupt in continuous conversion mode. In the other conversion modi, this bit has no effect.

Additionally, setting INTE2 changes the protect function of converted data (see description of ADCS1.PAUS).

INTE2	Function
0 [initial]	Disable End of Scan interrupt, ADC result protection protects the ADCR register data.
1	Enable End of Scan interrupt, ADC result protection protects the ADCD0...ADCD31 register data (in continuous conversion mode only)

- **ADCS1** : Access: Half-word, Byte

15	14	13	12	11	10	9	8	Bit
<b>BUSY</b>	<b>INT</b>	<b>INTE</b>	<b>PAUS</b>	<b>STS1</b>	<b>STS0</b>	<b>STRT</b>	<b>reserved</b>	
0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	0 R/W	Initial value Attribute

### [bit 15] BUSY (busy flag and stop)

BUSY	Function
Reading	A/D converter operation indication bit. Set on activation of A/D conversion and cleared on completion.
Writing	Writing "0" to this bit during A/D conversion forcibly terminates conversion. Use to forcibly terminate in continuous and stop modes.

- Read-modify-write instructions read the bit as "1".
- Cleared on the completion of A/D conversion in single conversion mode.
- In continuous and stop mode, the flag is not cleared until conversion is terminated by writing "0".
- Initialized to "0" by a software reset (RST).
- Do not specify forcible termination and software activation (BUSY="0" and STRT="1") at the same time.

### [bit 14] INT (End of Conversion Interrupt flag)

This bit is set when conversion data is stored in ADCR.

- If bit 5 (INTE) is "1" when this bit is set, an interrupt request is generated or, if activation of DMA is enabled, DMA is activated.
- Only clear this bit by writing "0" when A/D conversion is halted.
- Initialized to "0" by a software reset (RST).
- If DMA is used, this bit is cleared at the end of DMA transfer.

### [bit 13] INTE (End of Conversion Interrupt enable)

This bit is enables or disables the conversion completion interrupt.

INTE	Function
0	Disable interrupt [Initial value]
1	Enable interrupt

- Cleared by a software reset (RST).

# MB91460E Series

## [bit 12] PAUS (A/D converter pause)

This bit is set when A/D conversion temporarily halts.

The A/D converter has one register to store the conversion result (ADCR) and additionally 32 ADC channel data registers. If a conversion is finished and the data of the previous conversion has not been read out before, previous data would be overwritten.

To avoid this problem, the next conversion data is not stored in the data registers until the previous value has been read out (e.g. by DMA). A/D conversion halts during this time. A/D conversion resumes when the ADC interrupt flag ADCR1.INT is cleared.

The register protection function depends on the conversion mode and the setting of ADCR2.INTE2:

Mode	INTE2	Function
Single, Stop	X	Protect ADCR (the common result register)
Continous	0	Protect ADCR (the common result register)
	1	Protect ADCCD0...ADCCD31 (the dedicated channel data registers)

- In continous mode with INTE2==1, PAUS is set when data of the **start channel** (set by ADSCH) is ready for writing to the registers, but IRQ2 (End of Scan interrupt) is active.
- In the other modes or if INTE2==0, PAUS is set when data of any channel is ready for writing to the registers, but IRQ (End of Conversion) is active.
- PAUS is cleared by writing "0" or by a reset. (Not cleared at the end of DMA transfer.) However when waiting condition of DMA transfer, this bit cannot be cleared.
- Regarding protect function of converted data, see Section "[6. Operation of A/D Converter](#)".

## [bit 11, 10] STS1, STS0 (Start source select)

These bits select the A/D activation source.

STS1	STS0	Function
0	0	Software activation [Initial value]
0	1	External trigger pin activation and software activation
1	0	Timer activation and software activation
1	1	External trigger pin activation, timer activation and software activation

- These bits are initialized "00" by software reset (RST).
- In multiple-activation modes, the first activation to occur starts A/D conversion.
- The activation source changes immediately on writing to the register. Therefore care is required when switching activation mode during A/D operation.
- The A/D converter detects falling edges on the external trigger pin. When external trigger level is "L" and if these bits are changed to external trigger activation mode, A/D converting may starts.
- Selecting the timer selects the 16-bit reload timer 7.

## [bit 9] STRT (Start)

Writing "1" to this bit starts A/D conversion (software activation).

- Write "1" again to restart conversion.
- Initialized to "0" by a software reset (RST).
- In continuous and stop mode, restarting is not occurred. Check BUSY bit before writing "1". (Activate conversion after clearing.)
- Do not specify forcible termination and software activation (BUSY="0" and STRT="1") at the same time.

## [bit 8] reserved bit

Always write "0" to this bit.

- **ADCS0** : Access: Half-word, Byte. Read-modify-write access is not allowed

7	6	5	4	3	2	1	0	Bit
<b>MD1</b>	<b>MD0</b>	<b>S10</b>	<b>ACH4</b>	<b>ACH3</b>	<b>ACH2</b>	<b>ACH1</b>	<b>ACH0 / ACHMD</b>	
0	0	0	0	0	0	0	0	Initial value

R/W      R/W      R/W      R      R      R      R      R, W \*1      Attribute

1. ACHMD is a new, control bit, see "[bit 0] ACHMD (ACH register mode, write-only)" on page 36.

## [bit 7, 6] MD1, MD0 (A/D converter mode set)

These bits the operation mode.

MD1	MD0	Operating mode
0	0	Single mode 1 (Reactivation during A/D conversion is allowed)
0	1	Single mode 2 (Reactivation during A/D conversion is not allowed)
1	0	Continuous mode (Reactivation during A/D conversion is not allowed)
1	1	Stop mode (Reactivation during A/D conversion is not allowed)

- Single mode: A/D conversion is continuously performed from the selected start channel (ADSCH) to the selected end channel (ADECH). The conversion stops once it has been done for all these channels.
- Continuous mode: A/D conversion is repeatedly performed from the selected start channel (ADSCH) to the selected end channel (ADECH) in a row.
- Stop mode: A/D conversion is performed from the selected start channel (ADSCH) to the selected end channel (ADECH), followed by a pause after each channel. The conversion is resumed upon activation.

When A/D conversion is started in continuous mode or stop mode, conversion operation continued until stopped by the BUSY bit.

Conversion is stopped by writing "0" to the BUSY bit.

On activation after forcibly stopping, conversion starts from the start channel, selected by ADSCH register.

Reactivation during A/D conversion is disabled for any of the timer, external trigger and software start sources in single mode 2, continuous and stop mode.

# MB91460E Series

## [bit 5] S10

This bit defines resolution of A/D conversion. If this bit set "0", the resolution is 10-bit. In the other case, resolution is 8-bit and the conversion result is stored to ADCR0 and in the lower 8 bits of the dedicated ADC result registers.

- Initialized to "0" by a reset.

## [bit 4 to 0] ACH4-0 (Analog convert select channel, read-only)

These bits show the number of the currently or previously converted analog channel, depending on bit ACHMD (see below).

ACH4	ACH3	ACH2	ACH1	ACH0	Converted channel
0	0	0	0	0	AN0
0	0	0	0	1	AN1
...					...
1	1	1	1	0	AN30
1	1	1	1	1	AN31

- Writing these bits has no effect (bit 0 is writeable with special function ADCHMD).
- Initialized to "0000" by software reset (RST).

## [bit 0] ACHMD (ACH register mode, write-only)

For reading out the ACH4-0 register bits (see below), there is a *direct* mode and a *latched* mode.

In direct mode, ACH4-0 shows the number of the ADC channel which is *currently in conversion*, e.g. the internal conversion channel pointer. This pointer is incremented immediately after a conversion is finished. On MB91460 series devices having the old ADC macro, ACH4-0 always show this mode.

In the new latched mode, ACH4-0 shows the number of the ADC channel whose conversion was *finished previously*. After a conversion is finished, the conversion channel pointer is latched and the latched data can be read in this mode. At the end of the next conversion, the latch is overwritten if no PAUSE condition exists.

ACHMD	Function
0	Direct ACH register mode [Initial value]
1	Latched ACH register mode

- ACHMD is a write-only bit.
- Read- or read-modify-write access returns the value of bit ACH0, that's why read-modify-write access is not allowed.
- Initial value is 0.

## 4.2. Common Data Register (ADCR1, ADCR0)

These registers store the conversion results of the A/D converter. ADCR0 stores lower 8-bit. ADCR1 stores upper 2-bit. The register values are updated at the completion of each conversion. The registers normally store the results of the previous conversion.

- **ADCR1** : Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
-	-	-	-	-	-	<b>D9</b>	<b>D8</b>	
0	0	0	0	0	0	X	X	Initial value
R0, W0	R	R	Attribute					

- **ADCR0** : Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	
X	X	X	X	X	X	X	X	Initial value
R	R	R	R	R	R	R	R	Attribute

- Bit 15 to 10 of ADCR1 are read as "0".
- The A/D converter has a conversion data protection function. See the "Operation" section for further information.

## 4.3. Dedicated A/D Channel Data Register (ADCD0 to ADCD31)

There are 32 ADC result data registers, one per channel. The registers are written by hardware at the end of conversion of the attached channel. ADCD0 is attached to channel 0, ADCD31 is attached to channel 31.

- **ADCD0 ... ADCD31** : Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
-	-	-	-	-	-	<b>D9</b>	<b>D8</b>	
0	0	0	0	0	0	X	X	Initial value
R0	R0	R0	R0	R0	R0	R	R	Attribute
7	6	5	4	3	2	1	0	Bit
<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	
X	X	X	X	X	X	X	X	Initial value
R	R	R	R	R	R	R	R	Attribute

- Bit 15 to 10 of the ADCD registers are read as "0".
- The A/D converter has a conversion data protection function. In continuous conversion mode, the protection function can be changed to protect the A/D Channel Data registers rather than the A/D Data Register (ADCR1). See section "6.6. Protection of the ADC Channel Data Registers" for further information.

## 4.4. Sampling Timer Setting Register (ADCT)

ADCT register controls the sampling time and comparison time of analog input. This register sets A/D conversion time. Do not update value of this register during A/D conversion operation.

- **ADCT1:** Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
<b>CT5</b>	<b>CT4</b>	<b>CT3</b>	<b>CT2</b>	<b>CT1</b>	<b>CT0</b>	<b>ST9</b>	<b>ST8</b>	
0	0	0	1	0	0	0	0	Initial value

R/W      R/W      R/W      R/W      R/W      R/W      R/W      R/W      Attribute

- **ADCT0:** Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
<b>ST7</b>	<b>ST6</b>	<b>ST5</b>	<b>ST4</b>	<b>ST3</b>	<b>ST2</b>	<b>ST1</b>	<b>ST0</b>	
0	0	1	0	1	1	0	0	Initial value

R/W      R/W      R/W      R/W      R/W      R/W      R/W      R/W      Attribute

### [bit 15 to 10] CT5-0 (A/D comparison time set)

These bits specify clock division of comparison time.

- Setting "000001" means one division (=CLKP).
- Do not set these bits "000000".
- Initialized these bits to "000100" by software reset (RST).
- Comparison time = CT value \* CLKP cycle \* 10 + (4 \* CLKP)
- Do not set comparison time over 500 us.

### [bit 9 to 0] ST9-0 (Analog input sampling time set)

These bits specify sampling time of analog input.

- Initialized these bits to "0000101100" by software reset (RST).
- Sampling time = ST value \* CLKP cycle
- Do not set sampling time below 1.2 us when AVCC is below 4.5 V.

Necessary sampling time and ST value are calculated by following.

- Necessary sampling time (Tsamp) =  $(R_{ext} + R_{in}) * C_{in} * 7$
- ST9 to ST0 = Tsamp / CLKP cycle

ST has to be set that sampling time is over Tsamp.

Example: CLKP = 32MHz, AVCC >= 4.5V, Rext = 200K

$$Tsamp = (200 * 103 + 2.52 * 103) * 10.7 * 10-12 * 7 = 15.17 \text{ [us]}$$

$$ST = 15.17-6 / 31.25-9 = 485.44$$

ST has to be set over 486<sub>D</sub> (111100110<sub>B</sub>).

Tsamp is decided by Rext. Thus conversion time should be considered together with Rext.

## 4.5. A/D Channel Setting Register (ADSCH, ADECH)

These registers specify the channels for the A/D converter to convert. Do not update these registers while the A/D converting is operating.

- **ADSCH**: Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
-	-	-	<b>ANS4</b>	<b>ANS3</b>	<b>ANS2</b>	<b>ANS1</b>	<b>ANS0</b>	
-	-	-	0	0	0	0	0	Initial value

RX, W0    RX, W0    RX, W0    R/W    R/W    R/W    R/W    R/W    Attribute

- **ADECH** : Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
-	-	-	<b>ANE4</b>	<b>ANE3</b>	<b>ANE2</b>	<b>ANE1</b>	<b>ANE0</b>	
-	-	-	0	0	0	0	0	Initial value

RX, W0    RX, W0    RX, W0    R/W    R/W    R/W    R/W    R/W    Attribute

These bits set the start and end channel for A/D converter.

- Setting of ANE4 to ANE0 the same channel as in ANS4 to ANS0 specifies conversion for that channel only. (Single conversion)
- In continuous or stop mode, conversion is performed up to the channel specified by ANE4 to ANE0. Conversion then starts again from the start channel specified by ANS4 to ANS0.
- If ANS > ANE, conversion starts with the channel specified by ANS, continuous up to channel 31, starts again from channel 0, and ends with the channel specified by ANE.
- Initialized to ANS="00000", ANE="00000" by a software reset (RST).

Example: Channel Setting ANS=30ch, ANE=3ch, single conversion mode

Operation : Conversion channel 30ch -> 31ch -> 0ch -> 1ch -> 2ch -> 3ch end

[bit 12 to 8] ANS4-0 (Analog start channel set)

[bit 4 to 0] ANE4-0 (Analog end channel set)

ANS4 ANE4	ANS3 ANE3	ANS2 ANE2	ANS1 ANE1	ANS0 ANE0	Start / End Channel
0	0	0	0	0	AN0
0	0	0	0	1	AN1
0	0	0	1	0	AN2
0	0	0	1	1	AN3
...					...
1	1	1	0	1	AN29
1	1	1	1	0	AN30
1	1	1	1	1	AN31

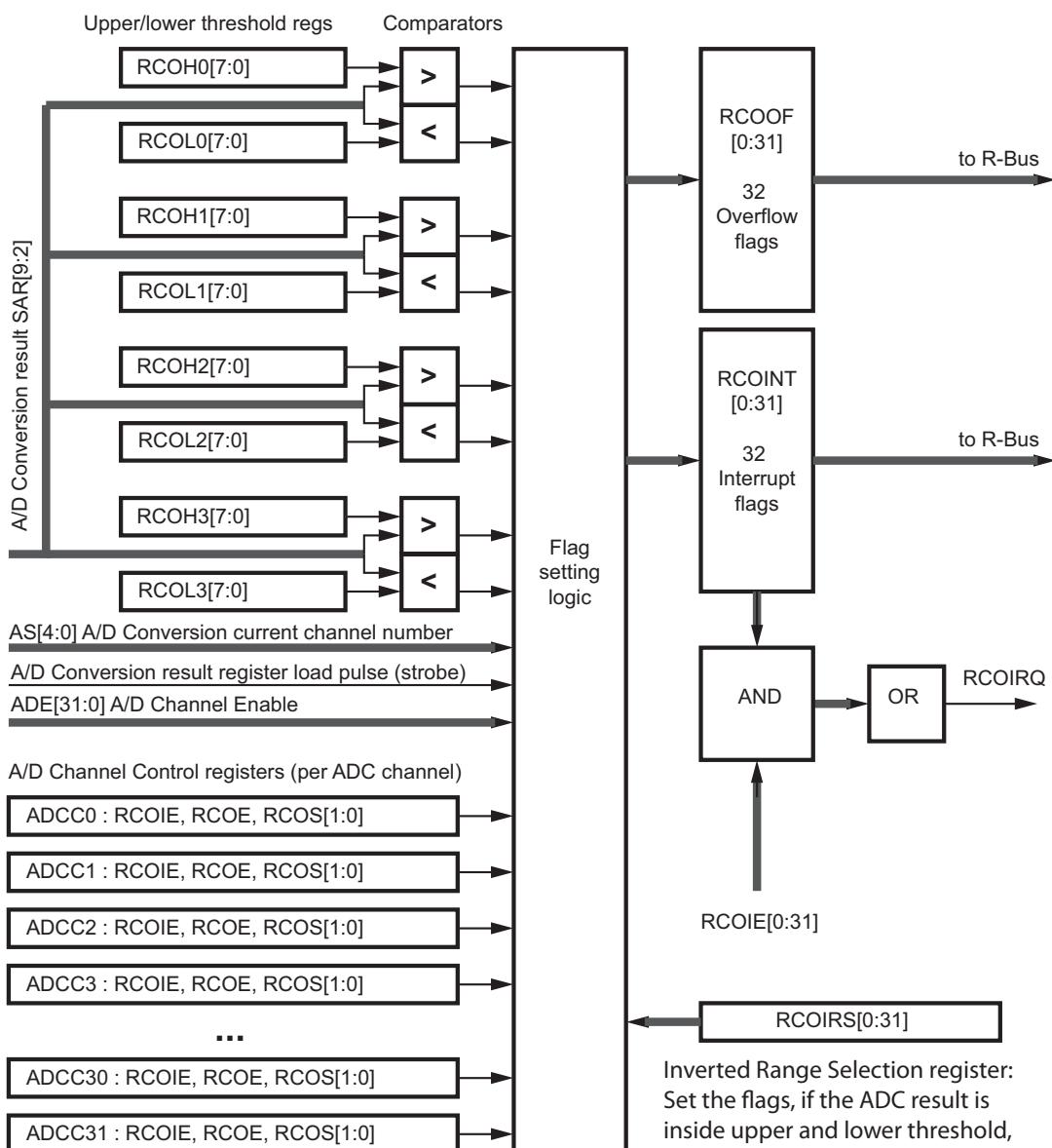
## 5. Range Comparator

### 5.1. Range Comparator Structure

The Range Comparator has 4 comparsion groups with an upper and a lower threshold register each. The 32 ADC channels can be enabled for range comparsion and assigned to one of the 4 comparators individually. If enabled, the comparsion will set up to 2 flags for this ADC channel:

- An interrupt flag RCOINT, signalling that the ADC result is outside the range or, by “inverted” configuration, inside the range.
- An overflow flag RCOOF, showing that the range violation was an overflow and no underflow.

Furthermore, each ADC channel can be enabled to send an interrupt request to the CPU, if the RCOINT flag is set.



RCOS[1:0]: Select one of the 4 comparators for this channel

RCOE : Enable Comparsion for this ADC channel

RCOIE: Enable Comparsion Interrupt for this ADC channel

## 5.2. Range Comparator Registers

The Range Comparator (RCO) has the following registers:

- RCOHx[7:0] : Upper threshold register, one register per comparator block (x = 0...3)
- RCOLx[7:0] : Lower threshold register, one register per comparator block (x = 0...3)
- ADCCm[7:0] : ADC channel control, one register per 2 ADC channels (m = 0...15)
- RCOIRS[0:31] : RCO Inverted Range Selection, one bit per ADC channel
- RCOOF[0:31] : RCO Overflow Flags, one bit per ADC channel, read-only
- RCOINT[0:31] : RCO Interrupt Flags, one bit per ADC channel

### 5.2.1. Range Comparator Threshold registers (RCOH0/L0 to RCOH3/L3)

- RCOH0-3 : Higher threshold, access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
RCOH7	RCOH6	RCOH5	RCOH4	RCOH3	RCOH2	RCOH1	RCOH0	
1 R/W	Initial value Attribute							

#### [bit 7:0] RCOH[7:0] (Range Comparator High threshold)

The RCOH bits define the higher comparision threshold of the Range Comparator channel.

The upper Range Comparator compares that the upper 8 bits of the ADC conversion result are higher then RCOH[7:0]

- RCOL0-3 : Lower threshold, access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
RCOL7	RCOL6	RCOL5	RCOL4	RCOL3	RCOL2	RCOL1	RCOL0	
0 R/W	Initial value Attribute							

#### [bit 7:0] RCOL[7:0] (Range Comparator Low threshold)

The RCOL bits define the lower comparision threshold of the Range Comparator channel.

The lower Range Comparator compares that the upper 8 bits of the ADC conversion result are lower then RCOL[7:0]

# MB91460E Series

## 5.2.2. A/D Converter Channel Control registers (ADCC0 to ADCC15)

The A/D channel control registers serve 2 ADC channels per register and control the range comparision for these channels.

ADCC0 register controls A/D channels 0 + 1,

ADCC1 register controls A/D channels 2 + 3,

...

ADCC15 register controls A/D channels 30 + 31

- **ADCC0-15:** Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
<b>RCOIE1</b>	<b>RCOE1</b>	<b>RCOS11</b>	<b>RCOS10</b>	<b>RCOIE0</b>	<b>RCOE0</b>	<b>RCOS01</b>	<b>RCOS00</b>	
0	0	0	0	0	0	0	0	Initial value

R/W      R/W      R/W      R/W      R/W      R/W      R/W      R/W      Attribute

Bits 7:4 control A/D channels 1,3,5,7,...31      Bits 3:0 control A/D channels 0,2,4,6,...,30

### [bit 7,3] RCOIE1, RCOIE0 (Range Comparator Interrupt enable)

The RCOIE bits enable the Range Comparator interrupt for the corresponding ADC channel.

RCOIE	Function
0	RCO interrupt for this ADC channel is disabled [default]
1	RCO interrupt for this ADC channel is enabled

### [bit 6,2] RCOE1, RCOE0 (Range Comparator operation enable)

The RCOE bits enable the Range Comparision for the corresponding ADC channel:

RCOE	Function
0	RCO disabled, RCO flags for this ADC channel will not be set [default]
1	RCO enabled for this ADC channel

### [bits 5:4,1:0] RCOS1[1:0], RCOS0[1:0] (converter channel select)

These bits select the A/D converter channel to be assigned to the Range Comparator channel:

RCOS[1:0]	Function
00	Select range comparator channel 0 for this ADC channel [default]
01	Select range comparator channel 1 for this ADC channel
10	Select range comparator channel 2 for this ADC channel
11	Select range comparator channel 3 for this ADC channel

### 5.2.3. Inverted Range Selection register

The RCOIRS register controls that the comparision should check for “out of range” or “inside range”.

The 32 bits of RCOIRS is organized “per ADC channel”. ADC channel 0 is located on the MSB of the register and ADC channel 31 is on the LSB.

- **RCOIRS** : Access: Word, Half-word, Byte

31	30	29	28	27	26	259	24	Bit
<b>RCOIRS0</b>	<b>RCOIRS1</b>	<b>RCOIRS2</b>	<b>RCOIRS3</b>	<b>RCOIRS4</b>	<b>RCOIRS5</b>	<b>RCOIRS6</b>	<b>RCOIRS7</b>	
0	0	0	0	0	0	0	0	Initial value
R/W	Attribute							
23	22	21	20	19	18	17	16	Bit
<b>RCOIRS8</b>	<b>RCOIRS9</b>	<b>RCOIRS10</b>	<b>RCOIRS11</b>	<b>RCOIRS12</b>	<b>RCOIRS13</b>	<b>RCOIRS14</b>	<b>RCOIRS15</b>	
0	0	0	0	0	0	0	0	Initial value
R/W	Attribute							
15	14	13	12	11	10	9	8	Bit
<b>RCOIRS16</b>	<b>RCOIRS17</b>	<b>RCOIRS18</b>	<b>RCOIRS19</b>	<b>RCOIRS20</b>	<b>RCOIRS21</b>	<b>RCOIRS22</b>	<b>RCOIRS23</b>	
0	0	0	0	0	0	0	0	Initial value
R/W	Attribute							
7	6	5	4	3	2	1	0	Bit
<b>RCOIRS24</b>	<b>RCOIRS25</b>	<b>RCOIRS26</b>	<b>RCOIRS27</b>	<b>RCOIRS28</b>	<b>RCOIRS29</b>	<b>RCOIRS30</b>	<b>RCOIRS31</b>	
0	0	0	0	0	0	0	0	Initial value
R/W	Attribute							

Note that bit[31] is assigned to ADC channel 0, bit[30] is assigned to ADC channel one and so on.

#### [bits 31:0] RCOIRS[0:31] (Inverted Range Select)

The RCOIRS bits control how the Range Comparator result flags are set.

- If the RCOIRS[n] is 0, the flags are set when the ADC result is above the upper threshold OR below the lower threshold. That is called “**out of range**” mode.
- If the RCOIRS[n] is 1, the flags are set when the ADC result is below or equal the upper threshold AND above or equal the lower threshold. That is called “**inside range**” mode.

RCOIRS n	Function
0	Range comparision for this ADC channel checks for “out of range” (default)
1	Range comparision for this ADC channel checks for “inside range”

## 5.2.4. Range Comparator Result Flags

The result of range comparision is stored in 2 flag registers:

- RCOINT[0:31]: Range comparision interrupt flags
- RCOOF[0:31]: Range comparision overflow flags

The Range Comparator Result flags are organized “per ADC channel”. There are 32 Range Comparator overflow flags and 32 interrupt flags. In case of a RCO interrupt, all interrupt flags can be read out by one 32-bit read operation and analyzed using the Bit Search Unit. The Bit Search Unit will return the number of the interrupting channel. Since bit search works from MSB to LSB (from left to right), ADC channel 0 is located on the MSB of the registers and ADC channel 31 is on LSB.

- **RCOINT[0:31]** : Access: Word, Half-word, Byte

31	30	29	28	27	26	259	24	Bit
<b>RCOINT0</b>	<b>RCOINT1</b>	<b>RCOINT2</b>	<b>RCOINT3</b>	<b>RCOINT4</b>	<b>RCOINT5</b>	<b>RCOINT6</b>	<b>RCOINT7</b>	
0	0	0	0	0	0	0	0	Initial value
R/W0	Attribute							
23	22	21	20	19	18	17	16	Bit
<b>RCOINT8</b>	<b>RCOINT9</b>	<b>RCOINT10</b>	<b>RCOINT11</b>	<b>RCOINT12</b>	<b>RCOINT13</b>	<b>RCOINT14</b>	<b>RCOINT15</b>	
0	0	0	0	0	0	0	0	Initial value
R/W0	Attribute							
15	14	13	12	11	10	9	8	Bit
<b>RCOINT16</b>	<b>RCOINT17</b>	<b>RCOINT18</b>	<b>RCOINT19</b>	<b>RCOINT20</b>	<b>RCOINT21</b>	<b>RCOINT22</b>	<b>RCOINT23</b>	
0	0	0	0	0	0	0	0	Initial value
R/W0	Attribute							
7	6	5	4	3	2	1	0	Bit
<b>RCOINT24</b>	<b>RCOINT25</b>	<b>RCOINT26</b>	<b>RCOINT27</b>	<b>RCOINT28</b>	<b>RCOINT29</b>	<b>RCOINT30</b>	<b>RCOINT31</b>	
0	0	0	0	0	0	0	0	Initial value
R/W0	Attribute							

Note that bit[31] is assigned to ADC channel 0, bit[30] is assigned to ADC channel one and so on.

### [bits 31:0] RCOINT[0:31] (Range Comparator Interrupt flags)

The RCOINT flags show that a “out of range” or “inside range” condition has been found on the ADC channel.

The bits are set under the following condition:

- the ADC channel is enabled ADER.ADE[i] is set and
- the range comparision for this channel is enabledADCCn.RCOE[i] is set and
- the conversion of the ADC channel is just finished and
- an interrupt condition was found (see the table on next page).
- The bits are cleared by writing 0 or by software reset (RST). Writing 1 has no effect.
- Read-modify-write operations read 1.

The interrupt condition depends on the comparision results and the RCOIRS setting for this channel:

Mode	RCOIRS	Upper threshold comparator	Lower threshold comparator	Interrupt condition
out of range	0	1	x	INT condition: above range, RCOOF is set
		0	0	-
		x	1	INT condition: below range, RCOOF is cleared
inside range	1	1	x	-
		0	0	INT condition: inside range
		x	1	-

Note: The upper threshold comparator returns 1 if the upper 8 bits of the ADC result are greater than the threshold value in RCOH[7:0].

The lower threshold comparator returns 1 if the upper 8 bits of the ADC result are smaller than the threshold value in RCOL[7:0].

- **RCOOF[0:31]** : Access: Read-only, Word, Half-word, Byte

31	30	29	28	27	26	259	24	Bit
<b>RCOOF0</b>	<b>RCOOF1</b>	<b>RCOOF2</b>	<b>RCOOF3</b>	<b>RCOOF4</b>	<b>RCOOF5</b>	<b>RCOOF6</b>	<b>RCOOF7</b>	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute
23	22	21	20	19	18	17	16	Bit
<b>RCOOF8</b>	<b>RCOOF9</b>	<b>RCOOF10</b>	<b>RCOOF11</b>	<b>RCOOF12</b>	<b>RCOOF13</b>	<b>RCOOF14</b>	<b>RCOOF15</b>	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute
15	14	13	12	11	10	9	8	Bit
<b>RCOOF16</b>	<b>RCOOF17</b>	<b>RCOOF18</b>	<b>RCOOF19</b>	<b>RCOOF20</b>	<b>RCOOF21</b>	<b>RCOOF22</b>	<b>RCOOF23</b>	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute
7	6	5	4	3	2	1	0	Bit
<b>RCOOF24</b>	<b>RCOOF25</b>	<b>RCOOF26</b>	<b>RCOOF27</b>	<b>RCOOF28</b>	<b>RCOOF29</b>	<b>RCOOF30</b>	<b>RCOOF31</b>	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute

Note that bit[31] is assigned to ADC channel 0, bit[30] is assigned to ADC channel one and so on.

#### [bits 31:0] RCOOF[0:31] (Range Comparator Overflow flag)

The RCOOF read-only flags store the output signal of the upper threshold comparator at the time when an interrupt condition (see above) appeared and the corresponding RCOINT flag was **not** set. So the RCOOF flags indicate the upper comparator state when the RCOINT flag had the last rising edge.

The RCOOF flag for a ADC channel is loaded with the upper threshold comparator output signal under the following condition:

- the corresponding RCOINT flag is not yet setand
- the corresponding RCOINT flag has a set condition in this cycle.

The flags are initialized by software reset (RST).

RCOOFn	Function
0	The output of the upper threshold comparator was 0 [default]
1	The output of the upper threshold comparator was 1

### 5.3. Range Comparator Interrupt request

The Range Comparator has one interrupt output line RCOIRQ. The interrupt output line becomes active if at least one of the Range Comparator interrupt flags RCOINT[31:0] is set and the corrsponding interrupt enable bit in the ADCC registers is set..

It is not possible to activate a DMA request from the range comparator interrupts.

## 6. Operation of A/D Converter

The A/D converter operates using the successive approximation method with 10-bit or 8-bit resolution. There is one 16-bit register provided to store conversion results (ADCR), which is updated each time conversion completes. Additionally, there is one ADC Channel Data register per channel (ADCD0...31), which is updated each time the assigned channel is converted. The Channel Data registers especially improve the continuous conversion mode.

It is recommended to use the DMA service. The following describes the operation modes.

### 6.1. Single Mode

In single conversion mode, the analog input signals selected by the ANS bits and ANE bits are converted in order until the completion of conversion on the end channel determined by the ANE bits. A/D conversion then ends. If the start channel and end channel are the same (ANS=ANE), only a single channel conversion is performed.

Examples:

- ANS=00000b, ANE=00011b  
Start -> AN0 -> AN1 -> AN2 -> AN3 -> End
- ANS=00010b, ANE=00010b  
Start -> AN2 -> End

### 6.2. Continuous Mode

In continuous mode the analog input signals selected by the ANS bits and ANE bits are converted in order until the completion of conversion on the end channel determined by the ANE bits, then the converter returns to the ANS channel for analog input and repeats the process continuously. When the start and end channels are the same (ANS=ANE), conversion is performed continuously for that channel.

Examples:

- ANS=00000b, ANE=00011b  
Start -> AN0 -> AN1 -> AN2 -> AN3 -> AN0 ... -> repeat
- ANS=00010b, ANE=00010b  
Start -> AN2 -> AN2 -> AN2 ... -> repeat

In continuous mode, conversion is repeated until '0' is written to the BUSY bit. (Writing '0' to the BUSY bit forcibly stops the conversion operation.) Note that forcibly terminating operation halts the current conversion during mid-conversion. (If operation is forcibly terminated, the value in the conversion register is the result of the most recently completed conversion.)

### 6.3. Stop Mode

In stop mode the analog input signal selected by the ANS bits and ANE bits are converted in order, but conversion operation pauses after each channel. The pause is released by applying another start signal.

At the completion of conversion on the end channel determined by the ANE bits, the converter returns to the ANS channel for analog input signal and repeats the conversion process continuously. When the start and end channel are the same (ANS=ANE), only a signal channel conversion is performed.

Examples:

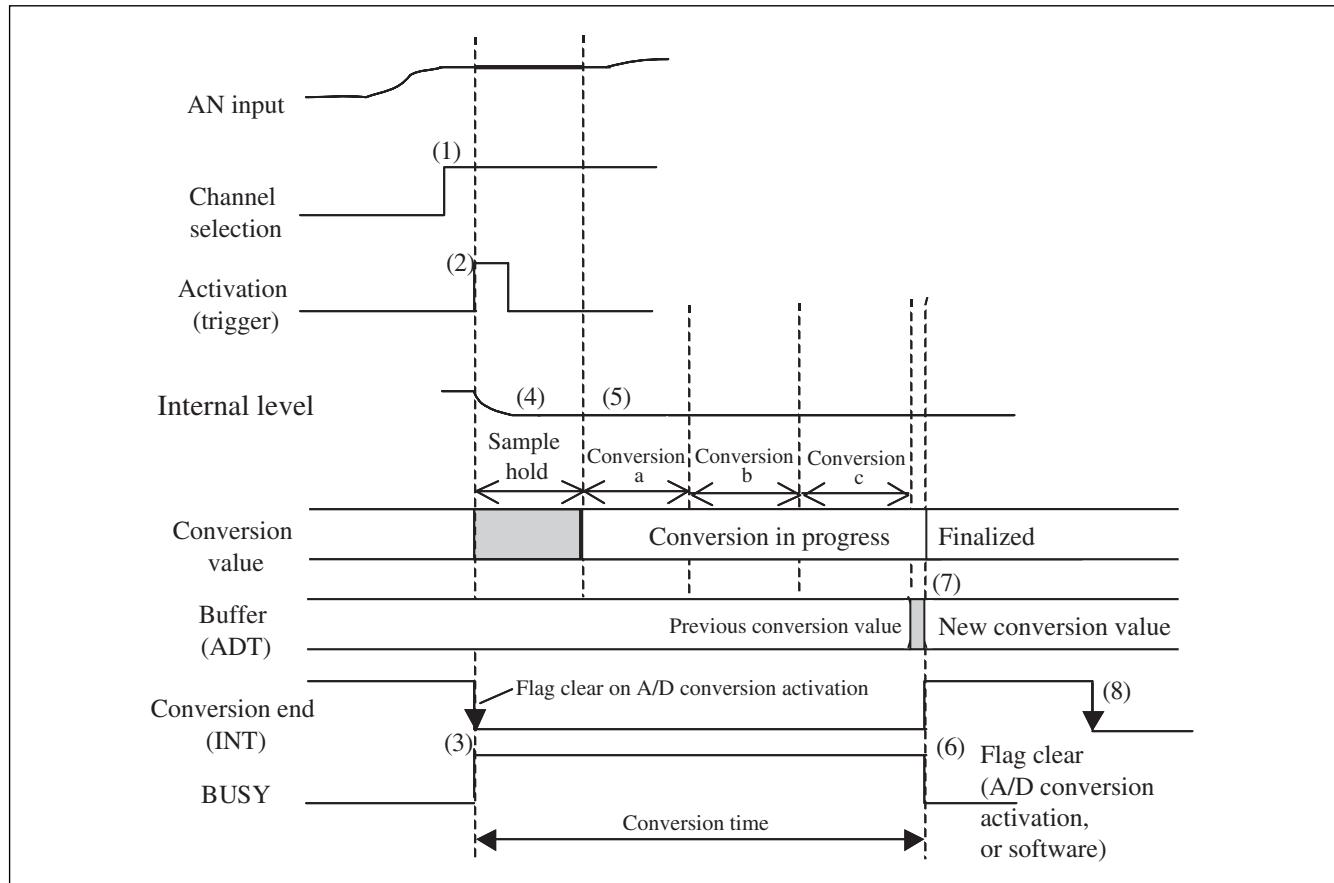
- ANS=00000b, ANE=00011b  
Start -> AN0 -> stop -> start -> AN1 -> stop -> start -> AN2 -> stop -> start -> AN3 -> stop -> start -> AN0 ... -> repeat
- ANS=00010b, ANE=00010b  
Start -> AN2 -> stop -> start -> AN2 -> stop -> start -> AN2 ... -> repeat

# MB91460E Series

In stop mode the startup source is the source determined by the STS1, STS0 bits. This mode enables synchronization of the conversion start signal.

## 6.4. Single-shot Conversion

The following figure shows the operation of A/D converter in Single-shot conversion mode



(1) Channel selection

(2) A/D conversion activation (Trigger input: Software trigger/Reload timer/External trigger)

(3) INT flag clear, BUSY flag set

(4) Sample hold

(5) Conversion (Conversion a + Conversion b + Conversion c)

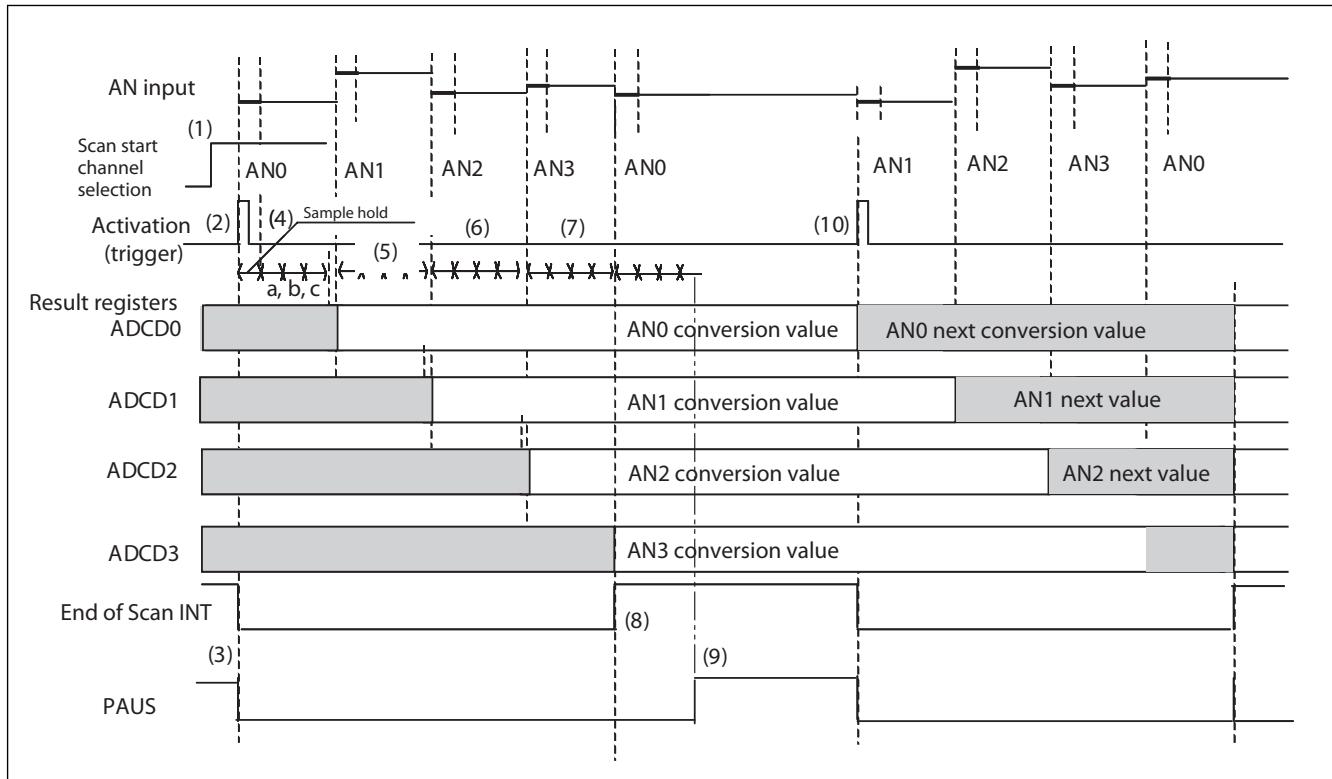
(6) Conversion end, INT flag set, BUSY flag clear

(7) Buffers the conversion value. Buffered data storage

(8) Software-based INT flag clear

## 6.5. Scan Conversion

The following figure shows the operation of A/D converter in Scan conversion mode



- (1) Activation channel selection
- (2) A/D activation (Trigger: Software trigger/Reload timer/External trigger)
- (3) INT flag clear, PAUS flag clear
- (4) AN0 conversion
  - a. Sample hold, conversion (conversion a + conversion b + conversion c)
  - b. Conversion end
  - c. Buffers the conversion value.
- (5) AN1 conversion
- (6) AN2 conversion
- (7) AN3 conversion
- (8) INT2 (End of Scan) flag is set, AN0 conversion starts
- (9) Because INT2 has not been cleared yet, the ADC protects the result register of AN0 against overwriting and enters PAUSE state.
- (10) INT2 flag cleared by DMA or by software, the ADC stores the result of AN0 and continues sampling AN1.

## 6.6. Protection of the ADC Channel Data Registers

There are 32 ADC result data registers, one register per channel. The registers are written by hardware at the end of conversion of the attached channel. ADCCD0 is attached to channel 0, ADCCD31 is attached to channel 31.

The CPU can read the data registers any time.

# MB91460E Series

If a conversion is finished and the data of the previous conversion has not been read out before, previous data would be overwritten. To avoid this problem, the next conversion data is not stored in the data registers until the previous value has been read out (e.g. by DMA). A/D conversion halts during this time and the PAUS flag is set. A/D conversion restarts when the ADC interrupt flag ADCR1.INT is cleared.

The register protection function depends on the conversion mode and the setting of ADCR2.INTE2:

Mode	INTE2	Function
Single, Stop	X	Protection of ADCR
Continous	0	Protection of ADCR
	1	Protection of ADCCD0...ADCCD31

## 6.6.1. Protection of ADCCD0...31

In continous mode with INTE2==1, PAUS is set when data of the **start channel (set by ADSCH)** is ready for writing to the registers, but IRQ2 (End of Scan interrupt) is already active.

Example: Start channel =4, end channel=7, continous mode, ADCS1.INTE=0, ADCS2.INTE2=1

Start by CPU --> convert channel 4 + safe data to ADCCD4,  
convert channel 5 + safe data to ADCCD5,  
convert channel 6 + safe data to ADCCD6,  
convert channel 7 + safe data to ADCCD7 ---> End of Scan interrupt (IRQ2),  
convert channel 4 + set PAUS (protect ADCCD4...7).

After the CPU or DMA have read the data registers and cleared IRQ2, the scan conversion continues.

## 6.6.2. Protection of ADCR

In the other modes or if INTE2==0, PAUS is set when data of any channel is ready for writing to the registers, but IRQ (End of Conversion) is active. Because in this mode the protection function is active after each single conversion, the ADCR register is protected.

## 7. ADC Interrupt Generation and DMA Access

There are 2 ADC interrupt sources: End of Conversion and End of Scan.

### 7.1. End of Conversion

The End of Conversion (EoC) interrupt is enabled by ADCS1.INTE bit and is compatible to the A/D convertes in old devices of MB91460 series. If EoC is enabled, it appears after any conversion cycle. It is recommended to use DMA transfer to read out the data from ADCR.

### 7.2. End of Scan

The End of Scan (EoS) interrupt is enabled by ADCS2.INTE2 bit. If EoS is enabled, it appears after the conversion of the end channel, which is defined by the setting of ADECH register.

If the End of Conversion interrupt is enabled in parallel, both interrupt bits are set. In this case it is recommended that the interrupt routine reads out ADCS2 register (containing mirrored bits of ADCS1[7:4]) to check where the interrupt comes from.

### 7.3. DMA Transfer

DMA transfer can be triggered by End of Conversion interrupt or by End of Scan interrupt. The interrupts are assigned to separate DMA resource numbers (please refer to the Interrupt Vector Table).

The automatic interrupt clear after DMA transfer works for End of Conversion and for End of Scan separately.

## ■ HARDWARE WATCHDOG (Extension)

This chapter describes a new feature of the Hardware Watchdog. For reference, please refer to chapter 21 Hardware Watchdog in the MB91460 series hardware manual.

### 1. Enabling the Hardware Watchdog in SLEEP and STOP State

The Hardware Watchdog can now be enabled in SLEEP and STOP state by software. On old devices, the watchdog is cleared in SLEEP and STOP and restarts counting at the transition to RUN mode.

Additionally, the restriction of MB91V460A about the settings ED1,ED0 = 01,10,11 has been removed.

#### 1.1. HWWDE: Hardware watchdog timer duration register

The Hardware Watchdog Timer Duration register changes like following:

7	6	5	4	3	2	1	0	Bit
-	-	-	STP_RUN	-	-	ED1	ED0	
X	X	X	0	X	X	0	0	Initial value

RX, W0    RX, W0    RX, W0    R, W1    RX, W0    RX, W0    R, W    R, W    Attribute

- Bit7-5: Reserved bits. Always write 0 to these bits.
- Bit4: STP\_RUN (Run in SLEEP/STOP mode):
  - STP\_RUN = 1 enables that the Hardware Watchdog continues running in SLEEP and STOP mode. The RC Oscillator will continue operation in SLEEP and STOP too.
  - STP\_RUN = 0 (default) the the Hardware Watchdog is cleared in SLEEP and STOP mode.
  - STP\_RUN can be set by CPU, but it cannot be cleared by the CPU
  - STP\_RUN is cleared by software reset (RST)
- Bit3-2: Reserved bits. Always write 0 to these bits.
- Bit1-0: ED (Elongate watchdog duration).

ED1-0	Function
00	The watchdog period is $2^{16}$ CLKRC cycles [initial setting]
01	The watchdog period is $2^{17}$ CLKRC cycles
10	The watchdog period is $2^{18}$ CLKRC cycles
11	The watchdog period is $2^{19}$ CLKRC cycles

- These bits are cleared by software reset (RST) and can be written and read by CPU.

#### 1.2. Caution

The section "Caution" changes as follows:

- Software disabling is not possible.  
The watchdog timer starts counting immediately after reset (release of INITX). Software cannot stop the counting.
- Hardware disabling is only possible on the evaluation device MB91V460A **and MB91FV460B**.  
The watchdog timer can be permanently disabled by setting the corresponding jumper of the

# MB91460E Series

evaluation board (this is not possible on flash devices with this watchdog timer). So always ensure correct configuration of the evaluation system to reflect the behaviour of the flash device.

- Postponement of reset

In order to postpone the watchdog reset, the clearing of the watchdog timer is necessary. Whenever the CL bit of register is set to '0' (there is no minimum writing limitation), the timer is cleared and the occurrence of reset is postponed. Just writing to the register without setting CL to '0' does not clear the timer.

- Timer stop and clear

In modes where the CPU does not work (SLEEP state, STOP state or STOP with RTC active state), the timer is cleared first then the counting is stopped. **If the bit HWWDE.STP\_RUN is set, the counting continues, and the RC oscillator will continue too.**

- During DMA transfer

During DMA transfer between D-bus modules, the writing e0f to CL bit is not possible. Thus, if the transfer time is more than 328ms (calculated from the fastest frequency of the RC oscillator as minimum period), a reset occurs.

- Duration setting

Unlike on MB91V460 Rev.A it is possible to elongate the duration of the watchdog reset.

- CLKRC frequency

Unlike on MB91V460 Rev.A it is possible to change the CLKRC frequency to 2MHz. Even though the watchdog timer is always operated with a frequency of 100kHz (10us) typical.

- Difference between watchdog reset, external reset and Power-on reset

External reset pin (INITX), Clock Supervisor and Hardware Watchdog build a "reset chain":

External reset pin / Power-On reset

→ Clock Supervisor  
→ Hardware Watchdog

→ Shutdown Controller<sup>1</sup>

→ CPU

Each module in the chain transfers the incoming reset signal to its reset output.

External reset pin or Power-On will clear all the modules in the chain, but the Hardware Watchdog reset will not clear the Clock Supervisor.



---

1. Shutdown Controller is implemented on MB91F467E only.

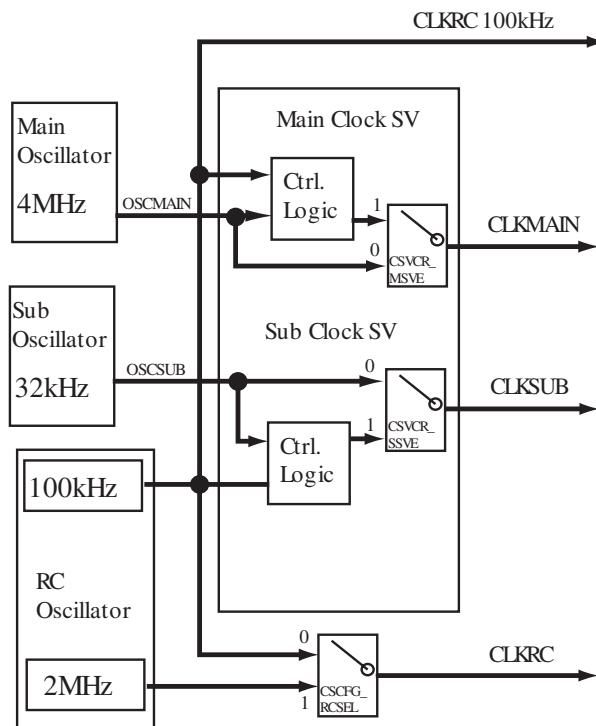
## ■ CLOCK SUPERVISOR (New Feature)

This section gives an overview of the Clock Supervisor. Purpose of the Clock Supervisor is the supervision of the Main- and Sub oscillators. In case of oscillation (OSCMAIN or OSCSUB) failure the Clock Supervisor control logic will take action, i.e. switching to an internal RC-oscillation clock (CLKRC 100kHz), depending on the operation mode set in the control register.

In MB91FV460B, MB91F467P and other new devices, a new Clock Supervisor version with extended functionality is implemented. This new feature is marked with the keyword “New feature”.

### 1. Overview Clock Supervisor

Figure 0-1 Block diagram of the clock supervisor



The purpose of the clock supervisor is the supervision of the main and sub oscillation clocks. In case of a oscillation failure (OSCMAIN and/or OSCSUB) it can be replaced by an on-chip RC-oscillation clock (CLKRC 100kHz), depending on the configuration.

If a clock the MCU currently uses, fails for a certain time (20-80 $\mu$ s for Main clock / 160-640 $\mu$ s for Sub clock) the MCU is reset by Setting Initialization Request (INIT) and the reset cause can be checked after reset vector fetch.

If the Sub clock is failing while the MCU is in Main clock mode, reset can be delayed until the transition to Sub clock mode or no reset will be initiated. The user can choose the behaviour with a control bit in the Clock Supervisor Control Register.

There are two independent supervisors, one for the Main clock and one for the Sub clock. They can be enabled/disabled separately.

Main clock and Sub clock supervisor are disabled and re-enabled automatically if the corresponding oscillator is disabled and re-enabled.

If the MCU changes to STOP state, the RC-oscillator can be automatically disabled by a control bit. It will be enabled again upon wake-up from STOP state.

There are two status bits in the Clock Supervisor Control Register which indicate the failure of the Main clock and Sub clock. These bits can be available at two port pins (device dependent).

Single clock devices can use the CLKRC as Sub clock.

**New feature:** The two Clock Supervisor status bits can be cleared by CPU access, if the main and/or sub oscillator has resumed oscillation. The clock is switched back to OSCMAIN and/or OSCTSUB in this case.

**New feature:** The RC oscillator is enabled in STOP mode automatically, if the Hardware Watchdog is configured to run during STOP. The RC oscillator can **only** be stopped in STOP mode, and then it depends on the Hardware Watchdog and the control bit in the Clock Supervisor Control Register.

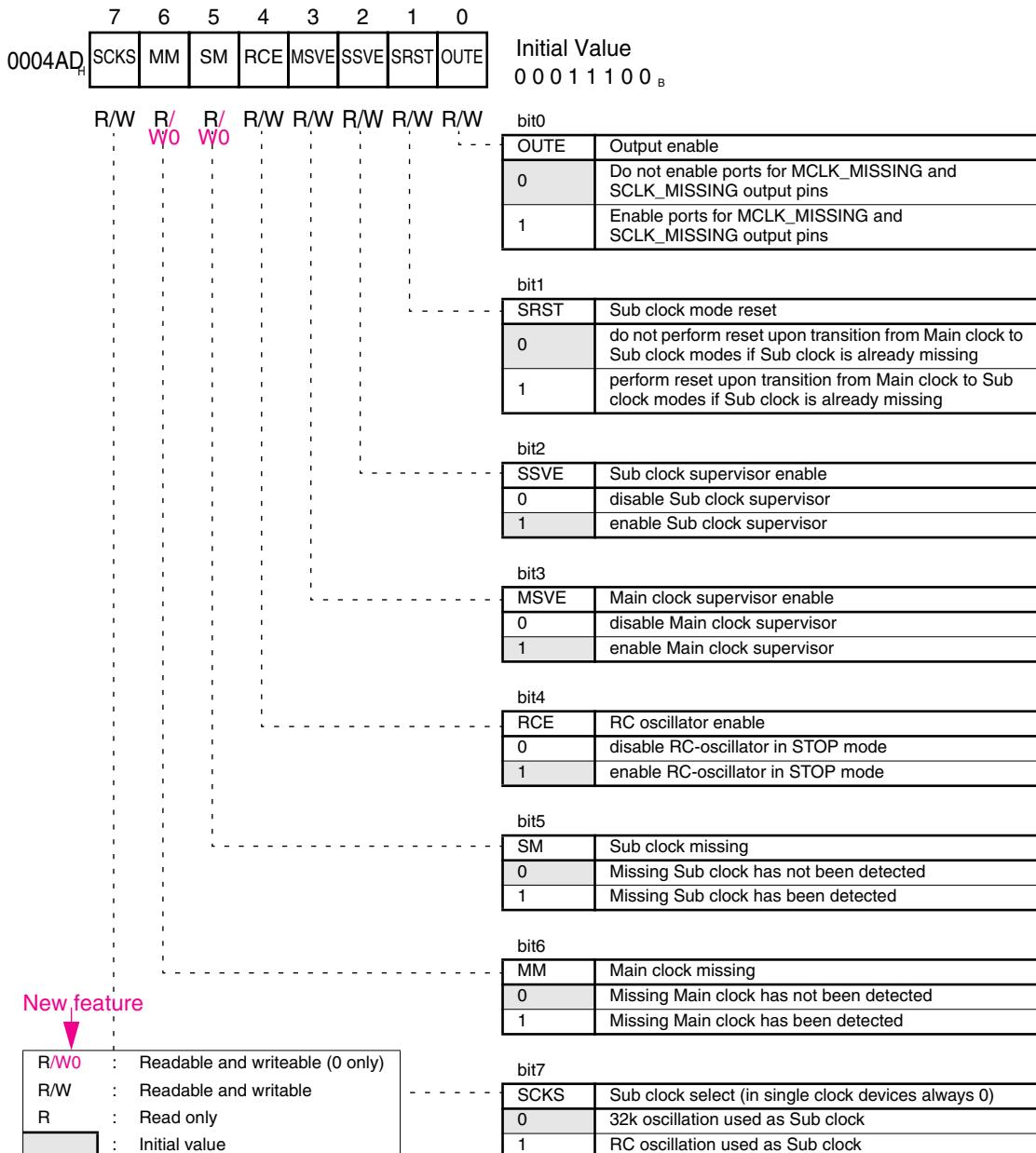
## 2. Clock Supervisor Register

This section lists the Clock Supervisor Control Register and describes the function of each bit in detail.

## 2.1. Clock Supervisor Control Register (CSVCR)

The Clock Supervisor Control Register (CSVCR) sets the operation mode of the Clock Supervisor. [Figure 0-2](#) shows the configuration of the Clock Supervisor Control Register.

**Figure 0-2 Configuration Clock Supervisor Control Register (CSVCR)**



# MB91460E Series

Table 0-1 describes the function of each bit of the Clock Supervisor Control Register (CSVCR).

**Table 0-1 Functional Description of each bit of the Clock Supervisor Control Register**

Bit	Name	Function
7	SCKS (Sub clock select)	<p>This bit is to select between 32 kHz external oscillation and internal RC oscillation as Sub clock. If this bit is '0' then the external 32 kHz oscillation is used as Sub clock, if it's '1' then the internal RC oscillation is used as Sub clock. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.</p> <p>Note: Don't change this bit while the CPU runs on Sub clock. First switch back to Main clock and then change SCKS!</p>
6	MM (Main clock missing)	<p>If this bit is 1, the Main clock supervisor has detected that the Main oscillation clock coming from X0, X1 is missing, e.g. by a broken crystal. If this bit is '0', a missing Main clock has not been detected. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.</p> <p><b>New feature:</b> This bit can be cleared by CPU access, if the main oscillator has resumed oscillation. If the main oscillator is still failing, the write access is ignored.</p>
5	SM (Sub clock missing)	<p>If this bit is 1, the Sub clock supervisor has detected that the sub oscillation clock coming from X0A, X1A is missing, e.g. by a broken crystal. If this bit is '0', a missing Sub clock has not been detected. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.</p> <p><b>New feature:</b> This bit can be cleared by CPU access, if the sub oscillator has resumed oscillation. If the sub oscillator is still failing, the write access is ignored.</p>
4	RCE (RC-oscillator enable)	<p>Setting this bit to '1' enables the RC-oscillator in STOP mode. Outside STOP mode, the RC-oscillator is always enabled. This bit is set to '1' by Power-On reset or external reset. Other types of reset will not affect this bit.</p> <p><b>New feature:</b> If HWWDE.STP_RUN (=HWWDE[4]) is set in the Hardware Watchdog, then the RC oscillator is enabled and read and read-modify-write operations will return '1' independently of RCE register setting.</p> <p>Effective RCE = RCE_Register or HWWDE.STP_RUN</p>
3	MSVE (Main clock supervisor enable)	Setting this bit to '1' enables the Main clock supervisor. This bit is set to '1' by Power-On reset only. Other types of reset will not affect this bit.
2	SSVE (Sub clock supervisor enable)	Setting this bit to '1' enables the Sub clock supervisor. This bit is set to '1' by Power-On reset only. Other types of reset will not affect this bit.
1	SRST (Sub clock mode reset)	If this bit is set to '1', a reset is performed upon transition from Main/PLL clock mode to Sub clock mode if the Sub clock is already missing. If this bit is set to '0', no reset is performed in this case. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.
0	OUTE (Output enable)	This bit can be used as an output enable to output the signals MCLK_MISSING (bit 3 of CSVCR) and SCLK_MISSING (bit 4 of CSVCR) to port pins. For more information about the pins see the corresponding Datasheet. If this bit is set to '1', the ports are enabled for MCLK_MISSING and SCLK_MISSING output. This bit is cleared to '0' by Power-On reset or external reset. Other types of reset will not affect this bit.

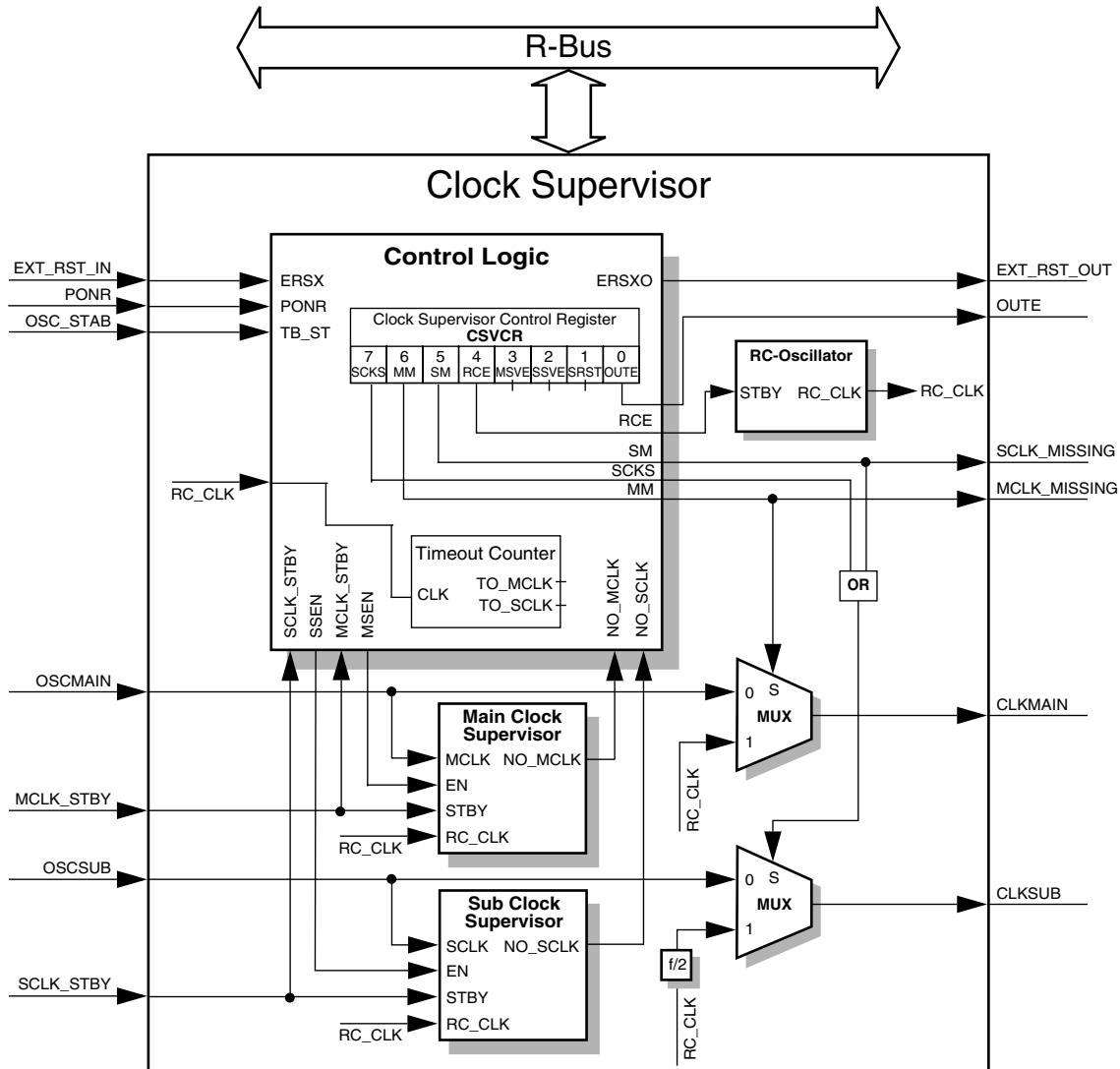
### 3. Block Diagram Clock Supervisor

This section presents a block diagram of the Clock Supervisor. The building blocks of the Clock Supervisor are:

- Main Clock Supervisor
- Sub Clock Supervisor
- Control Logic
- RC-Oscillator

### 3.1. Block Diagram Clock Supervisor

**Figure 0-3 Block Diagram of Clock Supervisor**



SCLK\_OUT and MCLK\_OUT can be observed using the Clock Monitor Module. SCLK\_MISSING and MCLK\_MISSING can be programmed to device specific outputs (see the datasheet of the used device for the information which pins are used) by setting OUTE=1.

Signal EXT\_RST\_IN is the reset input, connected to the external INITX pin.

Signal EXT\_RST\_OUT is the reset output and causes Setting Initialization Request (INIT).

## 4. Operation Modes

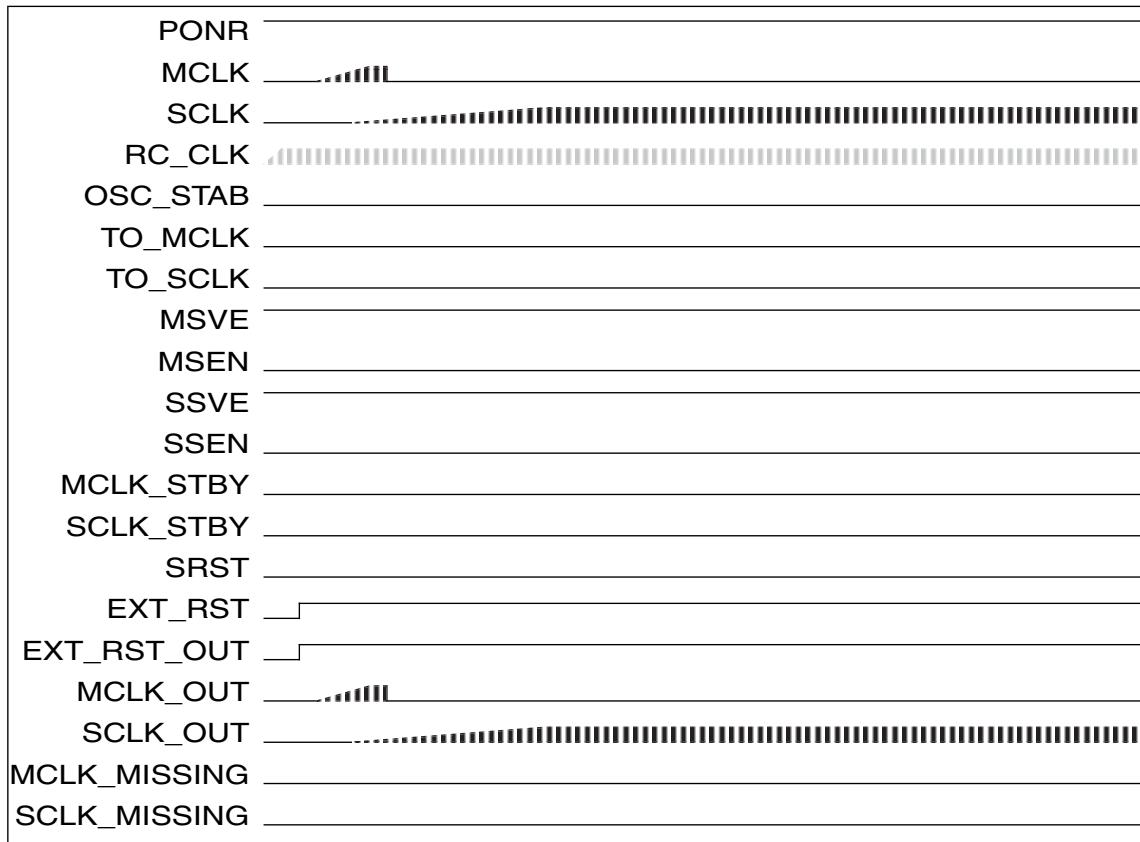
This section describes all operation modes of the Clock Supervisor.

### 4.1. Operation mode with initial settings

In case the clock supervisor control register (CSVCR) is not configured at the beginning of the user program, the RC-oscillator, the Main clock supervisor and the Sub clock supervisor is enabled.

- The RC-oscillator is enabled at power-on.
- The Main clock supervisor is enabled after the 'oscillation stabilization wait time' or in case the Main clock is missing before the completion of the 'oscillation stabilization wait time', after the 'Main clock timeout' (TO\_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC. If the Main clock is missing from power-on, the power-on reset state is never left, which in this case is a safe state. The user must make sure with external pull-up/pull-down resistors that all relevant signal are pulled to the correct level.
- The Sub clock supervisor is enabled after the completion of the 'Sub clock timeout' (TO\_SCLK) from the timeout counter. The timeout counter is clocked with CLKRC.
- If the Main clock stops while the Main clock supervisor is enabled, the Main clock is replaced with CLKRC 100kHz, the MM bit is set to '1' and reset (EXT\_RST\_OUT) is asserted.
- If the Sub clock stops and the Sub clock supervisor is enabled, the behaviour depend on whether the MCU is in Main clock mode or in Sub clock mode. If the Sub clock stops in Sub clock mode, CLKRC divided by two substitutes the Sub clock, the SM bit is set to '1' and reset (EXT\_RST\_OUT) is asserted. If the Sub clock stops in Main clock mode, CLKRC divided by two substitutes the Sub clock, the SM bit is set to '1' and no reset occurs upon transition to Sub clock mode, since the SRST bit has its initial value of '0'. If the SRST bit is '1' a reset (INIT) occurs.

Figure 0-4 Timing Diagram: Initial settings, Main clock missing during power-on reset



# MB91460E Series

Figure 0-5 Timing Diagram: Initial settings, Main clock missing during 'oscillation stabilization wait time'

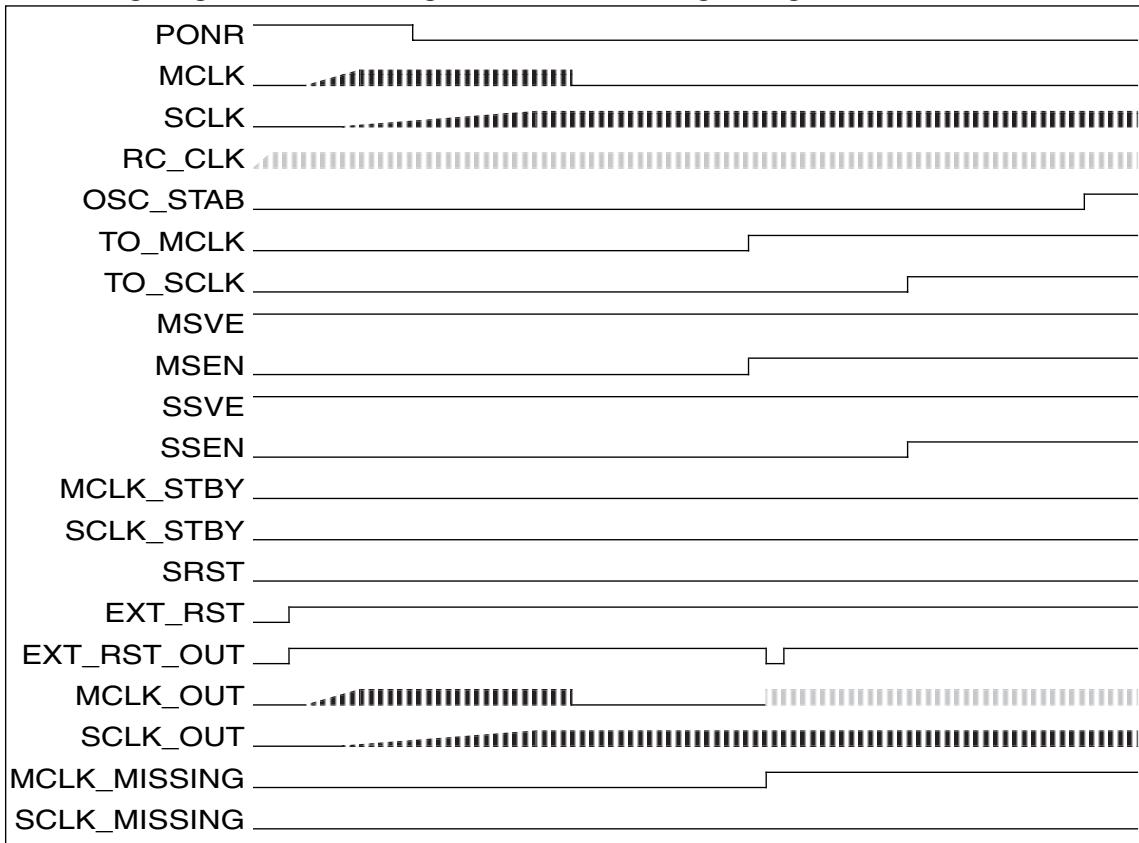
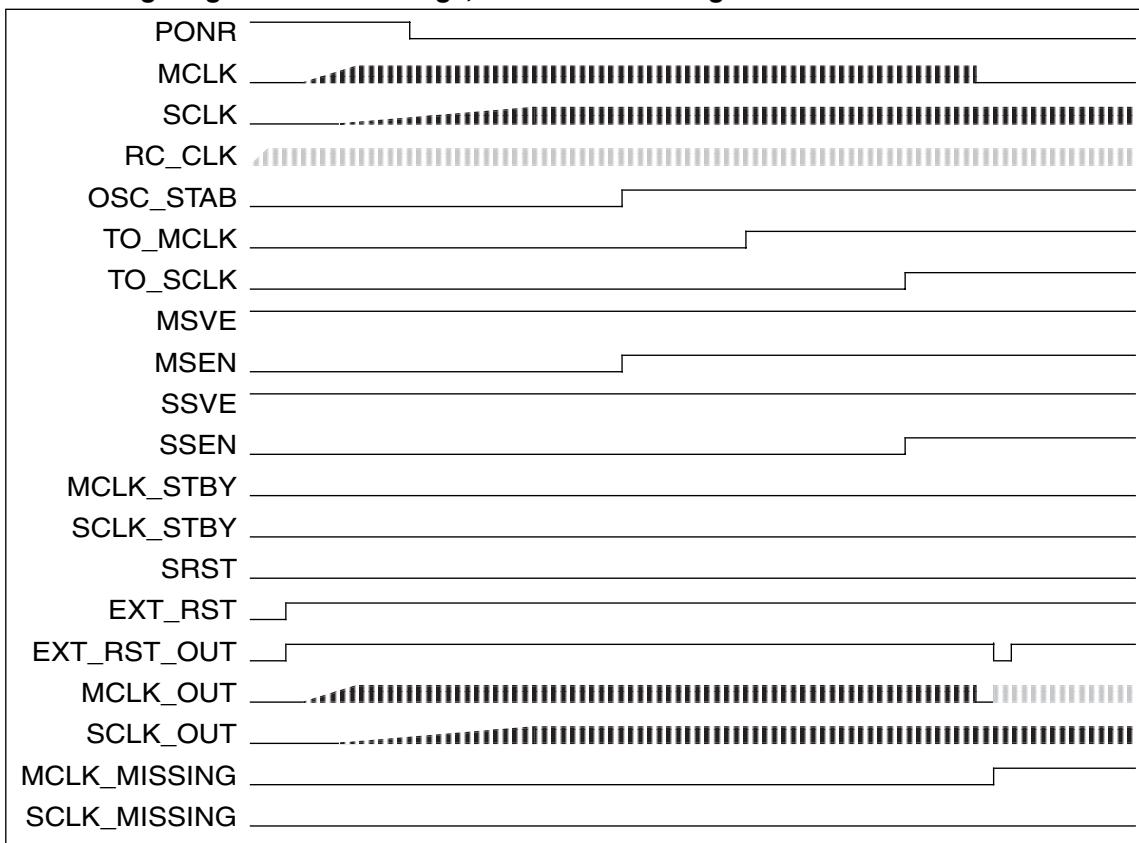


Figure 0-6 Timing Diagram: Initial settings, Main clock missing after 'oscillation stabilization wait time'



# MB91460E Series

Figure 0-7 Timing Diagram: Initial settings, Sub clock missing before timeout

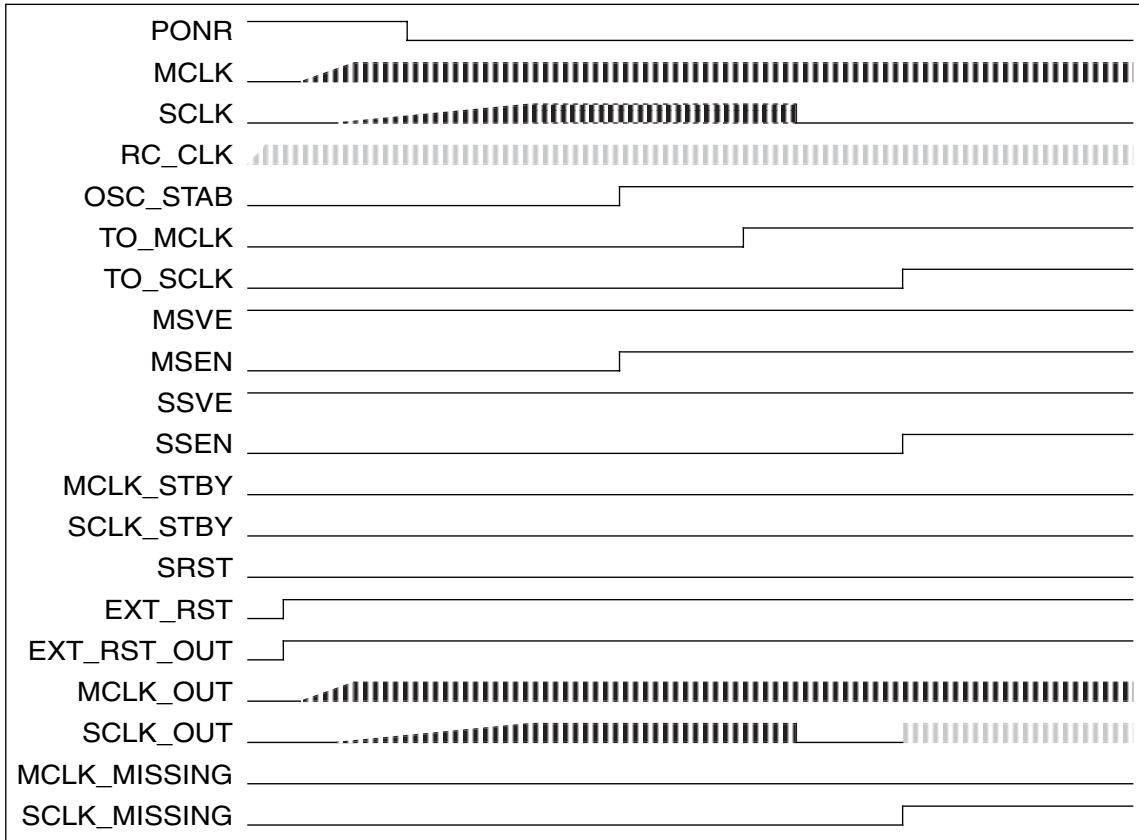
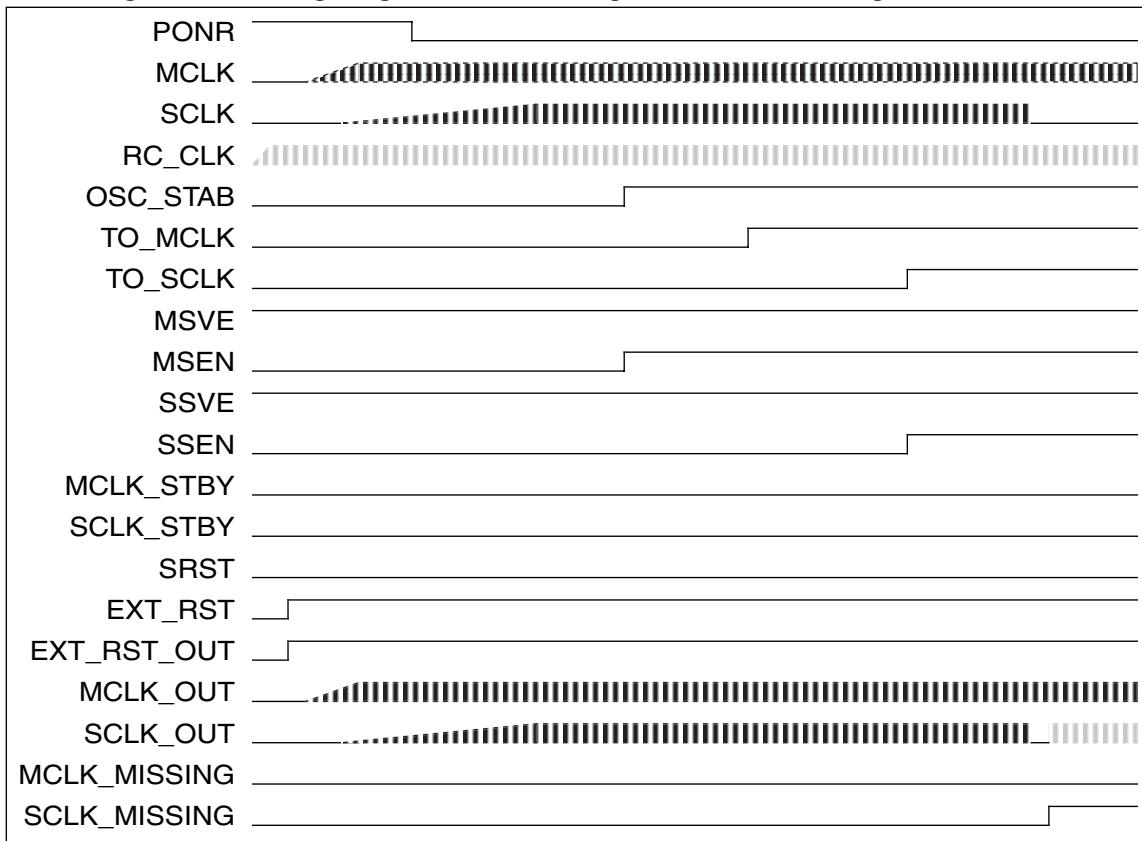


Figure 0-8 Timing Diagram: Initial settings, Sub clock missing after timeout

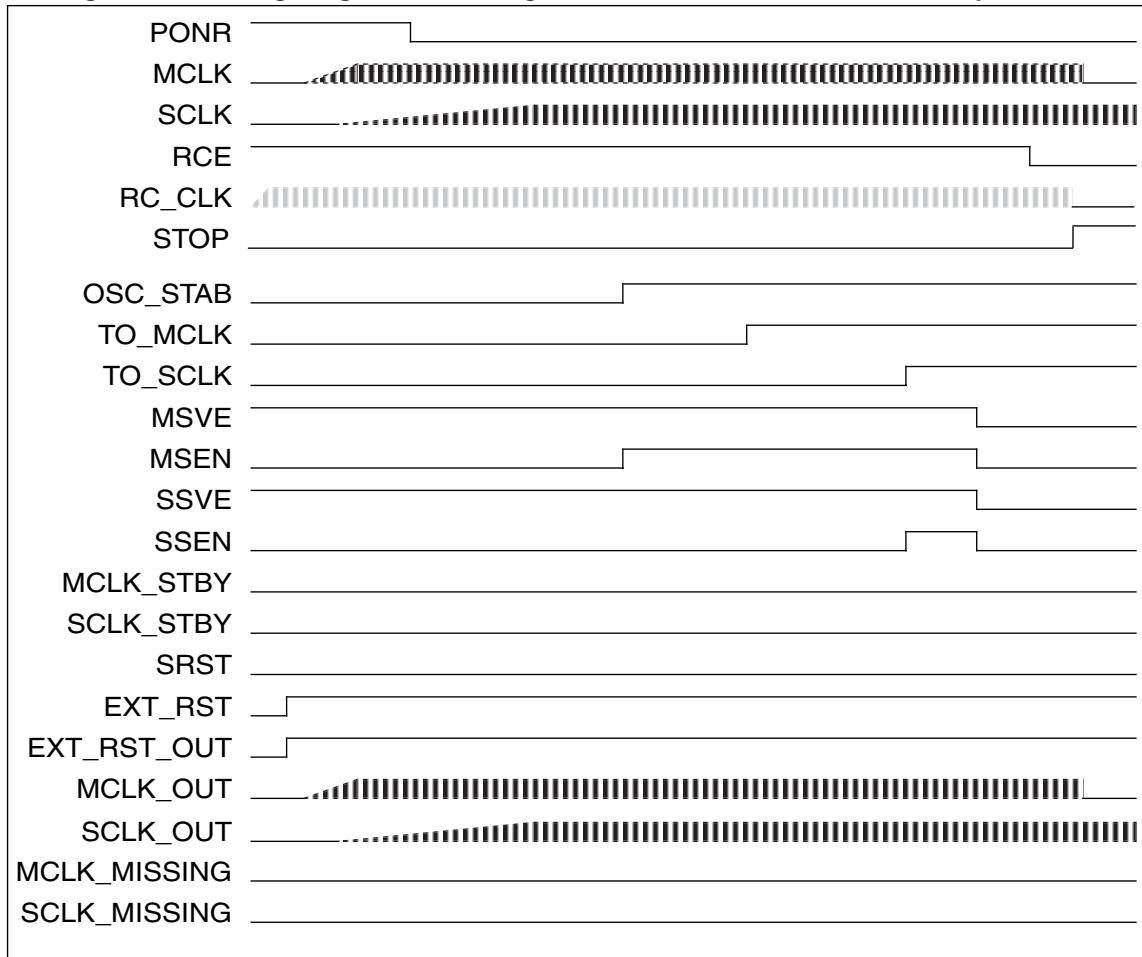


## 4.2. Disabling the RC-oscillator and the clock supervisors

The initial point of this scenario is that the RC-oscillator and Main clock or Sub clock supervisor is enabled.

- The RC-oscillator can be disabled only in STOP mode.  
First check that both SM and MM (bit 5 and bit 6 of CSVCR) are '0'.  
Then disable the RC-oscillator by setting RCE to '0'. If either SM or MM bit is '1', RCE must not be set to '0'.
- **New feature:** If the Hardware Watchdog is to run in STOP mode (HWWDE.STP\_RUN='1') then the RC-oscillator is enabled by hardware.
- The Main clock supervisor is disabled by setting MSVE (bit 3 of CSVCR) to '0'.
- The Sub clock supervisor is disabled by setting SSVE (bit 2 of CVSVR) to '0'.

**Figure 0-9 Timing Diagram: Disabling the RC-oscillator and the clock supervisors**

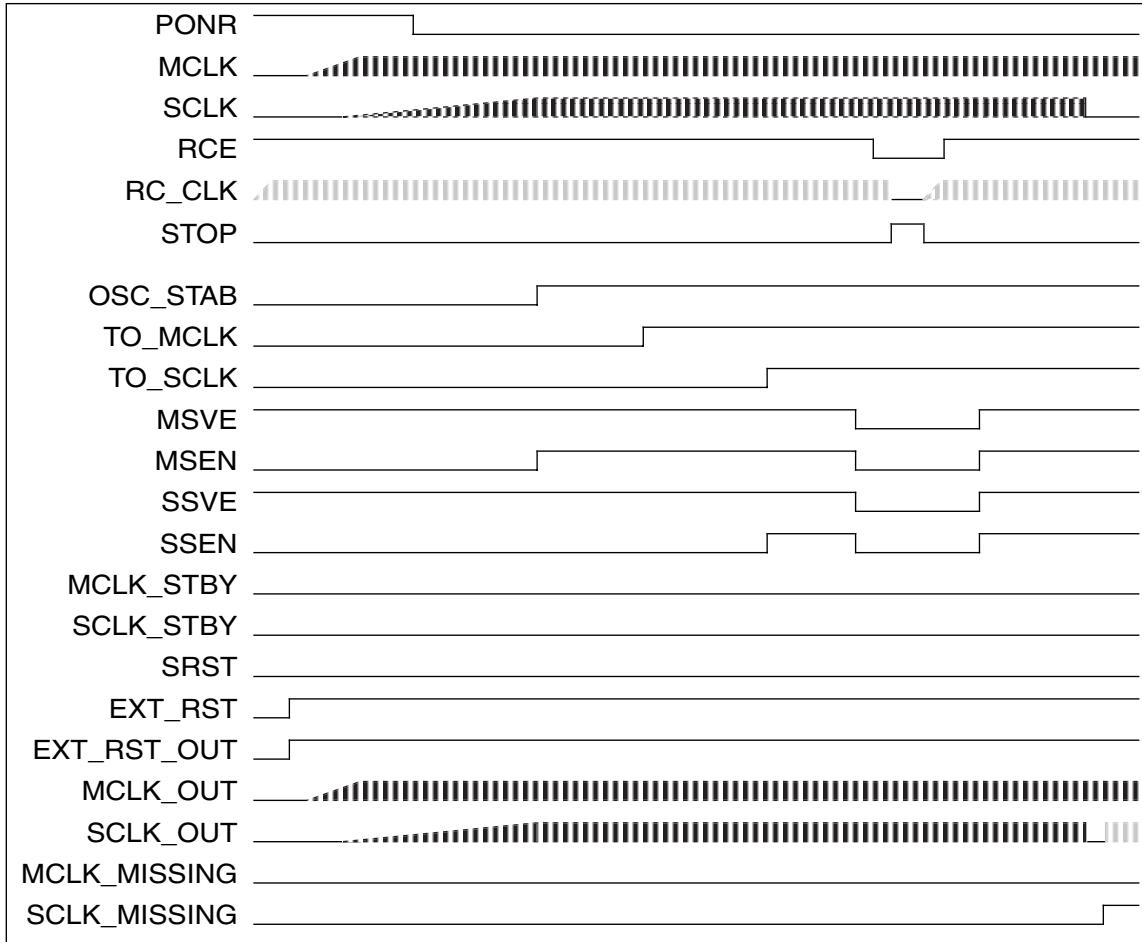


## 4.3. Re-enabling the RC-oscillator and the clock supervisors

The initial point of this scenario is that the RC-oscillator and both Main clock and Sub clock supervisor are disabled.

- The RC-oscillator is always enabled in RUN state. It can only be disabled in STOP, and after wakeup from STOP it will re-start automatically.
- The Main clock supervisor is enabled by setting MSVE (bit 3 of CSVCR) to '1'.
- The Sub clock supervisor is enabled by setting SSVE (bit 2 of CSVCR) to '1'.

**Figure 0-10 Timing Diagram: Re-enabling the RC-oscillator and the clock supervisors**



## 4.4. New feature: Switching back from RC to Main Oscillation

The initial point of this scenario is that the Main clock was missing, the Main clock supervisor has set the MM flag and switched to RC clock. The CPU already got reset (INIT) from clock supervisor and has detected MM=1 as reset source (See "Check if reset was asserted by the Clock Supervisor" on P. 73). The user is quite sure that the Main clock returned meanwhile or will return soon and wants to switch back to Main clock.

- The MM flag can be cleared by writing '0' (bit 6 of CSVCR).
- If the Main clock is still missing during the write access, the write operation has no effect, the MM flag keeps '1' value and the clock supervisor continues giving out RC clock.
- If the Main clock is operating during the write access, the MM flag is cleared and the clock is switched back to Main clock.
- It is possible to poll the MM flag until the Main clock is resumed:

```
ldi      #_csvcr,r1
clear_CSV_loop:
bandh  #0b1001,@r1      ; Clear MM+SM
btsth  #0b0110,@r1      ; Check: Is one of them 1?
bne    clear_CSV_loop
```

## 4.5. New feature: Switching back from RC to Sub Oscillation

The initial point of this scenario is that the CPU is running on Sub clock and Sub clock was missing. The Sub clock supervisor has set the SM flag and switched to RC clock (divided by 2). A clock supervisor reset was not generated because of CSVCR.SRST was '0'. Now the CPU is running user software on RC clock. The flag SM=1 was found by polling. The user is quite sure that the Sub oscillation returned meanwhile or will return soon and wants to switch back to Sub oscillation.

- The SM flag can be cleared by writing '0' (bit 5 of CSVCR).
- If the Sub clock is still missing during the write access, the write operation has no effect, the SM flag keeps '1' value and the clock supervisor continues giving out RC clock.
- If the Sub clock is operating during the write access, the SM flag is cleared and the clock is switched back to Sub clock.
- It is possible to poll the SM flag like described in the Main clock example above.

## 4.6. Sub clock modes

The Main clock supervisor is automatically disabled in Sub clock modes. The enable bit MSVE remains unchanged. At transition from Sub clock mode to Main clock mode the Main clock supervisor is enabled after the 'oscillation stabilization wait time' or in case the Main clock is missing before the completion of the 'oscillation stabilization wait time', after the 'Main clock timeout' (TO\_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC.

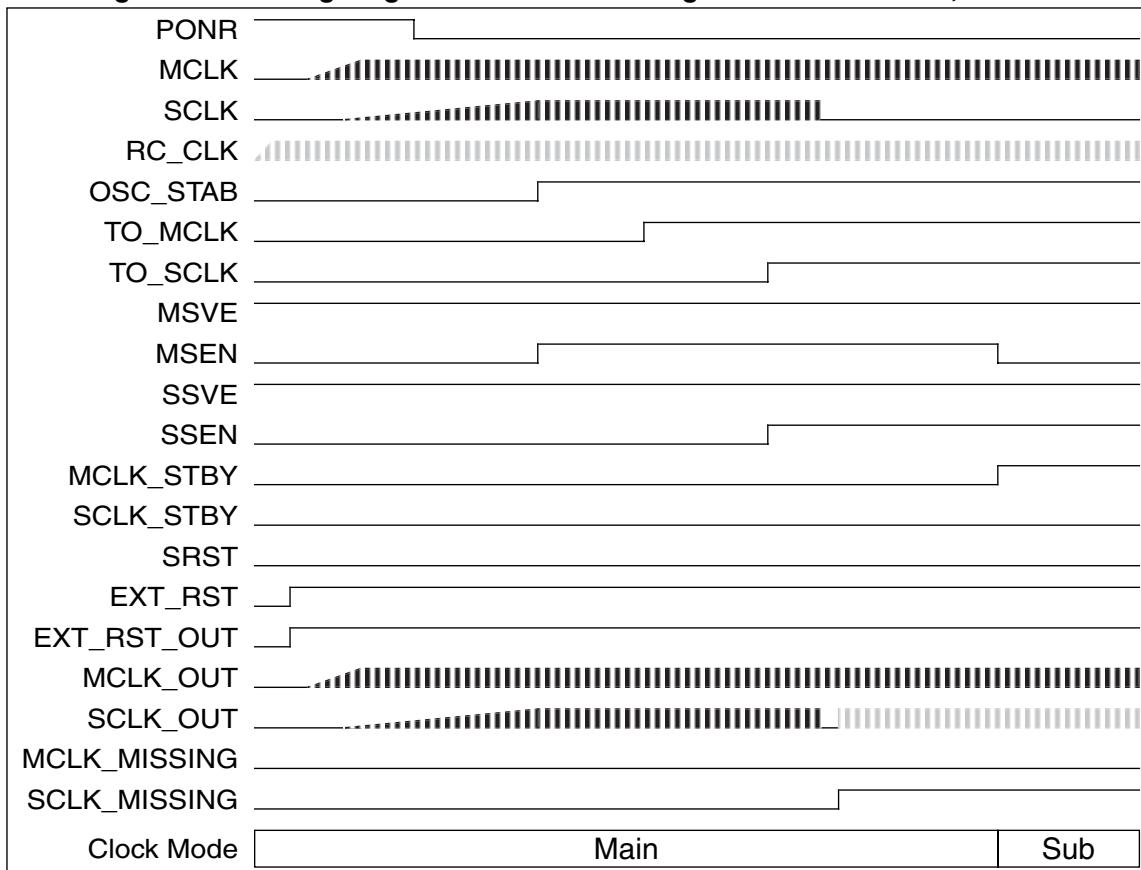
## 4.7. Changing the behaviour upon transition to Sub clock mode if the Sub clock has already stopped in Main clock mode

If the Sub clock has stopped in Main clock mode and this was detected by the Sub clock supervisor, the behaviour upon transition to Sub clock mode depends on the state of the SRST bit.

- If SRST is set to '0' (initial value), reset is not asserted at the transition to Sub clock mode. The transition is performed using the RC-oscillation clock as Sub clock. In this case it is recommended to check the SM bit before the transition to Sub clock mode to get the information if Sub clock or CLKRC is used.
- If SRST is set to '1', reset is asserted at the transition to Sub clock mode.

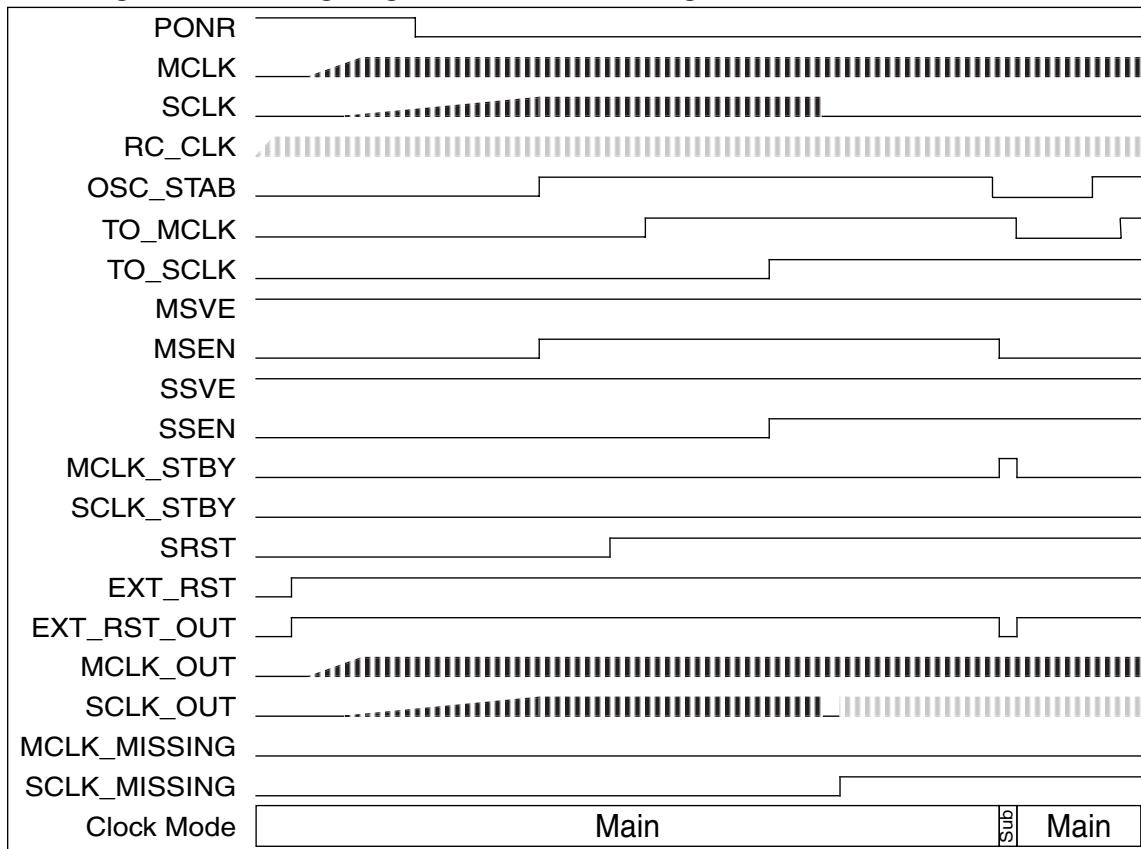
The following timing diagrams (Figure 0-11, Figure 0-12, ) illustrate this behaviour.

Figure 0-11 Timing Diagram: Sub clock missing in Main clock mode, SRST=0

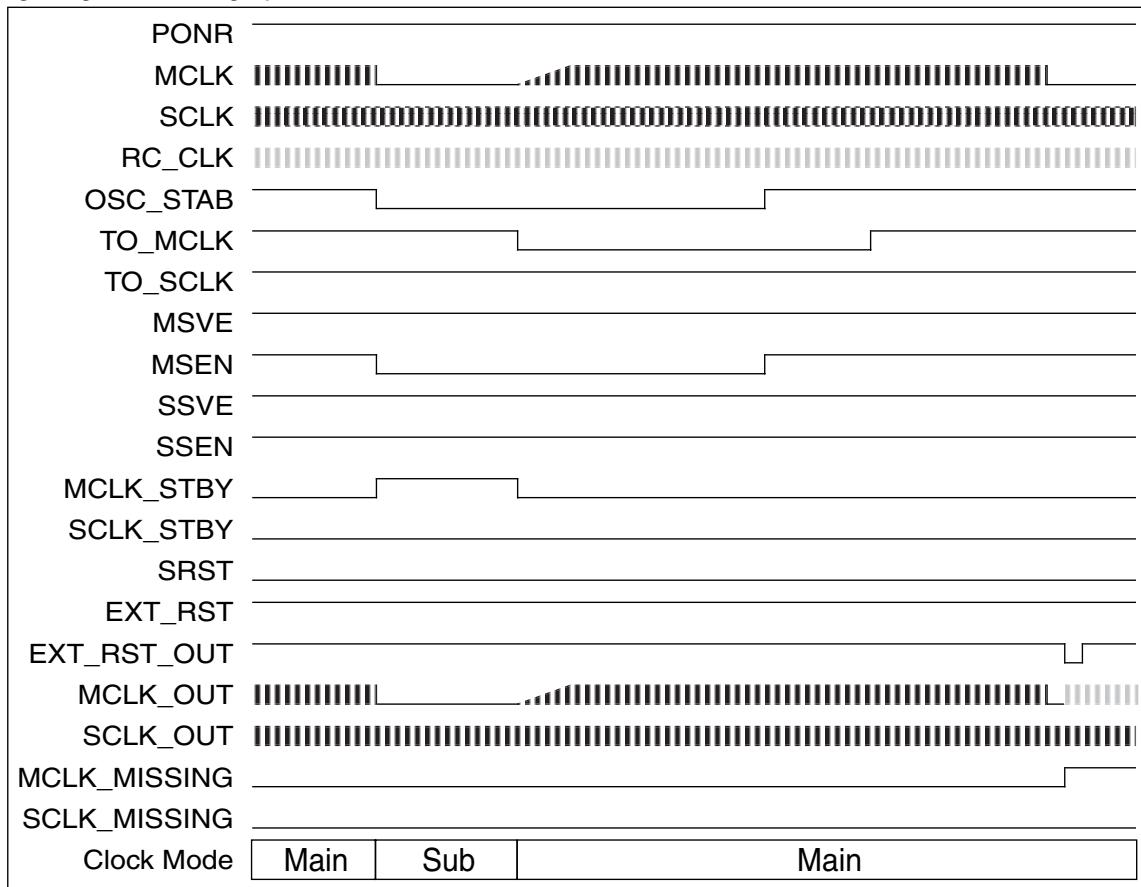


# MB91460E Series

Figure 0-12 Timing Diagram: Sub clock missing in Main clock mode, SRST=1



Timing Diagram: Waking up from Sub clock mode



# MB91460E Series

## 4.8. STOP mode (with both oscillators disabled)

In this section, "STOP mode" means that the CPU is in STOP state and both oscillators are disabled by setting STCR.OSCD1='1' and STCR.OSCD2='1'. The Clock Supervisor's inputs MCLK\_SBY and SCLK\_SBY are connected to the oscillator disable lines OCSD1 and OSCD2, respectively.

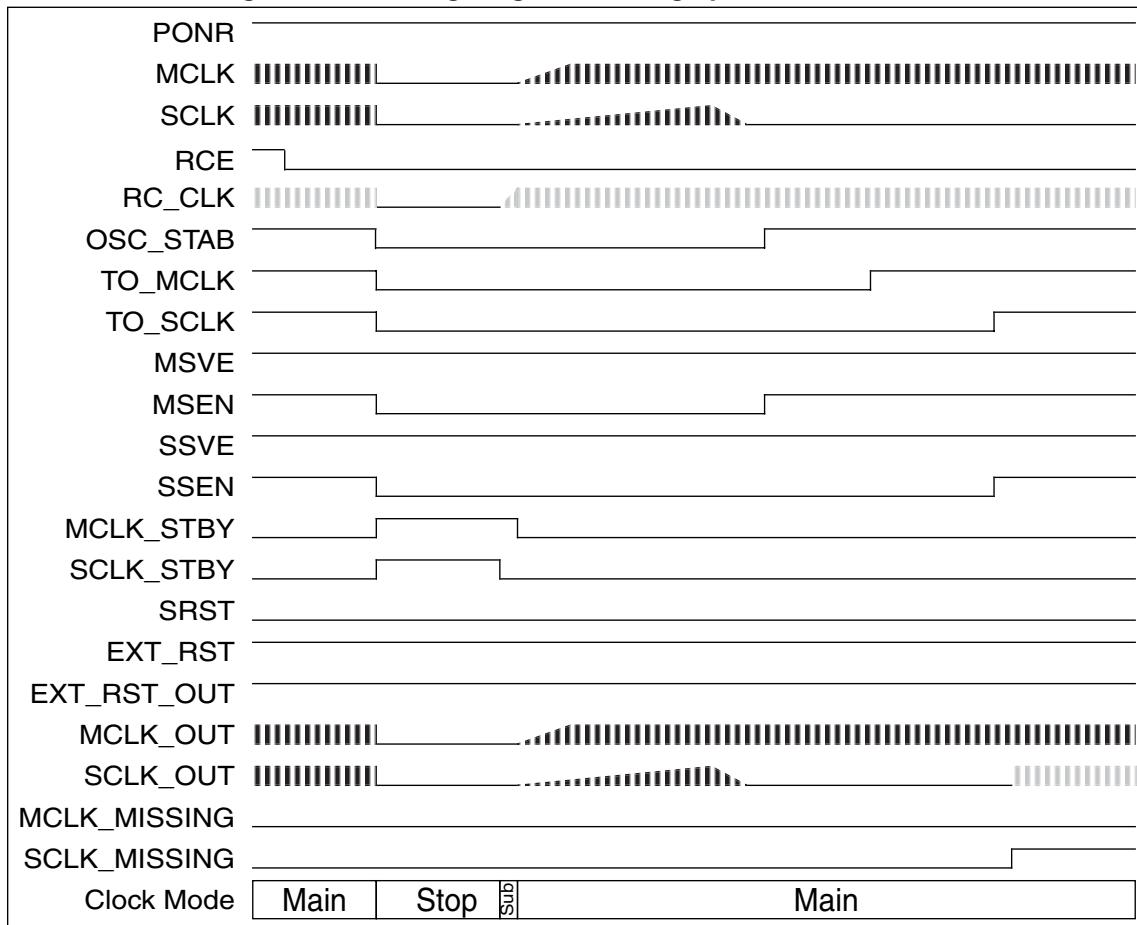
If Main clock and Sub clock supervisors are enabled, they will be automatically disabled at transition into STOP state. The corresponding enable bits in the clock supervisor control register remain unchanged. So after wake-up from STOP mode the clock supervisors will be enabled again. If the corresponding enable bits are set to '0', the clock supervisors will stay disabled after wake-up from STOP mode.

The RC-oscillator is disabled in STOP, if the RCE bit in the CSVCR register is cleared.

**New feature:** If the Hardware Watchdog is enabled in STOP state (HWWDE.STP\_RUN='1'), then the RC-oscillator is enabled by hardware during STOP. The RCE bit is unchanged, but read and read-modify-write operations return '1'.

- The RC-oscillator is enabled immediately after wake-up from STOP mode.
- The Main clock supervisor is enabled after the 'oscillation stabilization wait time' or in case the Main clock is missing after wake-up from STOP mode, after the 'Main clock timeout' (TO\_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC.
- The Sub clock supervisor is enabled after the 'Sub clock timeout' (TO\_SCLK) from the timeout counter which is clocked with the CLKRC.

**Figure 0-13 Timing Diagram: Waking up from STOP state**



## 4.9. RTC mode (STOP mode with Real Time Clock enabled)

In this section, “RTC mode” means that the CPU is in STOP state and one of the quartz oscillators is enabled by setting STCR.OSCD1=’0’ or STCR.OSCD2=’0’. The enabled oscillator clock is switched to the Real Time Clock to keep it running during STOP. The behaviour of the Clock Supervisor depends on several settings.

- If the RTC is connected to Main clock, the behaviour of the main clock supervisor is like described in Table 0-2

**Table 0-2 Main Clock Supervisor in RTC mode.**

RC oscillator enable CSVCR.RCE	Main Oscillator disable STCR.OSCD1	Main clock supervisor enable SVCR.MSVE	Behaviour in STOP mode if Main clock fails and the RTC is connected to Main clock
1	1	X	Main clock fail cannot be seen because the Main oscillator is disabled. The Main clock supervisor is disabled because of the Main oscillator is disabled. The RTC will not run because of the same reason. Note: This is no RTC mode.
1	0	1	The clock supervisor will set MM flag, switch the Main clock to RC clock and generate an reset (INIT) to CPU. The STOP mode is cancelled by the reset. The RTC is initialized by the reset.
1	0	0	Main clock supervisor is disabled by MSVE=0. In case of Main clock fail, the RTC clock simply stops.
0	X	X	Main clock supervisor is disabled because of it does not get RC clock. In case of Main clock fail, the RTC clock simply stops.

Note **New feature:** RCE setting is valid if HWWDE.STP\_RUN (HWWDE[4]) is ‘0’. Otherwise, RCE is overwritten to ‘1’.

- If the RTC is connected to Sub clock, the behaviour of the sub clock supervisor is like described in Table 0-3

**Table 0-3 Sub Clock Supervisor in RTC mode.**

RC oscillator enable CSVCR.RCE	Sub Oscillator disable STCR.OSCD2	Sub clock supervisor enable SVCR.SSVE	Behaviour in STOP mode if Sub clock fails and the RTC is connected to Sub clock
1	1	X	Sub clock fail cannot be seen because the Sub oscillator is disabled. The Sub clock supervisor is disabled because of the Sub oscillator is disabled. The RTC will not run because of the same reason. Note: This is no RTC mode.
1	0	1	The clock supervisor will set SM flag and switch the Sub clock to RC clock. The RTC continues running on RC clock. A reset is not generated because there is no transition from Main clock to Sub clock during STOP mode.
1	0	0	Sub clock supervisor is disabled by SSVE=0. In case of Sub clock fail, the RTC clock simply stops.
0	X	X	Sub clock supervisor is disabled because of it does not get RC clock. In case of Sub clock fail, the RTC clock simply stops.

Note **New feature:** RCE setting is valid if HWWDE.STP\_RUN (HWWDE[4]) is ‘0’. Otherwise, RCE is overwritten to ‘1’.

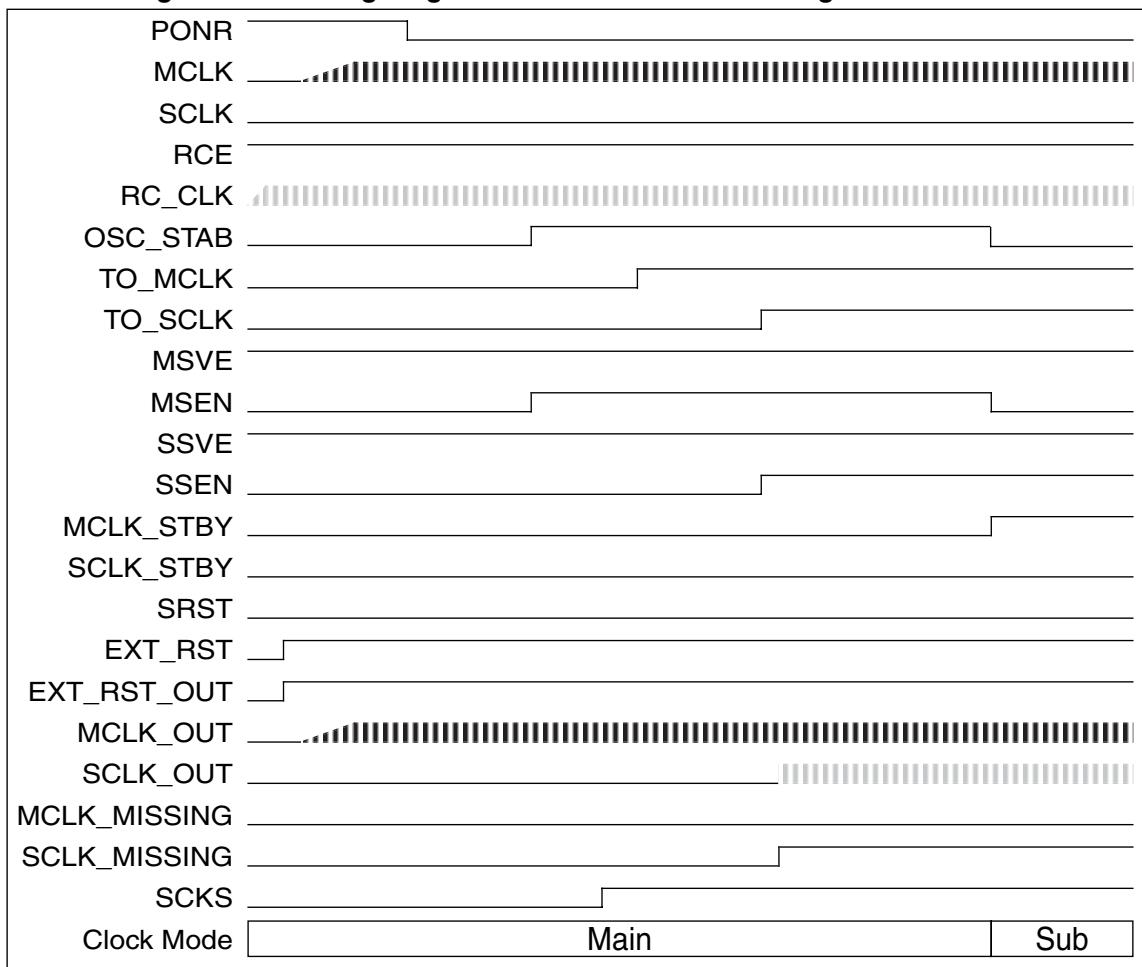
- The RC-oscillator is enabled immediately after wake-up from STOP state.

- If the Main clock was disabled in STOP: The Main clock supervisor is enabled after the 'oscillation stabilization wait time' or in case the Main clock is missing after wake-up from STOP state, after the 'Main clock timeout' (TO\_MCLK) from the timeout counter. The timeout counter is clocked with CLKRC.
- If the Sub clock was disabled in STOP: The Sub clock supervisor is enabled after the 'Sub clock timeout' (TO\_SCLK) from the timeout counter which is clocked with the CLKRC.

## 4.10. RC-Clock as Sub Clock

The Sub clock supervisor can provide the CLKRC as Sub clock. To enable this feature, SCKS bit (bit7 of CSVCR) must be set to '1'.

**Figure 0-14 Timing Diagram: Sub clock mode with single clock device**



## 4.11. Check if reset was asserted by the Clock Supervisor

To find out whether the Clock Supervisor has asserted reset, the software must check the reset cause by reading the RSRR register (see the hardware manual "RSRR: Reset Cause Register" on P. 229). On the most flash devices, the RSRR register is read and cleared by the Boot ROM software. The content of RSRR can be found in CPU register R4[7:0] after Boot ROM is done.

If INIT (bit 7 of RSRR) is set, the cause was either external reset at the INITX pin or the clock supervisor or the hardware watchdog (HWWD). If neither SM bit nor MM bit (bit 5 and bit 6 of CSVCR) is set, reset cause was the external reset or the hardware watchdog. If SM is '1' the reset cause is a missing Sub clock and if MM is '1' the reset cause is a missing Main clock.

## 5. Cautions

After a Clock Supervisor reset, the CLKPLL is not usable as clk source, if the clock supervisor reset was caused by a missing OSCMAIN.

## ■ USART LIN/FIFO (Extension)

This chapter describes an extension of the USART (LIN/FIFO USART).

For reference, please refer to chapter 32 USART (LIN/FIFO) in the MB91460 series hardware manual.

### 1. USART End of Transmission Interrupt (ET)

The USART macros have been extended to generate an "End of Transmission" (ET) interrupt after the last bit of a transmission has been sent. If ET is enabled and there is no FIFO installed, the interrupt is generated after each transmission. If FIFO is installed, ET appears after the transmission while the FIFO is empty.

The ET interrupt cannot request a DMA transfer.

The ET can be enabled and observed in the FSR (FIFO Status Register). Therefore, also USART modules which are not equipped with FIFO, have the FIFO Status Register.

#### 1.1. USART Interrupts

With the ET interrupt, the list of USART interrupts extends to:

Reception/transmis-sion/ICU	Inter-rupt request flag	Flag Register	Operation mode				Interrupt cause	Interrupt cause enable bit	How to clear the Interrupt Request
			0	1	2	3			
Reception	RDRF	SSR	x	x	x	x	receive data is written to RDR (FIFO level reached)	SSR:RIE	Receive data is read
	ORE	SSR	x	x	x	x	Overrun error		"1" is written to clear rec. error bit (SCR: CRE)
	FRE	SSR	x	x	*1	x	Framing error		
	PE	SSR	x		*2		Parity error		
	LBD	ESCR	x			x	LIN synch break detected	ESCR:LBIE	"0" is written to ESCR:LBD
	TBI & RBI	ESCR	x	x		x	no bus activity	ECCR:BIE	Receive data / Send data

# MB91460E Series

Transmission	TDRE	SSR or FSR * <sup>3</sup>	x	x	x	x	Empty transmission register	SSR:TIE	Transfer data is written
	ET	FSR	x	x	x	x	End of transmission [and FIFO empty * <sup>4</sup> ]	FSR:ETIE	"0" is written to FSR:ETINT
Input Capture Unit	ICP4	IPCP	x			x	1st falling edge of LIN synch field	IPCP:ICE	disable ICE temporary
	ICP4	IPCP	x			x	5th falling edge of LIN synch field	IPCP:ICE	disable ICE

- Only available if ECCR04/SSM = 1
- Only available if ECCR04/SSM = 1
- FSR:TDRE is a read-only mirror of the SSR:TDRE bit
- if FIFO is installed

X: Used

## 1.2. FSR: FIFO Status register for ET interrupt control

The FSR register controls and observes the ET interrupt and displays FIFO status (if FIFO is installed).

15	14	13	12	11	10	9	8	Bit
<b>TDRE</b>	<b>ETINT</b>	<b>ETIE</b>	<b>NVFD (Number of valid FIFO data)</b>					
X	X	0	0	0	0	0	0	Initial value
R	R,W0	R,W	R	R	R	R	R	Attribute

- bit15: TDRE Transmission Data Register Empty flag (shadow)
  - This is a read-only shadow of TDRE flag. Interrupt routines can determine the interrupt source (TDRE or ET) by just reading the FSR register.
- bit 14: ETINT End of Transmission interrupt flag
  - This flag is set when the ET condition has appeared:
    - If no FIFO is installed, after the last bit of a transmission has been sent,
    - if FIFO is installed, after the last bit of a transmission has been sent and the FIFO is empty.
  - This flag is cleared by software reset (RST) or by writing 0.
  - Writing 1 has no effect.
  - Read - modify - write access always reads 1.
- bit13: ETIE End of Transmission interrupt enable
  - ETIE = 1 enables that the ET interrupt request is sent to the CPU when ETINT is set.
  - ETIE = 0 (default) disables the ET interrupt request.
  - This bit is cleared by software reset (RST) and can be written and read by CPU.
- bit12-8: NVFD[4:0] Number of valid FIFO data
  - These bits indicate the number of stored receptions (SVD=0) or pending transmissions (SVD=1) in the FIFO buffer.
  - If no FIFO is installed, these bits return 0x00.

■

# MB91460E Series

## ■ SHUTDOWN MODE

### 1. Overview

In Shutdown mode, the power supply of more than 80% of the internal logic and the main memories is switched off to minimize leakage.

This mode is a type of STOP state.

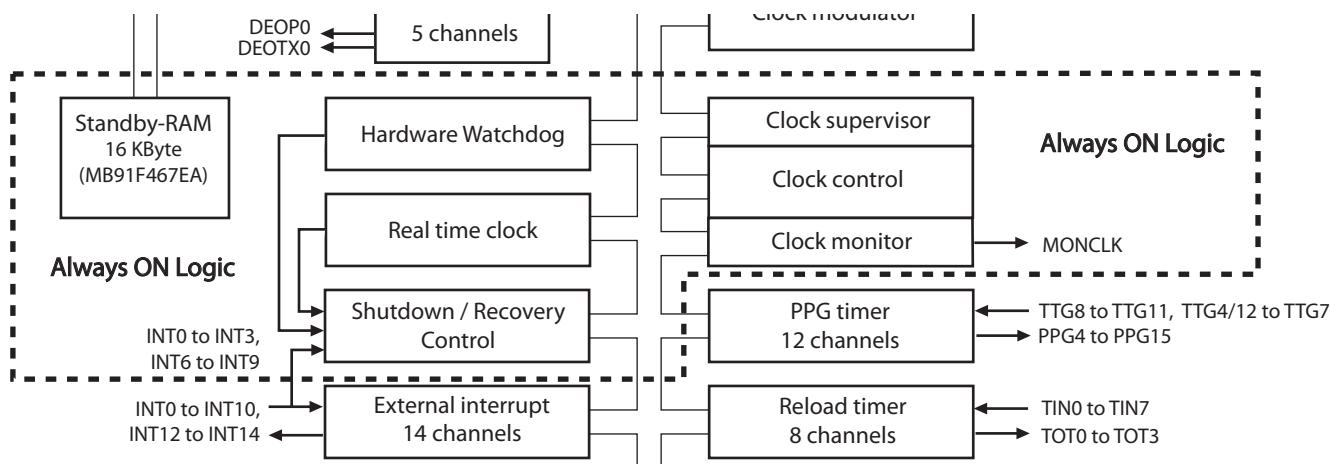
The device can enter this mode if it goes to STOP state when Shutdown is enabled.

During this mode, the oscillators can stop oscillating and the power is not supplied except for some logic.

The power continues to be supplied to the following circuits even in shutdown state:

- Standby RAM 16 KByte for data (address FFFAC000H to FFFAFFFH)
- Shutdown / recovery control circuit
- Clock control logic
- Real Time Clock
- 4 MHz oscillator + 32 kHz oscillator + RC oscillator
- Hardware Watchdog + Clock Supervisor

In the "BLOCK DIAGRAM" on page 26, this part of the device is called "Always ON Logic":



The device will recover from Shutdown mode after the following events:

- Reset assertion by the INITX pin <sup>1</sup>
- External interrupt (8 sources)
- Real Time Clock interrupt
- Hardware watchdog reset
- Main Clock Supervisor reset

1. Reset by the INITX pin will kill the ShutDown state and restart the device like at power-on.

## 2. Standby RAM

MB91F467E contains a 16 KByte low-leakage RAM used as Standby RAM. The power supply of this RAM is not switched off in Shutdown state.

The Standby RAM is located at addresses FFFAC000H to FFFAFFFH.

To access it, to the RAM must be enabled by setting RAMEN bit in SHDE register. RAMEN is initialized by Software Reset (RST). If the RAM is to be accessed, make sure that no external bus Chip Select area overlaps the Standby RAM addresses.

The bit RAMEN is written using CLKP, while the Standby RAM is accessed with CLKB. If CLKP is slower than CLKB, make sure to have some wait time (at least 2 CLKP periods) between setting of RAMEN and first RAM access.

For the Standby RAM, low-leakage macros have been implemented. Read and write acces are performed with 1 wait cycle.

## 3. Shutdown Registers

### 3.1. Notes About the Reset Signals

The following register description mentiones different reset signals, which are explained shortly here. For more information, please refer to the MB91460 series hardware manual, "Chapter 9 Reset".

- **Settings Initialization Reset (INIT):**

initializes all the device's control and clock settings. INIT can be triggered

- by low level on external INITX pin
- by low level on external HSTX pin (no hardware standby pin available in MB91460E series)
- by Hardware Watchdog Timer
- by Clock Supervisor
- by Software Watchdog Timer
- by Low Voltage Detection

- **Operation Initialization Reset (RST, "Software Reset"):**

initializes CPU and peripherals and restarts the software. RST can be triggered

- by low level on external RSTX pin (not available in MB91460E series)
- by INIT (INIT always causes RST)
- by software (STCR.SRST=0)

- **Shutdown Recovery:** The Shutdown state is released when a valid recovery factor is found. Shutdown recovery causes a Settings Initialization Reset (INIT) with some exceptions. For details, please refer to "Recovery from shutdown mode" on page 88.

# MB91460E Series

## 3.2. SHDE: Shutdown control register

This register enables/disables the shutdown state as well as the Standby RAM.

- **SHDE** : Address 0004D4H Access: Byte

7	6	5	4	3	2	1	0	
<b>SDENB</b>	-	-	-	-	-	-	<b>RAMEN</b>	
0	X	X	X	X	X	X	0	Initial value <sup>1</sup>
retained	X	X	X	X	X	X	0	Initial value <sup>2</sup>
R/W	-	-	-	-	-	-	R/W	Attribute

1. Initial value after external pin INITX=0 or Shutdown Recovery
2. Initial value after Software Reset (RST)

### [bit 7] SDENB : Shutdown enable

SDENB	Function
1	Enable shutdown state: On transition to STOP mode, the device enters Shutdown state.
0	Disable shutdown state: On transition to STOP mode, the device enters the normal STOP mode.

### [bit 6 to bit 1] Reserved bits

- The read value is undefined.
- Always write 0 to these bits.

### [bit 0] RAMEN : Standby RAM enable

RAMEN	Function
1	Enable the Standby RAM <sup>1</sup> : Read and write access to the Standby RAM is possible
0	Disable the Standby RAM: Read and write access to the Standby RAM is disabled.

1. The Standby RAM is located inside the address space of External Bus. If the Standby RAM is enabled, make sure that no chip select area of the External Bus overlaps the standby RAM area.

Note: RAMEN is cleared by INIT and by Software Reset because the chip select control registers (CSER, ACR0-7, ASR0-7, AWR0-7) are initialized by the same conditions. After both kinds of reset, chip select CS0 is enabled to cover all addresses of external bus area, which would overlap the Standby RAM address space.

Note: The bit RAMEN is written using CLKP, while the Standby RAM is accessed with CLKB. If CLKP is slower than CLKB, make sure to have some wait time (at least 2 CLKP periods) between setting of RAMEN and first RAM access.

### 3.3. EXTE: Shutdown recovery external interrupt enable register

This register enables external interrupts as the source for recovering from the shutdown state.

- **EXTE** : Address 0004D6H Access: Byte

7	6	5	4	3	2	1	0	
<b>RX1</b>	<b>RX0</b>	<b>INT7</b>	<b>INT6</b>	<b>INT3</b>	<b>INT2</b>	<b>INT1</b>	<b>INT0</b>	
0	0	0	0	0	0	0	0	Initial value <sup>1</sup>
retained	retained	retained	retained	retained	retained	retained	retained	Initial value <sup>2</sup>
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

1. Initial value after external pin INITX=0 or Shutdown Recovery
2. Initial value after Software Reset (RST)

Eight external interrupts that can be set as recovery sources are allocated to each bit, as shown in the table below:

<b>bit</b>	<b>Pin No</b>	<b>Pin Name</b>
7	93	P32_2/RX1/INT9
6	91	P23_0/RX0/INT8
5	90	P24_7/SCL3/INT7
4	89	P24_6/SDA3/INT6
3	86	P24_3/INT3
2	85	P24_2/INT2
1	84	P24_1/INT1
0	83	P24_0/INT0

#### [bit 7 to bit 0] Interrupt enable bits

<b>Value</b>	<b>Function</b>
1	Enable recovery interrupt
0	Disable recovery interrupt

- These bits can be read and written.
- External pin INITX=0 or Shutdown recovery clear these bits.

# MB91460E Series

## 3.4. SHDINT: Shutdown recovery internal interrupt control and status register

The SHDINT register contains control bits and flags for enabling and indicating internal interrupts for recovery from shutdown mode.

- **SHDINT** : Address 0004DBH Access: Byte

7	6	5	4	3	2	1	0	
-	-	-	-	<b>HWWD<sub>F</sub></b>	<b>HWWDE</b>	<b>RTCF</b>	<b>RTCE</b>	
X	X	X	X	0	0	0	0	Initial value <sup>1</sup>
X	X	X	X	retain	0	retain	0	Initial value <sup>2</sup>
X	X	X	X	retain	0	retain	retain	Initial value <sup>3</sup>
-	-	-	-	R(RM1)/ W0	R	R(RM1)/ W0	R/W	Attribute

1. Initial value after external pin INITX=0
2. Initial value after Shutdown Recovery
3. Initial value after Software Reset (RST)

### [bit 7 to bit 4] Reserved bits

- The read value is undefined.
- Always write 0 to these bits.

### [bit 3] HWWDF: Hardware Watchdog recovery flag

HWWD <sub>F</sub>	Function
1	Recovery factor from Hardware Watchdog found
0	No recovery factor from Hardware Watchdog found

- This bit is set in Shutdown mode, if HWWDE is set and if an INITX signal from Hardware Watchdog is detected.
- Writing "1" to this bit does not affect the operation.
- Writing "0" clears the bit, external pin INITX=0 clears the bit.
- "1" is read by a read-modify-write instruction.

### [bit 2] HWWDE: Hardware Watchdog recovery enable (mirror of HWWDE.STP\_RUN <sup>1</sup>)

HWWDE	Function
1	Recovery reset from Hardware Watchdog is enabled, RC clock is enabled in STOP/Shutdown mode by hardware
0	Recovery reset from Hardware Watchdog is disabled, RC clock depends on CSVCR.RCE setting in STOP/Shutdown mode

- This bit is a read-only mirror of HWWDE.STP\_RUN, which can be set only once after reset and cannot be cleared by CPU access.
- This bit is cleared by Software Reset (RST). Note that external pin INITX=0 or Shutdown recovery are always followed by a Software Reset RST.

1. STP\_RUN is bit HWWDE[4]

## [bit 1] RTCF: Real Time Clock recovery flag

RTCF	Function
1	Recovery factor from Real Time Clock found
0	No recovery factor from Real Time Clock found

- This bit is set in Shutdown mode, if RTCE is set and an interrupt signal from Real Time Clock is detected.
- Writing "1" to this bit does not affect the operation.
- Writing "0" clears the bit, external pin INITX=0 clears the bit.
- "1" is read by a read-modify-write instruction.

## [bit 0] RTCE: Real Time Clock recovery enable

RTCE	Function
1	Recovery reset from Real Time Clock is enabled
0	Recovery reset from Real Time Clock is disabled

- This bit can be read and written.
- External pin INITX=0 or Shutdown recovery clear this bit.

# MB91460E Series

## 3.5. EXTF: Shutdown recovery external interrupt source flags

This register indicates the recovery source for when a shutdown recovery external interrupt is used to recover.

- **EXTF** : Address 0004D7<sub>H</sub> Access: Byte

7	6	5	4	3	2	1	0	
<b>RX1</b>	<b>RX0</b>	<b>INT7</b>	<b>INT6</b>	<b>INT3</b>	<b>INT2</b>	<b>INT1</b>	<b>INT0</b>	
0	0	0	0	0	0	0	0	Initial value <sup>1</sup>
retained	Initial value <sup>2</sup>							
retained	Initial value <sup>3</sup>							
R(RM1)/ W0	Attribute							

1. Initial value after external pin INITX=0
2. Initial value after Shutdown Recovery
3. Initial value after Software Reset (RST)

The bit configuration is the same as for the EXTE register.

### [bit 7 to bit 0] Interrupt factor flag bits

The bit corresponding to any input signal found to be valid as a recovery factor is set to "1."

Value	Function
1	Recovery factor found
0	No recovery factor found

- These bits are set in Shutdown mode, when the attached external interrupt channel is enabled by EXTE=1 and a recovery factor (level / edge) from the external interrupt channel is detected.
- Writing "1" to these bits does not affect the operation.
- Writing "0" clears the bits, external pin INITX=0 clears the bits.
- "1" is read by a read-modify-write instruction.

### 3.6. EXTLV1/2: Shutdown recovery external interrupt level selection register

This register sets the pin level for recovering from the shutdown state using an external interrupt.

- **EXTLV1** : Address 0004D8<sub>H</sub> Access: Halfword, Byte

15	14	13	12	11	10	9	8	
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	
0	0	0	0	0	0	0	0	Initial value <sup>1</sup>
retained	Initial value <sup>2</sup>							
R/W	Attribute							

1. Initial value after external pin INITX=0 or Shutdown Recovery
2. Initial value after Software Reset (RST)

- **EXTLV2** : Address 0004D9<sub>H</sub> Access: Halfword, Byte

7	6	5	4	3	2	1	0	
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	
0	0	0	0	0	0	0	0	Initial value <sup>1</sup>
retained	Initial value <sup>2</sup>							
R/W	Attribute							

1. Initial value after external pin INITX=0 or Shutdown Recovery
2. Initial value after Software Reset (RST)

Source levels of eight external interrupts that can be set as recovery sources are allocated to each bit, as shown in the table below.

bit	Pin No	Pin Name
15,14	93	P23_2/RX1/INT9
13,12	91	P23_0/RX0/INT8
11,10	90	P24_7/SCL3/INT7C
9,8	89	P24_6/SDA3/INT6D
7,6	86	P24_3/INT3
5,4	85	P24_2/INT2
3,2	84	P24_1/INT1
1,0	83	P24_0/INT0

[bit15 to bit0]: Interrupt level setting register

LBx	LAx	Interrupt Level
0	0	"L" level (initial value)
0	1	"H" level
1	0	Rising edge
1	1	Falling edge

Please refer to "External Interrupts: Level or Edge Setting" on page 87.

## 4. Shutdown Operation

### 4.1. Transition to shutdown state

Shutdown state is a special kind of the STOP state. During Shutdown, the settings in the STCR register for Oscillation Disable (STCR.OSCD1, STCR.OSCD2), Hi-Z mode (STCR.HIZ) and Oscillation Stabilization time (STCR.OS[1:0]) are valid the same kind as in normal STOP state. At recovery from Shutdown, STCR.OS[1:0] are not cleared to maintain the oscillator stabilisation time, while STCR.OSCD1, STCR.OSCD2 and STCR.HIZ are initialized by the recovery.

For transition into Shutdown, do the following:

- Enable at least one recovery condition (otherwise, recovery is only possible by external INITX pin)
- Enable the Shutdown mode
- Switch the device to STOP mode

The details are explained below.

#### 4.1.1. Precautions

Before enabling Shutdown, consider the following:

- Data, which is needed after recovery from Shutdown, should be copied into the Standby RAM.
- The CPU should run on Main- or Sub-Oscillation, not on PLL. The PLL should be disabled.
- The Sub-Regulator can be set to 1.2V in STOP mode by setting REGSEL.SUBSEL = 0x00
- Specify the levels of external interrupt signals used for recovery in EXTLV1/2 registers
- Enable the channels of external interrupt signals for recovery in EXTE register

#### 4.1.2. Deep Shutdown Settings for maximal power saving

The following settings generate Shutdown without any activity on the device:

- Disable all pin pull-up/pull-down settings which are not required, or set the STCR.HIZ<sup>1</sup> bit when going to STOP.
- Set external bus pins to port mode / input direction (otherwise some pins will output constant values, see "I/O Behaviour in Shutdown" on page 91).
- Don't set Hardware Watchdog Run in STOP mode (HWWDE.STP\_RUN<sup>2</sup> =0, this is default setting)
- Disable the RC oscillator in STOP mode (CSVCR.RCE=0)
- Disable the Low Voltage Detection in STOP mode (LVDET.LVEPD=1, LVDET.LVIPD=1)
- Disable the Main and the Sub oscillators in STOP mode (STCR.OSCD1=1, STCR.OSCD2=1)
- Set the Shutdown Enable bit SHDE.SDENB=1 to enable shutdown mode
- Go to STOP: set the STOP request STCR.STOP=1 and read back STCR two times.

---

1. With STCR.HIZ=1, all pull-ups and pull-downs are disabled in STOP/Shutdown.
2. STP\_RUN is bit [4] of HWWDE register. It enables running the Hardware Watchdog in STOP mode. STP\_RUN can only be set by software, but not cleared. STP\_RUN is cleared by INIT.

### 4.1.3. Shutdown with Real Time Clock running

The following settings generate Shutdown with the RTC running on Main-Oscillation, Sub-Oscillation or RC clock, and with recovery by RTC enabled:

- Set the RTC prescaler values depending on the clock speed (WTBR register)
- If recovery by the RTC is needed:
  - Enable at least one of the the RTC interrupts (half-second, second, minute, hour or day) in WTCR and/or WTCE register
  - Enable RTC recovery: set SHDINT.RTCE=1
- If RTC uses Main Oscillation:
  - Disable the RC oscillator in STOP mode (CSVCR.RCE=0)
  - Disable the Sub oscillator in STOP mode (STCR.OSCD2=1) and keep Main oscillator running (OSCD1=0)
  - The RTC is connected to Main oscillation by default.
- If RTC uses Sub Oscillation:
  - Disable the RC oscillator in STOP mode (CSVCR.RCE=0)
  - Disable the Main oscillator in STOP mode (STCR.OSCD1=1) and keep Sub oscillator running (OSCD2=0)
  - Connect the RTC to Sub oscillator: set CSCFG.CSC[1:0]=01
- If RTC uses RC clock:
  - Enable the RC oscillator in STOP mode (CSVCR.RCE=1, this is default setting)
  - Disable the Main and the Sub oscillators in STOP mode (STCR.OSCD1=1, STCR.OSCD2=1)
  - Connect the RTC to RC oscillator: set CSCFG.CSC[1:0]=10
- Set the Shutdown Enable bit SHDE.SDENB=1 to enable shutdown mode
- Go to STOP: set the STOP request STCR.STOP=1 and read back STCR two times.

### 4.1.4. Hardware Watchdog in Shutdown

The Hardware Watchdog can run in STOP mode, if the bit HWWDE.STP\_RUN<sup>1</sup> is set.

- Outside STOP mode, the Hardware Watchdog timeout will send an INIT signal to the CPU via the Shutdown control.
- In STOP mode without Shutdown, the Hardware Watchdog timeout will send an INIT signal to the CPU via the (inactive) Shutdown control, which cancelles the STOP mode immediately.
- In STOP mode with Shutdown enabled, the Hardware Watchdog timeout will set the SHDINT.HWWDF flag, causing a recovery from Shutdown.

The Hardware Watchdog can be enabled in Shutdown state like follows:

- Enable the Hardware Watchdog operation in STOP mode: set HWWDE.STP\_RUN = 1  
In parallel, this enables the RC oscillator by hardware, and the Hardware Watchdog recovery Enable bit SHDINT.HWWDE is set by hardware too.
- If RTC is needed, enable it like described in 4.1.3. Shutdown with Real Time Clock running above.
- Specify the levels of external interrupt signals used for recovery in EXTLV1/2 registers
- Enable the channels of external interrupt signals for recovery in EXTE register
- Set the Shutdown Enable bit SHDE.SDENB=1 to enable shutdown mode
- Clear/restart the Hardware Watchdog: write 0 to bit HWWD.CL
- Go to STOP: set the STOP request STCR.STOP=1 and read back STCR two times.

---

1. STP\_RUN is bit [4] of HWWDE register. It enables running the Hardware Watchdog in STOP mode. STP\_RUN can only be set by software, but not cleared. STP\_RUN is cleared by INIT.

# MB91460E Series

If the timeout is reached, the Hardware Watchdog generates INIT, which cancels the Shutdown state and forces recovery. The CPU will run on Main Oscillation after this recovery.

**WARNING:** If a Hardware Watchdog timeout INIT signal appears just at the transition to Standby Mode, the device may enter an unpredictable state. Always make sure that the hardware Watchdog has been cleared just before entering Shutdown.

## 4.1.5. Clock Supervisor in Shutdown

The INITX pin, Clock Supervisor and Hardware Watchdog form the “external INIT chain”, like shown in the figure in section “Determining the Reset Source after Shutdown” on page 89. The Shutdown control is part of this chain.

An INIT signal from the Clock Supervisor will pass the Hardware Watchdog and arrive at the same Shutdown control input line as the INIT signal from Hardware Watchdog. Therefore, clock supervision in Shutdown mode is only possible if the Hardware Watchdog is operating in parallel.

If the Hardware Watchdog is disabled in Shutdown mode, an INIT signal from the Clock Supervisor is ignored in Shutdown.

The Clock Supervisor is enabled by default. In Shutdown mode, as long as the Main- and/or Sub-oscillator is running and the RC clock is not stopped, the CSV is supervising the Main- or Sub-oscillator, respectively.

- The Clock Supervisor needs the RC clock, so set CSVCR.RCE=1, this is default setting.
- If the Main-oscillator is not stopped (STCR.OSCD1=0), the Main clock supervisor is running.
- If the Main-oscillator fails, the Main Clock Supervisor generates INIT, which can cancel the Shutdown state and force recovery. The CPU runs on RC clock during and after the recovery.
- If the Sub-oscillator is not stopped (STCR.OSCD2=0), the Sub Clock Supervisor is running.
- If the Sub-oscillator fails, the Sub clock is switched to RC clock divided by 2. An INIT is not generated, and the Real Time Clock continues running on on RC clock divided by 2, if RTC is enabled.

To disable the Clock Supervisor, clear the bits CSVCR.MSVE and CSVCR.SSVE.

## 4.1.6. Low Voltage Detection in Shutdown

Low Voltage Detection is not supported in Shutdown mode. Always set the Low Voltage Detection into power down mode (LVDET.LVEPD=1, LVDET.LVIPD=1) before enabling Shutdown.

## 4.1.7. External Interrupts: Input Voltage Setting

The input voltages (CMOS-Schmitt, Automotive, TTL, CMOS-2) of the external interrupt lines are defined by the setting of PILR and EPILR of the appropriate ports. The PILR and EPILR settings for the 8 external recovery interrupt lines are maintained during Shutdown mode until they are cleared by the Software reset following the Recovery INIT.

EPILR	PILR	Pin No	Pin Name
EPILR23[2]	PILR23[2]	93	P23_2/RX1/INT9
EPILR23[0]	PILR23[0]	91	P23_0/RX0/INT8
EPILR24[7]	PILR24[7]	90	P24_7/SCL3/INT7C
EPILR24[6]	PILR24[6]	89	P24_6/SDA3/INT6D
EPILR24[3]	PILR24[3]	86	P24_3/INT3
EPILR24[2]	PILR24[2]	85	P24_2/INT2
EPILR24[1]	PILR24[1]	84	P24_1/INT1
EPILR24[0]	PILR24[0]	83	P24_0/INT0

#### 4.1.8. External Interrupts: Level or Edge Setting

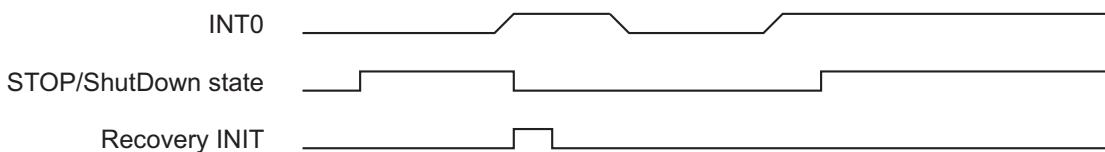
The registers EXTLV1 and EXTLV2 are used to set the interrupt level or edge for recovery per interrupt channel.

LBx	LAx	Interrupt Level
0	0	"L" level (initial value)
0	1	"H" level
1	0	Rising edge
1	1	Falling edge

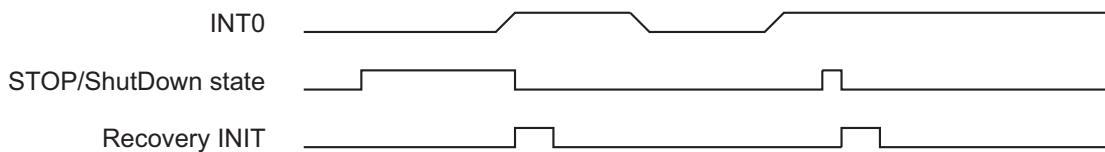
The settings "level" and "edge" generate different behaviour if the external source line is not changed back after recovery or if it changes to the sensitive level before Shutdown.

Examples:

- INT0 is enabled for recovery on **rising edge**. If a rising edge appears during Shutdown state, recovery is performed. If a rising edge is outside Shutdown state, there will be no recovery:



- INT0 is enabled for recovery on **high level**. If INT0 changes to high level during Shutdown state, recovery is performed. If INT0 changes to high level already before Shutdown state, the Shutdown is recovered immediately because the high level on INT0 is valid. Note that, in this case, a complete shut-down/power-up sequence with recovery INIT is performed:



Note: If "H" level or "L" level is enabled for recovery, the level must be active for minimum 500  $\mu$ s.

## 4.2. Recovery from shutdown mode

The following factors are available to recover from the shutdown state:

- Assert the reset signal at the INITX terminal for minimum 10 ms <sup>1 2</sup>
- Input of a valid recovery request via an external interrupt terminal
- Real Ttime Clock Interrupt (when RTC interrupt is enabled)
- Hardware Watchdog reset (when HWWD is enabled in STOP mode)
- Main Clock Supervisor reset (when Main oscillator is running and Main Clock Supervisor is enabled and recovery by HWWD is enabled)

Shutdown state is released when a valid recovery factor is permitted. After the Shutdown state release, the device restarts with a settings initialization reset (INIT), just like power-up operation. Only the Real Time Clock, the Oscillation Stabilization settings in STCR register, and the recovery source flags in the Shutdown registers EXTF and SHDINT are not cleared.

The internal restart sequence is as follows:

1. Resume the internal power supply.
2. Reset and assert the initialization reset (INIT).
3. Wait for oscillation stabilization.
4. Start the reset sequence.

As the external interrupt source flags and the RTC flag are retained in EXTF and SHDINT registers, it is possible to determine whether it is power-up operation or recovery from shutdown state by checking the flags.

### 4.2.1. The Real Time Clock at Recovery from Shutdown

In normal operation, the registers and settings of the Real Time Clock are initialized by Software Reset (RST).

At recovery from Shutdown, the RTC is **not** initialized:

- The prescaler, second, minute and hour counters continue counting also during the recovery INIT state.
- The clock selection for the RTC (by CSCFG.OSC1, CSCFG.OSC0) remains unchanged.
- The RTC interrupt enable bits and interrupt flags (in WTCR and WTCE registers) remain unchanged.

So at each recovery from Shutdown, the RTC continues running and the current time as well as the interrupt flags can be read from the RTC after recovery.

Note: The Interrupt Control Register for RTC (ICR58), the Interrupt Level Mask (ILM) register as well as the Condition Code Register (CCR, containing the I-Flag) are cleared by the recovery INIT, so that all interrupt processing is disabled.

If the software re-enables interrupt processing by setting ICR58, ILM and I-Flag, the software will process the pending RTC interrupt immediately.

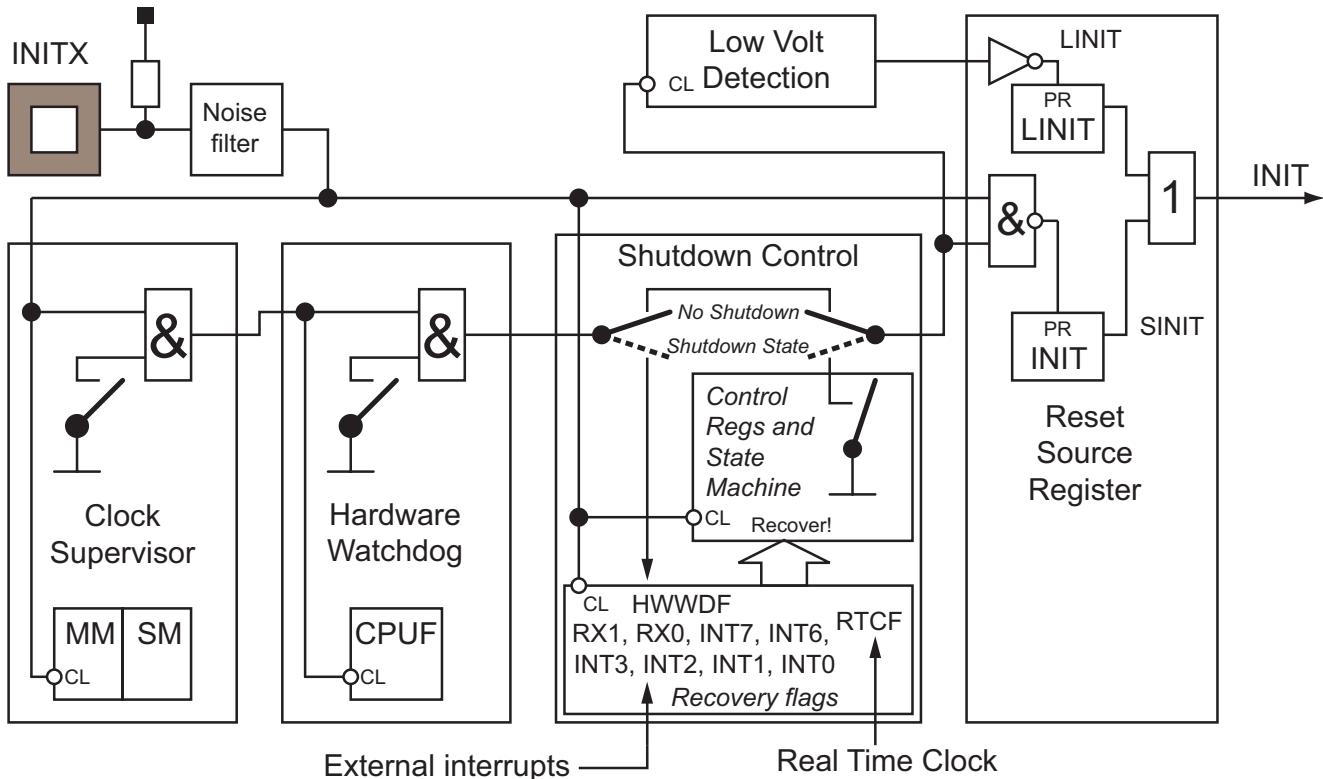
---

1. The minimum INTX=0 pulse length is determined by the time the main oscillator needs for stabilization.
2. Reset by INITX=0 will kill the ShutDown state and restart the device like at power-on.

### 4.3. Determining the Reset Source after Shutdown

The recovery from Shutdown is followed by an Setting Initialization Reset (INIT). Because INIT is always followed by a Software Reset (RST), the CPU fetches the Mode- and Reset-Vectors and jumps to the Reset Vector, which is located in the Boot ROM.

The following drawing shows how the Shutdown Control is located in the external INIT chain:



The following table lists the registers and flags for determination of the reset source, including Shutdown:

Register	Addr.	7	6	5	4	3	2	1	0
<b>RSRR</b>	<b>480<sub>H</sub></b> <sup>1</sup>	<b>INIT</b>	<b>HSTB</b>	<b>WDOG</b>	<b>ERST</b>	<b>SRST</b>	<b>LINIT</b>	<b>WT1</b>	<b>WT0</b>
<b>EXTF</b>	<b>4D7<sub>H</sub></b>	<b>RX1</b>	<b>RX0</b>	<b>INT7</b>	<b>INT6</b>	<b>INT3</b>	<b>INT2</b>	<b>INT1</b>	<b>INT0</b>
<b>SHDINT</b>	<b>4DB<sub>H</sub></b>	-	-	-	-	<b>HWWDF</b>	<b>HWWDE</b>	<b>RTCF</b>	<b>RTCE</b>
<b>CSVCR</b>	<b>4AD<sub>H</sub></b>	<b>SCKS</b>	<b>MM</b>	<b>SM</b>	<b>RCE</b>	<b>MSVE</b>	<b>SSVE</b>	<b>SRST</b>	<b>OUTE</b>
<b>HWWD</b>	<b>4C7<sub>H</sub></b>	-	-	-	-	<b>CL</b>	-	-	<b>CPUF</b>

1. RSRR is read and cleared by the Boot ROM software. After Boot ROM, the content of RSRR can be found in CPU register R4[7:0] and in a variable in memory.

Note: RSRR: Reset Source register

EXTF: External shutdown recovery flags, see page 82

SHDINT: Hardware Watchdog/ Real Time Clock recovery flags, see page 80

CSVCR: Clock Supervisor Control / Status register

HWWD: Hardware Watchdog register

For details about RSRR, CSVCR and HWWD, please refer to the hardware manual.

Recovery from Shutdown will set the INIT bit in RSRR register. Because the INIT bit can also be set by external INIT (low level at INITX pin), Clock Supervisor or Hardware Watchdog, the flags in EXTF, SHDINT, CSVCR and HWWD should be checked for determining the reset source.

# MB91460E Series

The recovery flags in EXTF and SHDINT are set **only** in Shutdown mode and **only** if recovery by this channel is enabled.

## 4.4. Registers which are not initialized by Shutdown Recovery

As described above, recovery from Shutdown performs a settings initialization reset (INIT) followed by software reset (RST). This sequence will initialize the complete device with some exceptions, explained in the following table.

Registers which are not initialized by Shutdown Recovery:

Register	Address	non-initialized Bits	Reason
STCR	481 <sub>H</sub>	OS1, OS0	Keep oscillation stabilization time setting
CSVCR	4AD <sub>H</sub>	all bits	Clock Supervisor is not initialized by recovery
CSCFG	4AE <sub>H</sub>	all bits	Keep RTC and Calibration clock source settings
CMCFG	4AF <sub>H</sub>	all bits	Keep Clock Monitor settings
WTCER	4A1 <sub>H</sub>		
WTCR	4A2 <sub>H</sub> - 4A3 <sub>H</sub>		
WTBR	4A5 <sub>H</sub> - 4A7 <sub>H</sub>		
WTHR	4A8 <sub>H</sub>		
WTMR	4A9 <sub>H</sub>		
WTSR	4AA <sub>H</sub>		
CUCR	4B0 <sub>H</sub> - 4B1 <sub>H</sub>		
CUTD	4B2 <sub>H</sub> - 4B3 <sub>H</sub>		
CUTR1	4B4 <sub>H</sub> - 4B5 <sub>H</sub>		
CUTR2	4B6 <sub>H</sub> - 4B7 <sub>H</sub>		
HWWDE	4C6 <sub>H</sub>	all bits	
HWWD	4C7 <sub>H</sub>	all bits	
EXTF	4D7 <sub>H</sub>	all bits	Keep external recovery flags
SHDINT	4DB <sub>H</sub>	HWWDF, RTCF	Keep hardware watchdog and RTC recovery flags

Note: If the ShutDown state is killed by external pin INITX=0, these registers are initialized like at normal power-on.

## 4.5. I/O Behaviour in Shutdown

During Shutdown mode, the I/O pins are switched into dedicated states:

Ports/Pins	Port function	Setting
P00_0 to P00_7, P01_0 to P01_7, P02_0 to P02_7, P03_0 to P03_7.	D[31:0]	External bus data I/O The pins are switched to input direction, but it is not possible to input signals on these pins.
P08_6, P08_7, P10_5, P13_0	BRQ, RDY, MCLKI, DREQ0	External bus control inputs If STCR.HIZ (HiZ mode in STOP) is not set, the pull-up/pull-down settings are maintained during shutdown.
P04_0 to P04_1, P05_0 to P05_7, P06_0 to P06_7, P07_0 to P07_7.	A[25:0]	External bus address outputs If STCR.HIZ is set, the pull-up and pull-down resistors are disabled.
P08_0 to P08_5, P09_0 to P09_7, P10_1 to P10_4, P10_6, P13_1, P13_2	WRnX, RDX, BGRNTX, CSnX, ASX, BAAX, WEX, MCLKO, MCLKE	External bus control and clock outputs If the pins were switched to output direction before shutdown (by PFR==1 or DDR==1), the pins will output '1' value and the driver strength is switched to 2 mA. Otherwise, the pins keep input direction, but it is not possible to input signals on these pins. If STCR.HIZ is not set, the pull-up/pull-down settings are maintained. If STCR.HIZ is set, the pull-up and pull-down resistors are disabled.
P24_0 to P24_3, P24_6, P24_7, P23_0, P23_2	INT0 to INT3, INT6, INT7, RX0/INT8, RX1/INT9	Pins used for Shutdown recovery The pins are switched to input direction. If STCR.HIZ is not set, the pull-up/pull-down settings are maintained during shutdown. If STCR.HIZ is set, the pull-up and pull-down resistors are disabled. If external interrupt is enabled for recovery from Shutdown (Shutdown INTE=1), the input threshold setting (PILR, EPILR) is maintained during the shutdown mode and it is possible to input signals for recovery. After the first recovery factor is accepted, the port settings are initialized when the device proceeds to the reset (INIT/RST) sequence.
Pnn_m <sup>1</sup>	all other Ports not mentioned above	All other pins are switched to input direction, but it is not possible to input signals on these pins. If STCR.HIZ is not set, the pull-up/pull-down settings are maintained during Shutdown. If STCR.HIZ is set, the pull-up and pull-down resistors are disabled.
ALARM_0	ALARM analog input	The state of ALARM input is not changed in Shutdown state.
MD_0 to MD_2	Mode inputs	The state of MD[2:0] is not changed in Shutdown state
INITX	External INIT	The state of INITX is not changed in Shutdown state. The pull-up is enabled. It is possible to input external INITX signal during Shutdown.
VCC18C	Regulator capacitor pin	The capacitor connection pin for internal regulator shows the voltage which is applied to internal Always-ON domain.

1. nn = 14 to 29, m = 0 to 7

# MB91460E Series

## ■ CPU AND CONTROL UNIT

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

### 1. Features

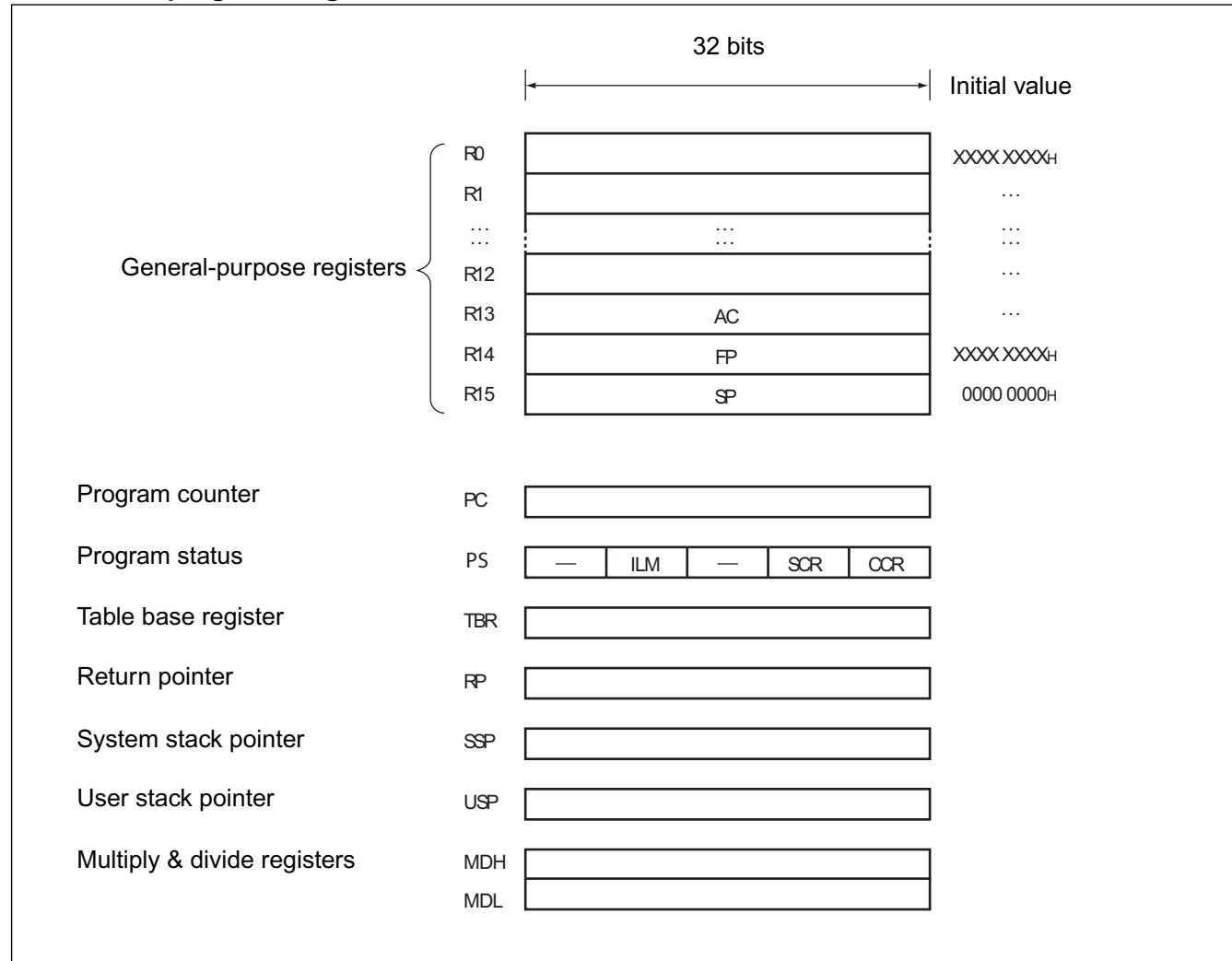
- Adoption of RISC architecture
  - Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  - 32-bit 32-bit multiplication: 5 cycles
  - 16-bit 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  - Quick response speed (6 cycles)
  - Multiple-interrupt support
  - Level mask function (16 levels)
- Enhanced instructions for I/O operation
  - Memory-to-memory transfer instruction
  - Bit processing instruction
  - Basic instruction word length: 16 bits
- Low-power consumption
  - Sleep mode/stop mode

### 2. Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

### 3. Programming model

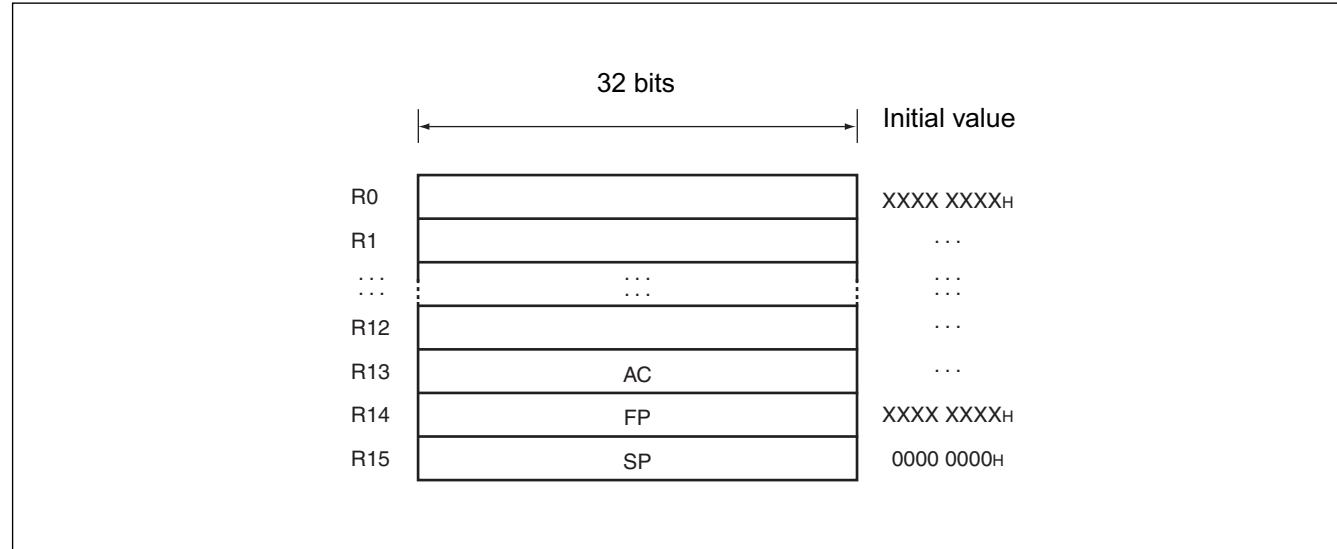
#### 3.1. Basic programming model



# MB91460E Series

## 4. Registers

### 4.1. General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

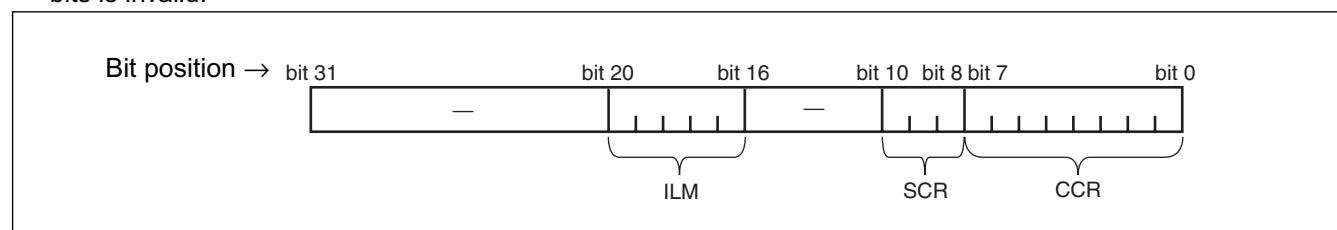
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000H (SSP value).

### 4.2. PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always "0". Write access to these bits is invalid.



## 4.3. CCR (Condition Code Register)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
—	SV	S	I	N	Z	V	C	- 000XXXXB

SV : Supervisor flag

S : Stack flag

I : Interrupt enable flag

N : Negative enable flag

Z : Zero flag

V : Overflow flag

C : Carry flag

## 4.4. SCR (System Condition Register)

bit 10	bit 9	bit 8	Initial value
D1	D0	T	XX0B

Flag for step division (D1, D0)

This flag stores interim data during execution of step division.

Step trace trap flag (T)

This flag indicates whether the step trace trap is enabled or disabled.

The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

## 4.5. ILM (Interrupt Level Mask register)

bit 20	bit 19	bit 18	bit 17	bit 16	Initial value
ILM4	ILM3	ILM2	ILM1	ILM0	01111B

This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value “01111B” at reset.

## 4.6. PC (Program Counter)

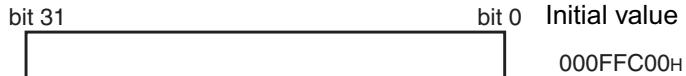
bit 31	bit 0	Initial value
		XXXXXXXXH

The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

# MB91460E Series

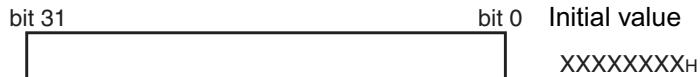
## 4.7. TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is 000FFC00H.

## 4.8. RP (Return Pointer)



The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

## 4.9. USP (User Stack Pointer)



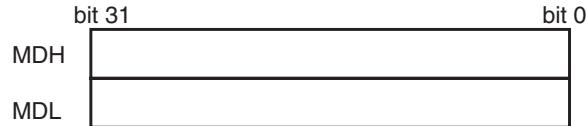
The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.

The initial value at reset is undefined.

- This register cannot be used with RETI instructions.

## 4.10. Multiply & divide registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

## ■ EMBEDDED PROGRAM/DATA MEMORY (FLASH)

### 1. Flash features

- MB91F467EA: 1088 Kbytes ( $16 \times 64$  Kbytes +  $8 \times 8$  Kbytes) = 8.5 Mbits
- Programmable wait state for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

### 2. Operation modes

(1) 64-bit CPU mode:

- CPU reads and executes programs in word (32-bit) length units.
- Flash writing is not possible.
- Actual Flash Memory access is performed in d-word (64-bit) length units.

(2) 32-bit CPU mode :

- CPU reads, writes and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

(3) 16-bit CPU mode :

- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in half-word (16-bit) length units.

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 "Flash Access Mode Switching".

# MB91460E Series

### 3. Flash access in CPU mode

#### 3.1. Flash configuration

##### 3.1.1. Flash memory map MB91F467EA

Address								
0014:FFFFh	SA6 (8KB)		SA7 (8KB)					
0014:C000h								
0014:BFFFh	SA4 (8KB)		SA5 (8KB)					
0014:8000h								
0014:7FFFh	SA2 (8KB)		SA3 (8KB)					
0014:4000h								
0014:3FFFh	SA0 (8KB)		SA1 (8KB)					
0014:0000h								
0013:FFFFh	SA22 (64KB)		SA23 (64KB)					
0012:0000h								
0011:FFFFh	SA20 (64KB)		SA21 (64KB)					
0010:0000h								
000F:FFFFh	SA18 (64KB)		SA19 (64KB)					
000E:0000h								
000D:FFFFh	SA16 (64KB)		SA17 (64KB)					
000C:0000h								
000B:FFFFh	SA14 (64KB)		SA15 (64KB)					
000A:0000h								
0009:FFFFh	SA12 (64KB)		SA13 (64KB)					
0008:0000h								
0007:FFFFh	SA10 (64KB)		SA11 (64KB)					
0006:0000h								
0005:FFFFh	SA8 (64KB)		SA9 (64KB)					
0004:0000h								
16bit read/write	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7
32bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]	
64bit read		dat[31:0]			dat[31:0]			
			dat[63:0]					

## 3.2. Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

### 3.2.1. Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 80 MHz	1	1	3	-	4	

### 3.2.2. Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 32 MHz	1	-	-	0	4	
to 48 MHz	1	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 80 MHz	1	-	-	0	7	

### 3.3. Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

#### 3.3.1. Address mapping MB91F467EA

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h + 00:2000h
04:0000h to 13:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 13:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h + 01:0000h

Note: FA result is without 20:0000h offset for parallel Flash programming .

Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

:

## 4. Parallel Flash programming mode

### 4.1. Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):

MB91F467EA

FA[21:0]	
003F:FFFFh 003F:0000h	SA23 (64KB)
003E:FFFFh 003E:0000h	SA22 (64KB)
003D:FFFFh 003D:0000h	SA21 (64KB)
003C:FFFFh 003C:0000h	SA20 (64KB)
003B:FFFFh 003B:0000h	SA19 (64KB)
003A:FFFFh 003A:0000h	SA18 (64KB)
0039:FFFFh 0039:0000h	SA17 (64KB)
0038:FFFFh 0038:0000h	SA16 (64KB)
0037:FFFFh 0037:0000h	SA15 (64KB)
0036:FFFFh 0036:0000h	SA14 (64KB)
0035:FFFFh 0035:0000h	SA13 (64KB)
0034:FFFFh 0034:0000h	SA12 (64KB)
0033:FFFFh 0033:0000h	SA11 (64KB)
0032:FFFFh 0032:0000h	SA10 (64KB)
0031:FFFFh 0031:0000h	SA9 (64KB)
0030:FFFFh 0030:0000h	SA8 (64KB)
002F:FFFFh 002F:E000h	SA7 (8KB)
002F:DFFFh 002F:C000h	SA6 (8KB)
002F:BFFFh 002F:A000h	SA5 (8KB)
002F:9FFFh 002F:8000h	SA4 (8KB)
002F:7FFFh 002F:6000h	SA3 (8KB)
002F:5FFFh 002F:4000h	SA2 (8KB)
002F:3FFFh 002F:2000h	SA1 (8KB)
002F:1FFFh 002F:0000h	SA0 (8KB)
FA[1:0]=00	FA[1:0]=10
DQ[15:0]	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[21] = 1

# MB91460E Series

## 4.2. Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to General Purpose Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	MB91F467EA external pins			Comment
		Flash memory mode	Normal function	Pin number	
—	INITX	—	INITX	73	
RESET	—	FRSTX	P09_6	60	
—	—	MD_2	MD_2	70	Set to '1'
—	—	MD_1	MD_1	71	Set to '1'
—	—	MD_0	MD_0	72	Set to '1'
RY/BY	FMCS:RDY bit	RY/BYX	P09_0	56	
BYTE	Internally fixed to 'H'	BYTEX	P09_2	58	
WE	Internal control signal + control via interface circuit	WEX	P13_2	191	
OE		OEX	P13_1	190	
CE		CEX	P13_0	189	
—		ATDIN	P25_7	187	Set to '0'
—		EQIN	P25_6	186	Set to '0'
—		TESTX	P09_3	59	Set to '1'
—		RDYI	P09_1	57	Set to '0'
A-1	Internal address bus	FA0	P25_5	185	Set to '0'
A0 to A3		FA1 to FA4	P27_0 to P27_3	158 to 161	
A4 to A7		FA5 to FA8	P27_4 to P27_7	164 to 167	
A8 to A11		FA9 to FA12	P26_0 to P26_3	168 to 171	
A12 to A15		FA13 to FA16	P26_4 to P26_7	174 to 177	
A16 to A19		FA17 to FA20	P25_0 to P25_3	178 to 181	
—		FA21	P25_4	184	Set to '1'
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	P03_0 to P03_7	192 to 199	
DQ8 to DQ15		DQ8 to DQ15	P02_0 to P02_7	200 to 207	

## 5. Poweron Sequence in parallel programming mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

## 6. Flash Security

### 6.1. Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000      BSV1: 0x14:8004  
FSV2: 0x14:8008      BSV2: 0x14:800C

### 6.2. Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

#### 6.2.1. FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to "0"	set to "0"	set to "0"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000")
set all to "0"	set to "0"	set to "1"	set to "0"	Write Protection (all device modes, without exception)
set all to "0"	set to "0"	set to "1"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000") and Write Protection (all device modes)
set all to "0"	set to "1"	set to "0"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000")
set all to "0"	set to "1"	set to "1"	set to "0"	Write Protection (all device modes, except INTVEC mode MD[2:0] = "000")
set all to "0"	set to "1"	set to "1"	set to "1"	Read Protection (all device modes, except INTVEC mode MD[2:0] = "000") and Write Protection (all device modes except INTVEC mode MD[2:0] = "000")

# MB91460E Series

## 6.2.2. FSV1 (bit15 to bit0)

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1 [15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0	set to "0"	set to "1"	
FSV1[1]	SA1	set to "0"	set to "1"	
FSV1[2]	SA2	set to "0"	set to "1"	
FSV1[3]	SA3	set to "0"	set to "1"	
FSV1[4]	SA4	set to "0"	—	Write protection is mandatory!
FSV1[5]	SA5	set to "0"	set to "1"	
FSV1[6]	SA6	set to "0"	set to "1"	
FSV1[7]	SA7	set to "0"	set to "1"	
FSV1[8]	—	set to "0"	set to "1"	not available
FSV1[9]	—	set to "0"	set to "1"	not available
FSV1[10]	—	set to "0"	set to "1"	not available
FSV1[11]	—	set to "0"	set to "1"	not available
FSV1[12]	—	set to "0"	set to "1"	not available
FSV1[13]	—	set to "0"	set to "1"	not available
FSV1[14]	—	set to "0"	set to "1"	not available
FSV1[15]	—	set to "0"	set to "1"	not available

Note : It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.

See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

### 6.3. Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 Kbytes sectors. It is only evaluated if write protection bit FSV1 [17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to "0"	set to "1"	
FSV2[1]	SA9	set to "0"	set to "1"	
FSV2[2]	SA10	set to "0"	set to "1"	
FSV2[3]	SA11	set to "0"	set to "1"	
FSV2[4]	SA12	set to "0"	set to "1"	
FSV2[5]	SA13	set to "0"	set to "1"	
FSV2[6]	SA14	set to "0"	set to "1"	
FSV2[7]	SA15	set to "0"	set to "1"	
FSV2[8]	SA16	set to "0"	set to "1"	
FSV2[9]	SA17	set to "0"	set to "1"	
FSV2[10]	SA18	set to "0"	set to "1"	
FSV2[11]	SA19	set to "0"	set to "1"	
FSV2[12]	SA20	set to "0"	set to "1"	
FSV2[13]	SA21	set to "0"	set to "1"	
FSV2[14]	SA22	set to "0"	set to "1"	
FSV2[15]	SA23	set to "0"	set to "1"	
FSV2[31:16]	—	set to "0"	set to "1"	not available

Note : See section "Flash access in CPU mode" for an overview about the sector organisation of the Flash Memory.

## ■ MEMORY SPACE

The FR family has 4 Gbytes of logical address space ( $2^{32}$  addresses) available to the CPU by linear access.

- Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access :  $000_{\text{H}}$  to  $0FF_{\text{H}}$

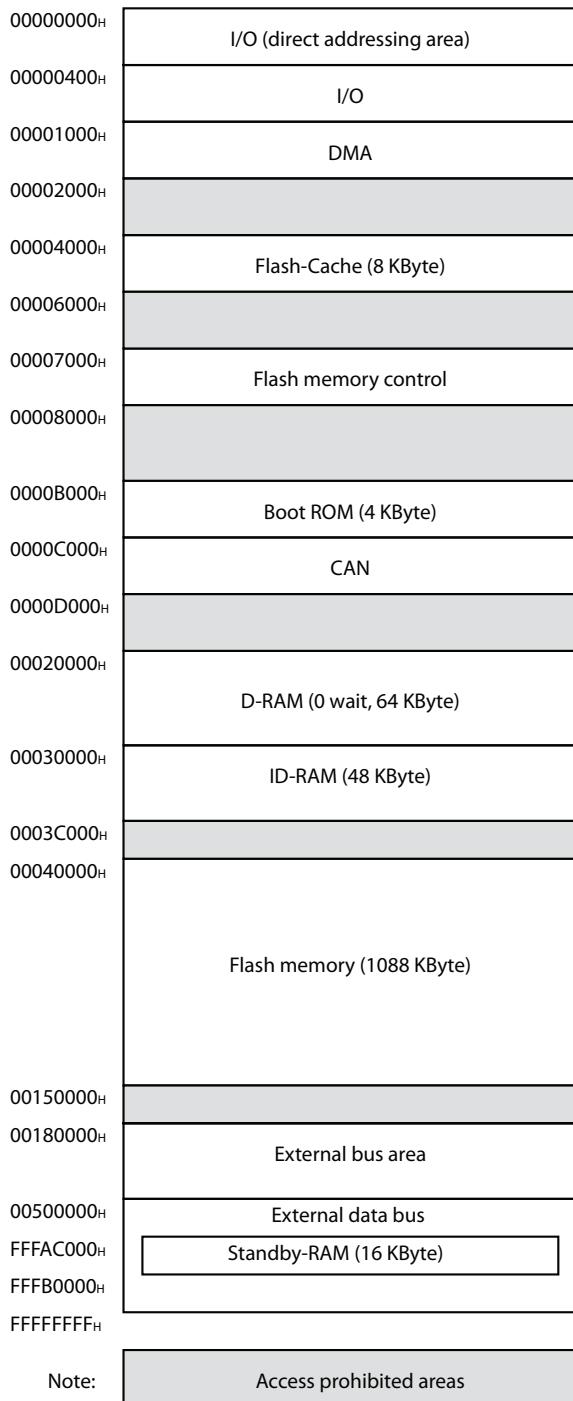
Half word access :  $000_{\text{H}}$  to  $1FF_{\text{H}}$

Word data access :  $000_{\text{H}}$  to  $3FF_{\text{H}}$

## ■ MEMORY MAPS

### 1. MB91F467EA

MB91F467EA



# MB91460E Series

## ■ I/O MAP

### 1. MB91F467EA

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR0 [R/W] XXXXXXXXXX	PDR1 [R/W] XXXXXXXXXX	PDR2 [R/W] XXXXXXXXXX	PDR3 [R/W] XXXXXXXXXX	T-unit port data register

Read/write attribute

Register initial value after reset

Register name (column 1 register at address 4n, column 2 register at address 4n + 1...)

Leftmost register address (for word access, the register in column 1 becomes the MSB side of the data.)

Note : Initial values of register bits are represented as follows:

- “ 1 ” : Initial value “ 1 ”
- “ 0 ” : Initial value “ 0 ”
- “ X ” : Initial value “ undefined ”
- “ - ” : No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000 <sub>H</sub>	PDR00 [R/W] XXXXXXXXXX	PDR01 [R/W] XXXXXXXXXX	PDR02 [R/W] XXXXXXXXXX	PDR03 [R/W] XXXXXXXXXX	R-bus Port Data Register
000004 <sub>H</sub>	PDR04 [R/W] ----- XX	PDR05 [R/W] XXXXXXXXXX	PDR06 [R/W] XXXXXXXXXX	PDR07 [R/W] XXXXXXXXXX	
000008 <sub>H</sub>	PDR08 [R/W] XXXXXXXXXX	PDR09 [R/W] XX - XXXX	PDR10 [R/W] - XXXXXX -	Reserved	
00000C <sub>H</sub>	Reserved	PDR13 [R/W] ---- XXX	PDR14 [R/W] XXXXXXXXXX	PDR15 [R/W] ---- XXXX	
000010 <sub>H</sub>	PDR16 [R/W] XXXXXXXXXX	PDR17 [R/W] XXXX ----	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014 <sub>H</sub>	PDR20 [R/W] ---- XXX	Reserved	PDR22 [R/W] -- XX - X - X	PDR23 [R/W] -- XXXXXX	
000018 <sub>H</sub>	PDR24 [R/W] XXXXXXXXXX	PDR25 [R/W] XXXXXXXXXX	PDR26 [R/W] XXXXXXXXXX	PDR27 [R/W] XXXXXXXXXX	
00001C <sub>H</sub>	Reserved	PDR29 [R/W] XXXXXXXXXX	Reserved		
000020 <sub>H</sub> to 00002C <sub>H</sub>	Reserved				Reserved
000030 <sub>H</sub>	EIRR0 [R/W] XXXXXXXXXX	ENIRO [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034 <sub>H</sub>	EIRR1 [R/W] XXXXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 10, INT 12 to INT 14)
000038 <sub>H</sub>	DICR [R/W] ----- 0	HRCL [R/W] 0 -- 11111	Reserved		Delay Interrupt
00003C <sub>H</sub> to 00004C <sub>H</sub>	Reserved				Reserved
000050 <sub>H</sub>	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054 <sub>H</sub>	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] -00000XX	FSR02 [RW/R] xx00 0000	Reserved	
000058 <sub>H</sub> , 00005C <sub>H</sub>	Reserved				Reserved

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000060 <sub>H</sub>	SCR04 [R/W, W] 00000000	SMR04 [R/W, W] 00000000	SSR04 [R/W, R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064 <sub>H</sub>	ESCR04 [R/W] 00000X00	ECCR04 [R/W, R, W] -00000XX	FSR04 [RW/R] xx00 0000	FCR04 [R/W] 0001 - 000	
000068 <sub>H</sub>	SCR05 [R/W, W] 00000000	SMR05 [R/W, W] 00000000	SSR05 [R/W, R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
00006C <sub>H</sub>	ESCR05 [R/W] 00000X00	ECCR05 [R/W, R, W] -00000XX	FSR05 [RW/R] xx00 0000	FCR05 [R/W] 0001 - 000	
000070 <sub>H</sub>	SCR06 [R/W, W] 00000000	SMR06 [R/W, W] 00000000	SSR06 [R/W, R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074 <sub>H</sub>	ESCR06 [R/W] 00000X00	ECCR06 [R/W, R, W] -00000XX	FSR06 [RW/R] xx00 0000	FCR06 [R/W] 0001 - 000	
000078 <sub>H</sub>	SCR07 [R/W, W] 00000000	SMR07 [R/W, W] 00000000	SSR07 [R/W, R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
00007C <sub>H</sub>	ESCR07 [R/W] 00000X00	ECCR07 [R/W, R, W] -00000XX	FSR07 [RW/R] xx00 0000	FCR07 [R/W] 0001 - 000	
000080 <sub>H</sub>	Reserved				Reserved
000084 <sub>H</sub>	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	Reserved		Baud rate Generator LIN-USART 2,4 to 7
000088 <sub>H</sub>	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
00008C <sub>H</sub>	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090 <sub>H</sub>	PWC20 [R/W] ----- XX XXXXXXXX		PWC10 [R/W] ----- XX XXXXXXXX		
000094 <sub>H</sub>	Reserved		PWS20 [R/W] -0000000	PWS10 [R/W] - -000000	Stepper Motor 0
000098 <sub>H</sub>	PWC21 [R/W] ----- XX XXXXXXXX		PWC11 [R/W] ----- XX XXXXXXXX		
00009C <sub>H</sub>	Reserved		PWS21 [R/W] -0000000	PWS11 [R/W] - -000000	Stepper Motor 1

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000A0 <sub>H</sub>	PWC22 [R/W] ----- XX XXXXXXXX		PWC12 [R/W] ----- XX XXXXXXXX		Stepper Motor 2
0000A4 <sub>H</sub>	Reserved		PWS22 [R/W] -0000000	PWS12 [R/W] - -000000	
0000A8 <sub>H</sub>	PWC23 [R/W] ----- XX XXXXXXXX		PWC13 [R/W] ----- XX XXXXXXXX		Stepper Motor 3
0000AC <sub>H</sub>	Reserved		PWS23 [R/W] -0000000	PWS13 [R/W] - -000000	
0000B0 <sub>H</sub>	PWC24 [R/W] ----- XX XXXXXXXX		PWC14 [R/W] ----- XX XXXXXXXX		Stepper Motor 4
0000B4 <sub>H</sub>	Reserved		PWS24 [R/W] -0000000	PWS14 [R/W] - -000000	
0000B8 <sub>H</sub>	PWC25 [R/W] ----- XX XXXXXXXX		PWC15 [R/W] ----- XX XXXXXXXX		Stepper Motor 5
0000BC <sub>H</sub>	Reserved		PWS25 [R/W] -0000000	PWS15 [R/W] - -000000	
0000C0 <sub>H</sub>	Reserved	PWC0 [R/W] -00000--	Reserved	PWC1 [R/W] -00000--	Stepper Motor Control 0 to 5
0000C4 <sub>H</sub>	Reserved	PWC2 [R/W] -00000--	Reserved	PWC3 [R/W] -00000--	
0000C8 <sub>H</sub>	Reserved	PWC4 [R/W] -00000--	Reserved	PWC5 [R/W] -00000--	
0000CC <sub>H</sub>	Reserved				Reserved
0000D0 <sub>H</sub>	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] ----- 00	ITBAL0 [R/W] 00000000	I <sup>2</sup> C 0
0000D4 <sub>H</sub>	ITMKH0 [R/W] 00 ----- 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
0000D8 <sub>H</sub>	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] 00011111	Reserved	
0000DC <sub>H</sub> to 000100 <sub>H</sub>	Reserved				Reserved
000104 <sub>H</sub>	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] ----- 0000	PPG Control 4 to 7
000108 <sub>H</sub>	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] ----- 0000	PPG Control 8 to 11
000110 <sub>H</sub> to 00012C <sub>H</sub>	Reserved				Reserved

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
000130 <sub>H</sub>	PTMR04 [R] 11111111 11111111		PCSR04 [R/W] XXXXXXXX XXXXXXXX		PPG 4	
000134 <sub>H</sub>	PDUT04 [R/W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 0000000 - 0		
000138 <sub>H</sub>	PTMR05 [R] 11111111 11111111		PCSR05 [R/W] XXXXXXXX XXXXXXXX		PPG 5	
00013C <sub>H</sub>	PDUT05 [R/W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 0000000 - 0		
000140 <sub>H</sub>	PTMR06 [R] 11111111 11111111		PCSR06 [R/W] XXXXXXXX XXXXXXXX		PPG 6	
000144 <sub>H</sub>	PDUT06 [R/W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 0000000 - 0		
000148 <sub>H</sub>	PTMR07 [R] 11111111 11111111		PCSR07 [R/W] XXXXXXXX XXXXXXXX		PPG 7	
00014C <sub>H</sub>	PDUT07 [R/W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 0000000 - 0		
000150 <sub>H</sub>	PTMR08 [R] 11111111 11111111		PCSR08 [R/W] XXXXXXXX XXXXXXXX		PPG 8	
000154 <sub>H</sub>	PDUT08 [R/W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 0000000 - 0		
000158 <sub>H</sub>	PTMR09 [R] 11111111 11111111		PCSR09 [R/W] XXXXXXXX XXXXXXXX		PPG 9	
00015C <sub>H</sub>	PDUT09 [R/W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 0000000 - 0		
000160 <sub>H</sub>	PTMR10 [R] 11111111 11111111		PCSR10 [R/W] XXXXXXXX XXXXXXXX		PPG 10	
000164 <sub>H</sub>	PDUT10 [R/W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 0000000 - 0		
000168 <sub>H</sub>	PTMR11 [R] 11111111 11111111		PCSR11 [R/W] XXXXXXXX XXXXXXXX		PPG 11	
00016C <sub>H</sub>	PDUT11 [R/W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 0000000 - 0		
000170 <sub>H</sub>	P0TMCSR <sub>H</sub> [R/W] - 0 - 000 - 0	P0TMCSRL [R/W] --- 00000	P1TMCSR <sub>H</sub> [R/W] - 0 - 000 - 0	P1TMCSRL [R/W] --- 00000	PFM	
000174 <sub>H</sub>	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX			
000178 <sub>H</sub>	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX			
00017C <sub>H</sub>	Reserved				Reserved	

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000180 <sub>H</sub>	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184 <sub>H</sub>		IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX	
000188 <sub>H</sub>		IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX	
00018C <sub>H</sub>		OCS01 [R/W] --- 0 - - 00 0000 - - 00		OCS23 [R/W] --- 0 - - 00 0000 - - 00	Output Compare 0 to 3
000190 <sub>H</sub>		OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX	
000194 <sub>H</sub>		OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX	
000198 <sub>H</sub>	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] -- 0 - - 000		SGFR [R/W, R] XXXXXXXX XXXXXXXX	Sound Generator
00019C <sub>H</sub>	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
0001A0 <sub>H</sub>		ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000	A/D Converter 0
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000 0 [R] --- 0 [W]	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8 <sub>H</sub>	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] --- 00000	ADECH [R/W] --- 00000	
0001AC <sub>H</sub>	Reserved	ACSR0 [R/W] - 11XXX00	Reserved		Alarm Comparator 0
0001B0 <sub>H</sub>		TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX	Reload Timer 0
0001B4 <sub>H</sub>		Reserved	TMCSRHO [R/W] --- 00000	TMCSRL0 [R/W] 0 - 000000	
0001B8 <sub>H</sub>		TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX	Reload Timer 1
0001BC <sub>H</sub>		Reserved	TMCSRHI [R/W] --- 00000	TMCSRL1 [R/W] 0 - 000000	
0001C0 <sub>H</sub>		TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX	Reload Timer 2 (PPG 4, PPG 5)
0001C4 <sub>H</sub>		Reserved	TMCSRHI2 [R/W] --- 00000	TMCSRL2 [R/W] 0 - 000000	

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0001C8 <sub>H</sub>	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
0001CC <sub>H</sub>	Reserved		TMCSRH3 [R/W] --- 00000	TMCSRL3 [R/W] 0 - 000000	
0001D0 <sub>H</sub>	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
0001D4 <sub>H</sub>	Reserved		TMCSRH4 [R/W] --- 00000	TMCSRL4 [R/W] 0 - 000000	
0001D8 <sub>H</sub>	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
0001DC <sub>H</sub>	Reserved		TMCSRH5 [R/W] --- 00000	TMCSRL5 [R/W] 0 - 000000	
0001E0 <sub>H</sub>	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
0001E4 <sub>H</sub>	Reserved		TMCSRH6 [R/W] --- 00000	TMCSRL6 [R/W] 0 - 000000	
0001E8 <sub>H</sub>	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
0001EC <sub>H</sub>	Reserved		TMCSRH7 [R/W] --- 00000	TMCSRL7 [R/W] 0 - 000000	
0001F0 <sub>H</sub>	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
0001F4 <sub>H</sub>	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
0001F8 <sub>H</sub>	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
0001FC <sub>H</sub>	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)

(Continued)

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
000200 <sub>H</sub>	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC	
000204 <sub>H</sub>	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX					
000208 <sub>H</sub>	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX					
00020C <sub>H</sub>	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX					
000210 <sub>H</sub>	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX					
000214 <sub>H</sub>	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX					
000218 <sub>H</sub>	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX					
00021C <sub>H</sub>	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX					
000220 <sub>H</sub>	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX					
000224 <sub>H</sub>	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX					
000228 <sub>H</sub> to 00023C <sub>H</sub>	Reserved					
000240 <sub>H</sub>	DMACR [R/W] 00 - - 0000	Reserved				
000244 <sub>H</sub> to 0002CC <sub>H</sub>	Reserved				Reserved	
0002D0 <sub>H</sub>	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7	
0002D4 <sub>H</sub>	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX			
0002D8 <sub>H</sub>	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX			
0002DC <sub>H</sub> to 0002EC <sub>H</sub>	Reserved				Reserved	
0002F0 <sub>H</sub>	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4  (ICU 4, ICU 5)	

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0002F4 <sub>H</sub>	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5  (ICU 6, ICU 7)
0002F8 <sub>H</sub>	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6
0002FC <sub>H</sub>	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7
000300 <sub>H</sub>	Reserved	UDRC0 [W] 00000000	Reserved	UDCR0 [R] 00000000	Up/Down Counter 0
000304 <sub>H</sub>	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308 <sub>H</sub> , 00030C <sub>H</sub>	Reserved				Reserved
000310 <sub>H</sub>	UDRC3 [W] 00000000	UDRC2 [W] 00000000	UDCR3 [R] 00000000	UDCR2 [R] 00000000	Up/Down Counter 2 to 3
000314 <sub>H</sub>	UDCCH2 [R/W] 00000000	UDCCL2 [R/W] 00001000	Reserved	UDCS2 [R/W] 00000000	
000318 <sub>H</sub>	UDCCH3 [R/W] 00000000	UDCCL3 [R/W] 00001000	Reserved	UDCS3 [R/W] 00000000	
00031C <sub>H</sub>	Reserved				Reserved
000320 <sub>H</sub>	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] ---- 0000	PPG Control 12 to 15
000324 <sub>H</sub> to 00032C <sub>H</sub>	Reserved				Reserved
000330 <sub>H</sub>	PTMR12 [R] 11111111 11111111		PCSR12 [R/W] XXXXXXXX XXXXXXXX		PPG 12
000334 <sub>H</sub>	PDUT12 [R/W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338 <sub>H</sub>	PTMR13 [R] 11111111 11111111		PCSR13 [R/W] XXXXXXXX XXXXXXXX		PPG 13
00033C <sub>H</sub>	PDUT13 [R/W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340 <sub>H</sub>	PTMR14 [R] 11111111 11111111		PCSR14 [R/W] XXXXXXXX XXXXXXXX		PPG 14
000344 <sub>H</sub>	PDUT14 [R/W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	

(Continued)

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
000348 <sub>H</sub>	PTMR15 [R] 11111111 11111111		PCSR15 [R/W] XXXXXXXX XXXXXXXX		PPG 15	
00034C <sub>H</sub>	PDUT15 [R/W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 0000000 - 0		
000350 <sub>H</sub> to 000364 <sub>H</sub>	Reserved				Reserved	
000368 <sub>H</sub>	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] ----- 00	ITBAL2 [R/W] 00000000	I <sup>2</sup> C 2	
00036C <sub>H</sub>	ITMKH2 [R/W] 00 ----- 11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] - 00000000		
000370 <sub>H</sub>	Reserved	IDAR2 [R/W] 00000000	ICCR2 [R/W] 00011111	Reserved		
000374 <sub>H</sub>	IBCR3 [R/W] 00000000	IBSR3 [R] 00000000	ITBAH3 [R/W] ----- 00	ITBAL3 [R/W] 00000000	I <sup>2</sup> C 3	
000378 <sub>H</sub>	ITMKH3 [R/W] 00 ----- 11	ITMKL3 [R/W] 11111111	ISMK3 [R/W] 01111111	ISBA3 [R/W] - 00000000		
00037C <sub>H</sub>	Reserved	IDAR3 [R/W] 00000000	ICCR3 [R/W] 00011111	Reserved		
000380 <sub>H</sub> to 00038C <sub>H</sub>	Reserved				Reserved	
000390 <sub>H</sub>	ROMS [R] 11111111 00000000 (MB91F467EA)		Reserved		ROM Select Register	
000394 <sub>H</sub> to 0003EC <sub>H</sub>	Reserved				Reserved	
0003F0 <sub>H</sub>	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module	
0003F4 <sub>H</sub>	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
0003F8 <sub>H</sub>	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
0003FC <sub>H</sub>	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
000400 <sub>H</sub> to 00043C <sub>H</sub>	Reserved				Reserved	

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000440 <sub>H</sub>	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444 <sub>H</sub>	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448 <sub>H</sub>	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044C <sub>H</sub>	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450 <sub>H</sub>	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454 <sub>H</sub>	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458 <sub>H</sub>	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045C <sub>H</sub>	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460 <sub>H</sub>	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464 <sub>H</sub>	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468 <sub>H</sub>	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046C <sub>H</sub>	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470 <sub>H</sub>	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474 <sub>H</sub>	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478 <sub>H</sub>	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
00047C <sub>H</sub>	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480 <sub>H</sub>	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX - 00	CTBR [W] XXXXXXXX	Clock Control
000484 <sub>H</sub>	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488 <sub>H</sub>	Reserved				Reserved

(Continued)

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
00048C <sub>H</sub>	PLLDIVM [R/W] ---- 0000	PLLDIVN [R/W] -- 000000	PLLDIVG [R/W] ---- 0000	PLLMULG [W] 00000000	PLL Interface	
000490 <sub>H</sub>	PLLCTRL [R/W] ---- 0000	Reserved				
000494 <sub>H</sub>	OSCC1 [R/W] ---- 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] ---- 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control	
000498 <sub>H</sub>	PORTE <sub>N</sub> [R/W] ----- 00	Reserved				
00049C <sub>H</sub>	Reserved				Reserved	
0004A0 <sub>H</sub>	Reserved	WTCSR [R/W] ----- 00	WTCR [R/W] 00000000 000 - 00 - 0			
0004A4 <sub>H</sub>	Reserved	WTBR [R/W] --- XXXXX XXXXXXXXX XXXXXXXXX				
0004A8 <sub>H</sub>	WTHR [R/W] --- 00000	WTMR [R/W] -- 000000	WTSR [R/W] -- 000000	Reserved	Real Time Clock (Watch Timer)	
0004AC <sub>H</sub>	CSVTR [R/W] --- 00010	CSVCR [R/W/ <b>W0</b> ] 000 <b>11</b> 100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000		
0004B0 <sub>H</sub>	CUCR [R/W] ----- 0 - - 00		CUTD [R/W] 10000000 00000000			
0004B4 <sub>H</sub>	CUTR1 [R] ----- 00000000		CUTR2 [R] 00000000 00000000			
0004B8 <sub>H</sub>	CMPR [R/W] -- 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulator	
0004BC <sub>H</sub>	CMT1 [R/W] 00000000 1 - - 0000		CMT2 [R/W] -- 000000 - - 000000			
0004C0 <sub>H</sub>	CANPRE [R/W] 0 - - 0000	CANCKD [R/W] ----- <b>00</b> *1	Reserved		CAN Clock Control	

1. Depends on the number of available CAN channels.

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0004C4 <sub>H</sub>	LVSEL [R/W] 00000111	LVDET [R/W] 0000 0 - 00	HWWDE [R/W] --- 0 -- 00 <sup>*1</sup>	HWWD [R/W, W] 00011000	Low Voltage Detection/ Hardware Watchdog
0004C8 <sub>H</sub>	OSCRH [R/W] 000 - - 001	OSCRL [R/W] ---- 000	WPCRH [R/W] 00 - - - 000	WPCRL [R/W] ---- - 00	Main-/Sub-Oscillation Stabilisation Timer
0004CC <sub>H</sub>	OSCCR [R/W] ---- 00 <sup>*2</sup>	Reserved	REGSEL [R/W] -- 11 0110 <sup>*3</sup>	REGCTR [R/W] --- 0 - - 00	Main- Oscillation Standby Control Main-/Subregulator Control
0004D0 <sub>H</sub>	Reserved				Reserved
0004D4 <sub>H</sub>	SHDE [R/W] 0 - - - - 0	reserved	EXTE [R/W] 0000 0000	EXTF [R/W0] 0000 0000	Shutdown Control
0004D8 <sub>H</sub>	EXTLV [R/W] 0000 0000 0000 0000		reserved	SHDINT [R/W] ---- 0000	
0004DC <sub>H</sub> to 00063C <sub>H</sub>	Reserved				Reserved

1. HWWDE[4] is STP\_RUN, see “HARDWARE WATCHDOG (Extension)” on page 51
2. OSCCR[1] is OSCDS2, see MB91460 series hardware manual
3. Main regulator default is 1.9V, sub regulator 1.8V (MB91F467D regulator defaults are 1.8V/1.6V)

(Continued)

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
000640 <sub>H</sub>	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00100000 * <sup>1</sup>		External Bus	
000644 <sub>H</sub>	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX			
000648 <sub>H</sub>	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX			
00064C <sub>H</sub>	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX			
000650 <sub>H</sub>	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX			
000654 <sub>H</sub>	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX			
000658 <sub>H</sub>	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX			
00065C <sub>H</sub>	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX			
000660 <sub>H</sub>	AWR0 [R/W] 01001111 11111011		AWR1 [R/W] XXXXXXXX XXXXXXXX			
000664 <sub>H</sub>	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX			
000668 <sub>H</sub>	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX			
00066C <sub>H</sub>	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX			
000670 <sub>H</sub>	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved			
000674 <sub>H</sub>	Reserved					
000678 <sub>H</sub>	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX		
00067C <sub>H</sub>	Reserved					
000680 <sub>H</sub>	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** * <sup>2</sup>		
000684 <sub>H</sub>	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved			

# MB91460E Series

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
000688 <sub>H</sub>	RCO0H0 [R/W] 11111111	RCO0L0 [R/W] 0000 0000	RCO0H1 [R/W] 11111111	RCO0L1 [R/W] 0000 0000	A/D Converter 0 Range Comparator	
00068C <sub>H</sub>	RCO0H2 [R/W] 11111111	RCO0L2 [R/W] 0000 0000	RCO0H3 [R/W] 11111111	RCO0L3 [R/W] 0000 0000		
000690 <sub>H</sub>	RCO0IRS [R/W] 00000000 00000000 00000000 00000000					
000694 <sub>H</sub>	RCO0OF [R] 00000000 00000000 00000000 00000000					
000698 <sub>H</sub>	RCO0INT [R/W0] 00000000 00000000 00000000 00000000					
00069C <sub>H</sub>	reserved					
0006A0 <sub>H</sub>	AD0CC0 [R/W] 0000 0000	AD0CC1 [R/W] 0000 0000	AD0CC2 [R/W] 0000 0000	AD0CC3 [R/W] 0000 0000	A/D Converter 0 Chan- nel Control	
0006A4 <sub>H</sub>	AD0CC4 [R/W] 0000 0000	AD0CC5 [R/W] 0000 0000	AD0CC6 [R/W] 0000 0000	AD0CC7 [R/W] 0000 0000		
0006A8 <sub>H</sub>	AD0CC8 [R/W] 0000 0000	AD0CC9 [R/W] 0000 0000	AD0CC10 [R/W] 0000 0000	AD0CC11 [R/W] 0000 0000		
0006AC <sub>H</sub>	AD0CC12 [R/W] 0000 0000	AD0CC13 [R/W] 0000 0000	AD0CC14 [R/W] 0000 0000	AD0CC15 [R/W] 0000 0000		
0006B0 <sub>H</sub>	AD0CS2 [RW] 0000 - - 00	reserved			A/D Converter 0 Con- trol register 2	
0006B4 <sub>H</sub> to 0006DC <sub>H</sub>	Reserved					
0006E0 <sub>H</sub>	ADC0D0 [R] ----- XX XXXXXXXX		ADC0D1 [R] ----- XX XXXXXXXX		A/D Converter 0 Chan- nel Data registers	
0006E4 <sub>H</sub>	ADC0D2 [R] ----- XX XXXXXXXX		ADC0D3 [R] ----- XX XXXXXXXX			
0006E8 <sub>H</sub>	ADC0D4 [R] ----- XX XXXXXXXX		ADC0D5 [R] ----- XX XXXXXXXX			
0006EC <sub>H</sub>	ADC0D6 [R] ----- XX XXXXXXXX		ADC0D7 [R] ----- XX XXXXXXXX			
0006F0 <sub>H</sub>	ADC0D8 [R] ----- XX XXXXXXXX		ADC0D9 [R] ----- XX XXXXXXXX			
0006F4 <sub>H</sub>	ADC0D10 [R] ----- XX XXXXXXXX		ADC0D11 [R] ----- XX XXXXXXXX			
0006F8 <sub>H</sub>	ADC0D12 [R] ----- XX XXXXXXXX		ADC0D13 [R] ----- XX XXXXXXXX			
0006FC <sub>H</sub>	ADC0D14 [R] ----- XX XXXXXXXX		ADC0D15 [R] ----- XX XXXXXXXX			
000700 <sub>H</sub>	ADC0D16 [R] ----- XX XXXXXXXX		ADC0D17 [R] ----- XX XXXXXXXX			

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000704 <sub>H</sub>	ADC0D18 [R] ----- XX XXXXXXXX		ADC0D19 [R] ----- XX XXXXXXXX		A/D Converter 0 Channel Data registers
000708 <sub>H</sub>	ADC0D20 [R] ----- XX XXXXXXXX		ADC0D21 [R] ----- XX XXXXXXXX		
00070C <sub>H</sub>	ADC0D22 [R] ----- XX XXXXXXXX		ADC0D23 [R] ----- XX XXXXXXXX		
000710 <sub>H</sub>	ADC0D24 [R] ----- XX XXXXXXXX		ADC0D25 [R] ----- XX XXXXXXXX		
000714 <sub>H</sub>	ADC0D26 [R] ----- XX XXXXXXXX		ADC0D27 [R] ----- XX XXXXXXXX		
000718 <sub>H</sub>	ADC0D28 [R] ----- XX XXXXXXXX		ADC0D29 [R] ----- XX XXXXXXXX		
00071C <sub>H</sub>	ADC0D30 [R] ----- XX XXXXXXXX		ADC0D31 [R] ----- XX XXXXXXXX		
000720 <sub>H</sub> to 0007F8 <sub>H</sub>	Reserved				
0007FC <sub>H</sub>	Reserved	MODR [W] XXXXXX	Reserved		Mode Register

1. ACR0 [11 : 10] depends on bus width setting in Mode vector fetch information.
2. TCR [3 : 0] INIT value = 0000, keeps value after RST

# MB91460E Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000800 <sub>H</sub> to 000CFC <sub>H</sub>	Reserved				Reserved
000D00 <sub>H</sub>	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	PDRD02 [R] XXXXXXXX	PDRD03 [R] XXXXXXXX	R-bus Port Data Direct Read Register
000D04 <sub>H</sub>	PDRD04 [R] ----- XX	PDRD05 [R] XXXXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
000D08 <sub>H</sub>	PDRD08 [R] XXXXXXXX	PDRD09 [R] XX - XXXX	PDRD10 [R] - XXXXXX -	Reserved	
000D0C <sub>H</sub>	Reserved	PDRD13 [R] ----- XXX	PDRD14 [R] XXXXXXXX	PDRD15 [R] ----- XXXX	
000D10 <sub>H</sub>	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXX -----	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
000D14 <sub>H</sub>	PDRD20 [R] ----- XXX	Reserved	PDRD22 [R] -- XX - X - X	PDRD23 [R] -- XXXXXX	
000D18 <sub>H</sub>	PDRD24 [R] XXXXXXXX	PDRD25 [R] XXXXXXXX	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
000D1C <sub>H</sub>	Reserved	PDRD29 [R] XXXXXXXX	Reserved		
000D20 <sub>H</sub> to 000D3C <sub>H</sub>	Reserved				Reserved
000D40 <sub>H</sub>	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	DDR02 [R/W] 00000000	DDR03 [R/W] 00000000	R-bus Port Direction Register
000D44 <sub>H</sub>	DDR04 [R/W] ----- 00	DDR05 [R/W] 00000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
000D48 <sub>H</sub>	DDR08 [R/W] 00000000	DDR09 [R/W] 00 - - 0000	DDR10 [R/W] - 000000 -	Reserved	
000D4C <sub>H</sub>	Reserved	DDR13 [R/W] ----- 000	DDR14 [R/W] 00000000	DDR15 [R/W] ----- 0000	
000D50 <sub>H</sub>	DDR16 [R/W] 00000000	DDR17 [R/W] 0000 - - -	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
000D54 <sub>H</sub>	DDR20 [R/W] ----- 000	Reserved	DDR22 [R/W] -- 00 - 0 - 0	DDR23 [R/W] -- 000000	
000D58 <sub>H</sub>	DDR24 [R/W] 00000000	DDR25 [R/W] 00000000	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
000D5C <sub>H</sub>	Reserved	DDR29 [R/W] 00000000	Reserved		
000D60 <sub>H</sub> to 000D7C <sub>H</sub>	Reserved				Reserved

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000D80 <sub>H</sub>	PFR00 [R/W] 00000000 *1	PFR01 [R/W] 00000000 *1	PFR02 [R/W] 00000000 *1	PFR03 [R/W] 00000000 *1	R-bus Port Function Register
000D84 <sub>H</sub>	PFR04 [R/W] - - - - 00 *1	PFR05 [R/W] 00000000 *1	PFR06 [R/W] 00000000 *1	PFR07 [R/W] 00000000 *1	
000D88 <sub>H</sub>	PFR08 [R/W] 00000000 *1	PFR09 [R/W] 00 - - 0000 *1	PFR10 [R/W] - 000 000 - *1	Reserved	
000D8C <sub>H</sub>	Reserved	PFR13 [R/W] - - - 000 *1	PFR14 [R/W] 00000000	PFR15 [R/W] - - - 0000	
000D90 <sub>H</sub>	PFR16 [R/W] 00000000	PFR17 [R/W] 0000 - - -	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
000D94 <sub>H</sub>	PFR20 [R/W] - - - - 000	Reserved	PFR22 [R/W] - - 00 - 0 - 0	PFR23 [R/W] - - 000000	
000D98 <sub>H</sub>	PFR24 [R/W] 00000000	PFR25 [R/W] 00000000	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
000D9C <sub>H</sub>	Reserved	PFR29 [R/W] 00000000	Reserved		
000DA0 <sub>H</sub> to 000DBC <sub>H</sub>	Reserved				Reserved
000DC0 <sub>H</sub>	EPFR00 [R/W] - - - - -	EPFR01 [R/W] - - - - -	EPFR02 [R/W] - - - - -	EPFR03 [R/W] - - - - -	R-bus Extra Port Function Register
000DC4 <sub>H</sub>	EPFR04 [R/W] - - - - -	EPFR05 [R/W] - - - - -	EPFR06 [R/W] - - - - -	EPFR07 [R/W] - - - - -	
000DC8 <sub>H</sub>	EPFR08 [R/W] - - - - -	EPFR09 [R/W] - - - - -	EPFR10 [R/W] - - 00 - - -	Reserved	
000DCC <sub>H</sub>	Reserved	EPFR13 [R/W] - - - 0 - -	EPFR14 [R/W] 00000000	EPFR15 [R/W] - - - 0000	
000DD0 <sub>H</sub>	EPFR16 [R/W] 0000 - - -	EPFR17 [R/W] - - - - -	EPFR18 [R/W] - 00 - - 00 -	EPFR19 [R/W] - 0 - - 0 - -	
000DD4 <sub>H</sub>	EPFR20 [R/W] - - - 00 -	Reserved	EPFR22 [R/W] - - - - -	EPFR23 [R/W] - - - - -	
000DD8 <sub>H</sub>	EPFR24 [R/W] - - - - -	EPFR25 [R/W] - - - - -	EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
000DDC <sub>H</sub>	Reserved	EPFR29 [R/W] - - - - -	Reserved		
000DE0 <sub>H</sub> to 000DFC <sub>H</sub>	Reserved				Reserved

1. In internal vector fetch mode (MD[2:0]=000) PFR00 to PFR13 are initialized to 0x00 for GPIO mode.  
In external vector fetch mode (MD[2:0]=001) PFR00 to PFR13 are initialized to 0xFF to enable the external bus.

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E00 <sub>H</sub>	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	PODR02 [R/W] 00000000	PODR03 [R/W] 00000000	R-bus Port Output Drive Select Register
000E04 <sub>H</sub>	PODR04 [R/W] ----- 00	PODR05 [R/W] 00000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
000E08 <sub>H</sub>	PODR08 [R/W] 00000000	PODR09 [R/W] 00 - - 0000	PODR10 [R/W] - 000000 -	Reserved	
000E0C <sub>H</sub>	Reserved	PODR13 [R/W] ----- 000	PODR14 [R/W] 00000000	PODR15 [R/W] ----- 0000	
000E10 <sub>H</sub>	PODR16 [R/W] 00000000	PODR17 [R/W] 0000 - - -	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
000E14 <sub>H</sub>	PODR20 [R/W] ----- 000	Reserved	PODR22 [R/W] - - 00 - 0 - 0	PODR23 [R/W] - - 000000	
000E18 <sub>H</sub>	PODR24 [R/W] 00000000	PODR25 [R/W] 00000000	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
000E1C <sub>H</sub>	Reserved	PODR29 [R/W] 00000000	Reserved		
000E20 <sub>H</sub> to 000E3C <sub>H</sub>	Reserved				Reserved
000E40 <sub>H</sub>	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	PILR02 [R/W] 00000000	PILR03 [R/W] 00000000	R-bus Port Input Level Select Register
000E44 <sub>H</sub>	PILR04 [R/W] ----- 00	PILR05 [R/W] 00000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
000E48 <sub>H</sub>	PILR08 [R/W] 00000000	PILR09 [R/W] 00 - - 0000	PILR10 [R/W] - 000000 -	Reserved	
000E4C <sub>H</sub>	Reserved	PILR13 [R/W] ----- 000	PILR14 [R/W] 00000000	PILR15 [R/W] ----- 0000	
000E50 <sub>H</sub>	PILR16 [R/W] 00000000	PILR17 [R/W] 0000 - - -	PILR18 [R/W] - 000 - 000	PILR19 [R/W] - 000 - 000	
000E54 <sub>H</sub>	PILR20 [R/W] ----- 000	Reserved	PILR22 [R/W] - - 00 - 0 - 0	PILR23 [R/W] - - 000000	
000E58 <sub>H</sub>	PILR24 [R/W] 00000000	PILR25 [R/W] 00000000	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
000E5C <sub>H</sub>	Reserved	PILR29 [R/W] 00000000	Reserved		
000E60 <sub>H</sub> to 000E7C <sub>H</sub>	Reserved				Reserved

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E80 <sub>H</sub>	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	EPILR02 [R/W] 00000000	EPILR03 [R/W] 00000000	R-bus Extra Port Input Level Select Register
000E84 <sub>H</sub>	EPILR04 [R/W] ----- 00	EPILR05 [R/W] 00000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
000E88 <sub>H</sub>	EPILR08 [R/W] 00000000	EPILR09 [R/W] 00 - - 0000	EPILR10 [R/W] - 000000 -	Reserved	
000E8C <sub>H</sub>	Reserved	EPILR13 [R/W] ----- 000	EPILR14 [R/W] 00000000	EPILR15 [R/W] ----- 0000	
000E90 <sub>H</sub>	EPILR16 [R/W] 00000000	EPILR17 [R/W] 0000 - - -	EPILR18 [R/W] - 000 - 000	EPILR19 [R/W] - 000 - 000	
000E94 <sub>H</sub>	EPILR20 [R/W] ----- 000	Reserved	EPILR22 [R/W] - - 00 - 0 - 0	EPILR23 [R/W] - - 000000	
000E98 <sub>H</sub>	EPILR24 [R/W] 00000000	EPILR25 [R/W] 00000000	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
000E9C <sub>H</sub>	Reserved	EPILR29 [R/W] 00000000	Reserved		
000EA0 <sub>H</sub> to 000EBC <sub>H</sub>	Reserved				Reserved
000EC0 <sub>H</sub>	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	PPER02 [R/W] 00000000	PPER03 [R/W] 00000000	R-bus Port Pull-Up/Down Enable Register
000EC4 <sub>H</sub>	PPER04 [R/W] ----- 00	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
000EC8 <sub>H</sub>	PPER08 [R/W] 00000000	PPER09 [R/W] 00 - - 0000	PPER10 [R/W] - 000000 -	Reserved	
000ECC <sub>H</sub>	Reserved	PPER13 [R/W] ----- 000	PPER14 [R/W] 00000000	PPER15 [R/W] ----- 0000	
000ED0 <sub>H</sub>	PPER16 [R/W] 00000000	PPER17 [R/W] 0000 - - -	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
000ED4 <sub>H</sub>	PPER20 [R/W] ----- 000	Reserved	PPER22 [R/W] - - 00 - 0 - 0	PPER23 [R/W] - - 000000	
000ED8 <sub>H</sub>	PPER24 [R/W] 00000000	PPER25 [R/W] 00000000	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
000EDC <sub>H</sub>	Reserved	PPER29 [R/W] 00000000	Reserved		
000EE0 <sub>H</sub> to 000EFC <sub>H</sub>	Reserved				Reserved

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
000F00 <sub>H</sub>	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	PPCR02 [R/W] 11111111	PPCR03 [R/W] 11111111	R-bus Port Pull-Up/Down Control Register	
000F04 <sub>H</sub>	PPCR04 [R/W] ----- 11	PPCR05 [R/W] 11111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111		
000F08 <sub>H</sub>	PPCR08 [R/W] 11111111	PPCR09 [R/W] 11 - - 1111	PPCR10 [R/W] - 111111 -	Reserved		
000F0C <sub>H</sub>	Reserved	PPCR13 [R/W] ----- 111	PPCR14 [R/W] 11111111	PPCR15 [R/W] ----- 1111		
000F10 <sub>H</sub>	PPCR16 [R/W] 11111111	PPCR17 [R/W] 1111 - - -	PPCR18 [R/W] - 111 - 111	PPCR19 [R/W] - 111 - 111		
000F14 <sub>H</sub>	PPCR20 [R/W] ----- 111	Reserved	PPCR22 [R/W] - - 11 - 1 - 1	PPCR23 [R/W] - - 111111		
000F18 <sub>H</sub>	PPCR24 [R/W] 11111111	PPCR25 [R/W] 11111111	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111		
000F1C <sub>H</sub>	Reserved	PPCR29 [R/W] 11111111	Reserved			
000F20 <sub>H</sub> to 000F3C <sub>H</sub>	Reserved				Reserved	
001000 <sub>H</sub>	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC	
001004 <sub>H</sub>	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001008 <sub>H</sub>	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00100C <sub>H</sub>	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001010 <sub>H</sub>	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001014 <sub>H</sub>	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001018 <sub>H</sub>	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00101C <sub>H</sub>	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001020 <sub>H</sub>	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001024 <sub>H</sub>	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
001028 <sub>H</sub> to 001FFC <sub>H</sub>	Reserved				Reserved	

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
002000 <sub>H</sub> to 006FFC <sub>H</sub>	MB91F467EA Flash-cache size is 8 Kbytes : 004000 <sub>H</sub> to 005FFC <sub>H</sub>				Flash-cache / I-RAM area	
007000 <sub>H</sub>	FMCS [R/W] 01101000	FMCR [R] --- 00000	FCHCR [R/W] ----- 00 10000011		Flash Memory/ Flash-cache/ I-RAM Control Register	
007004 <sub>H</sub>	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 -----	FMPS [R/W] ----- 000		
007008 <sub>H</sub>	FMAC [R] 00000000 00000000 00000000 00000000					
00700C <sub>H</sub>	FCHA0 [R/W] ----- 00000 00000000 00000000					
007010 <sub>H</sub>	FCHA1 [R/W] ----- 00000 00000000 00000000				Flash-cache Non-cacheable area setting Register	
007014 <sub>H</sub> to 007FFC <sub>H</sub>	Reserved					
008000 <sub>H</sub> to 00BFFC <sub>H</sub>	MB91F467EA Boot-ROM size is 4 Kbytes : 00B000 <sub>H</sub> to 00BFFC <sub>H</sub> (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area	
00C000 <sub>H</sub>	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register	
00C004 <sub>H</sub>	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001			
00C008 <sub>H</sub>	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000			
00C00C <sub>H</sub>	BRPE0 [R/W] 00000000 00000000		Reserved			
00C010 <sub>H</sub>	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register	
00C014 <sub>H</sub>	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111			
00C018 <sub>H</sub>	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000			
00C01C <sub>H</sub>	IF1MCTR0 [R/W] 00000000 00000000		Reserved			

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
00C020 <sub>H</sub>	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		CAN 0 IF 1 Register	
00C024 <sub>H</sub>	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000			
00C028 <sub>H</sub> , 00C02C <sub>H</sub>	Reserved					
00C030 <sub>H</sub>	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000			
00C034 <sub>H</sub>	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000			
00C038 <sub>H</sub> , 00C03C <sub>H</sub>	Reserved					
00C040 <sub>H</sub>	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000			
00C044 <sub>H</sub>	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111			
00C048 <sub>H</sub>	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000			
00C04C <sub>H</sub>	IF2MCTR0 [R/W] 00000000 00000000		Reserved			
00C050 <sub>H</sub>	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		CAN 0 IF 2 Register	
00C054 <sub>H</sub>	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000			
00C058 <sub>H</sub> , 00C05C <sub>H</sub>	Reserved					
00C060 <sub>H</sub>	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000			
00C064 <sub>H</sub>	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000			
00C068 <sub>H</sub> to 00C07C <sub>H</sub>	Reserved					

(Continued)

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
00C080 <sub>H</sub>	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags	
00C084 <sub>H</sub> to 00C08C <sub>H</sub>	Reserved					
00C090 <sub>H</sub>	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000			
00C094 <sub>H</sub> to 00C09C <sub>H</sub>	Reserved					
00C0A0 <sub>H</sub>	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000			
00C0A4 <sub>H</sub> to 00C0AC <sub>H</sub>	Reserved					
00C0B0 <sub>H</sub>	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000			
00C0B4 <sub>H</sub> to 00C0FC <sub>H</sub>	Reserved				Reserved	
00C100 <sub>H</sub>	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register	
00C104 <sub>H</sub>	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001			
00C108 <sub>H</sub>	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000			
00C10C <sub>H</sub>	BRPE1 [R/W] 00000000 00000000		Reserved			
00C110 <sub>H</sub>	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register	
00C114 <sub>H</sub>	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111			
00C118 <sub>H</sub>	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000			
00C11C <sub>H</sub>	IF1MCTR1 [R/W] 00000000 00000000		Reserved			
00C120 <sub>H</sub>	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000			
00C124 <sub>H</sub>	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000			

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
00C128 <sub>H</sub> , 00C12C <sub>H</sub>	Reserved				CAN 1 IF 1 Register	
00C130 <sub>H</sub>	IF1DTA21 [R/W] 00000000 00000000	IF1DTA11 [R/W] 00000000 00000000				
00C134 <sub>H</sub>	IF1DTB21 [R/W] 00000000 00000000	IF1DTB11 [R/W] 00000000 00000000				
00C138 <sub>H</sub> , 00C13C <sub>H</sub>	Reserved					
00C140 <sub>H</sub>	IF2CREQ1 [R/W] 00000000 00000001	IF2CMSK1 [R/W] 00000000 00000000				
00C144 <sub>H</sub>	IF2MSK21 [R/W] 11111111 11111111	IF2MSK11 [R/W] 11111111 11111111				
00C148 <sub>H</sub>	IF2ARB21 [R/W] 00000000 00000000	IF2ARB11 [R/W] 00000000 00000000				
00C14C <sub>H</sub>	IF2MCTR1 [R/W] 00000000 00000000	Reserved				
00C150 <sub>H</sub>	IF2DTA11 [R/W] 00000000 00000000	IF2DTA21 [R/W] 00000000 00000000				
00C154 <sub>H</sub>	IF2DTB11 [R/W] 00000000 00000000	IF2DTB21 [R/W] 00000000 00000000				
00C158 <sub>H</sub> , 00C15C <sub>H</sub>	Reserved				CAN 1 IF 2 Register	
00C160 <sub>H</sub>	IF2DTA21 [R/W] 00000000 00000000	IF2DTA11 [R/W] 00000000 00000000				
00C164 <sub>H</sub>	IF2DTB21 [R/W] 00000000 00000000	IF2DTB11 [R/W] 00000000 00000000				
00C168 <sub>H</sub> to 00C17C <sub>H</sub>	Reserved					
00C180 <sub>H</sub>	TREQR21 [R] 00000000 00000000	TREQR11 [R] 00000000 00000000				
00C184 <sub>H</sub> to 00C18C <sub>H</sub>	Reserved					
00C190 <sub>H</sub>	NEWDT21 [R] 00000000 00000000	NEWDT11 [R] 00000000 00000000				
00C194 <sub>H</sub> to 00C19C <sub>H</sub>	Reserved					

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C1A0 <sub>H</sub>	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
00C1A4 <sub>H</sub> to 00C1AC <sub>H</sub>		Reserved			CAN 1 Status Flags
00C1B0 <sub>H</sub>	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
00C1B4 <sub>H</sub> to 00C1FC <sub>H</sub>		Reserved			
00C200 <sub>H</sub> to 00EFFF <sub>H</sub>		Reserved			Resedved

(Continued)

# MB91460E Series

(Continued)

Address	Register				Block	
	+ 0	+ 1	+ 2	+ 3		
00F000 <sub>H</sub>	BCTRL [R/W] ----- 11111100 00000000				EDSU / MPU	
00F004 <sub>H</sub>	BSTAT [R/W] ----- 000 00000000 10 -- 0000					
00F008 <sub>H</sub>	BIAC [R] ----- 00000000 00000000					
00F00C <sub>H</sub>	BOAC [R] ----- 00000000 00000000					
00F010 <sub>H</sub>	BIRQ [R/W] ----- 00000000 00000000					
00F014 <sub>H</sub> to 00F01C <sub>H</sub>	Reserved					
00F020 <sub>H</sub>	BCR0 [R/W] ----- 00000000 00000000 00000000					
00F024 <sub>H</sub>	BCR1 [R/W] ----- 00000000 00000000 00000000					
00F028 <sub>H</sub>	BCR2 [R/W] ----- 00000000 00000000 00000000					
00F02C <sub>H</sub>	BCR3 [R/W] ----- 00000000 00000000 00000000					
00F030 <sub>H</sub> to 00F07C <sub>H</sub>	Reserved				Reserved	
00F080 <sub>H</sub>	BAD0 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU	
00F084 <sub>H</sub>	BAD1 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00F088 <sub>H</sub>	BAD2 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00F08C <sub>H</sub>	BAD3 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00F090 <sub>H</sub>	BAD4 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00F094 <sub>H</sub>	BAD5 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					
00F098 <sub>H</sub>	BAD6 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX					

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00F09C <sub>H</sub>	BAD7 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F0A0 <sub>H</sub>	BAD8 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A4 <sub>H</sub>	BAD9 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A8 <sub>H</sub>	BAD10 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0AC <sub>H</sub>	BAD11 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B0 <sub>H</sub>	BAD12 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B4 <sub>H</sub>	BAD13 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B8 <sub>H</sub>	BAD14 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0BC <sub>H</sub>	BAD15 [R/W] XXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0C0 <sub>H</sub> to 01FFFC <sub>H</sub>	Reserved				Reserved
020000 <sub>H</sub> to 02FFFC <sub>H</sub>	MB91F467EA D-RAM size is 64 Kbytes : 020000 <sub>H</sub> to 02FFFC <sub>H</sub> (data access is 0 wait cycles)				D-RAM area
030000 <sub>H</sub> to 03FFFC <sub>H</sub>	MB91F467EA ID-RAM size is 48 Kbytes : 030000 <sub>H</sub> to 03BFFC <sub>H</sub> (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

# MB91460E Series

## 2. Flash memory and external bus area

32bit read/write	dat[31:0]				dat[31:0]				Block	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]			
Address	Register								Block	
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7		
040000 <sub>H</sub> to 05FFF8 <sub>H</sub>	SA8 (64KB)				SA9 (64KB)				ROMS0	
060000 <sub>H</sub> to 07FFF8 <sub>H</sub>	SA10 (64KB)				SA11 (64KB)				ROMS1	
080000 <sub>H</sub> to 09FFF8 <sub>H</sub>	SA12 (64KB)				SA13 (64KB)				ROMS2	
0A0000 <sub>H</sub> to 0BFFF8 <sub>H</sub>	SA14 (64KB)				SA15 (64KB)				ROMS3	
0C0000 <sub>H</sub> to 0DFFF8 <sub>H</sub>	SA16 (64KB)				SA17 (64KB)				ROMS4	
0E0000 <sub>H</sub> to 0FFFF0 <sub>H</sub>	SA18 (64KB)				SA19 (64KB)				ROMS5	
0FFFF8 <sub>H</sub>	FMV [R] <sup>1</sup> 06 00 00 00 <sub>H</sub>				FRV [R] <sup>2</sup> 00 00 BF F8 <sub>H</sub>					
100000 <sub>H</sub> to 11FFF8 <sub>H</sub>	SA20 (64KB)				SA21 (64KB)				ROMS6	
120000 <sub>H</sub> to 13FFF8 <sub>H</sub>	SA22 (64KB)				SA23 (64KB)					
140000 <sub>H</sub> to 143FF8 <sub>H</sub>	SA0 (8KB)				SA1 (8KB)				ROMS7	
144000 <sub>H</sub> to 147FF8 <sub>H</sub>	SA2 (8KB)				SA3 (8KB)					
148000 <sub>H</sub> to 14BFF8 <sub>H</sub>	SA4 (8KB)				SA5 (8KB)					
14C000 <sub>H</sub> to 14FFF8 <sub>H</sub>	SA6 (8KB)				SA7 (8KB)					
150000 <sub>H</sub> to 17FFF8 <sub>H</sub>	Reserved									

32bit read/write	dat[31:0]				dat[31:0]				Block
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000 <sub>H</sub> to 1BFFF8 <sub>H</sub>	External Bus Area								ROMS8
1C0000 <sub>H</sub> to 1FFFF8 <sub>H</sub>	External Bus Area								ROMS9
200000 <sub>H</sub> to 27FFF8 <sub>H</sub>	External Bus Area								ROMS10
280000 <sub>H</sub> to 2FFFF8 <sub>H</sub>	External Bus Area								ROMS11
300000 <sub>H</sub> to 37FFF8 <sub>H</sub>	External Bus Area								ROMS12
380000 <sub>H</sub> to 3FFFF8 <sub>H</sub>	External Bus Area								ROMS13
400000 <sub>H</sub> to 47FFF8 <sub>H</sub>	External Bus Area								ROMS14
480000 <sub>H</sub> to 4FFFF8 <sub>H</sub>	External Bus Area								ROMS15
500000 <sub>H</sub> to FFFABFF8 <sub>H</sub>	External Bus Area								
FFFAC000 <sub>H</sub> to FFFAFFF8 <sub>H</sub>	MB91F467EA Standby-RAM 16 KBytes (1 wait cycle)								Standby RAM
FFFB0000 <sub>H</sub> to FFFFFFF8 <sub>H</sub>	External Bus Area								

1. Write operations to address 0FFFF8<sub>H</sub> is not possible. When reading these addresses, the values shown above will be read.
2. Write operations to address 0FFFC<sub>H</sub> is not possible. When reading these addresses, the values shown above will be read.

# MB91460E Series

## ■ INTERRUPT VECTOR TABLE

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	—	—	3FC <sub>H</sub>	000FFFFC <sub>H</sub>	—
Mode vector	1	01	—	—	3F8 <sub>H</sub>	000FFFF8 <sub>H</sub>	—
System reserved	2	02	—	—	3F4 <sub>H</sub>	000FFFF4 <sub>H</sub>	—
System reserved	3	03	—	—	3F0 <sub>H</sub>	000FFFF0 <sub>H</sub>	—
System reserved	4	04	—	—	3EC <sub>H</sub>	000FFFEC <sub>H</sub>	—
CPU supervisor mode (INT #5 instruction) *5	5	05	—	—	3E8 <sub>H</sub>	000FFFE8 <sub>H</sub>	—
Memory Protection exception *5	6	06	—	—	3E4 <sub>H</sub>	000FFFE4 <sub>H</sub>	—
System reserved	7	07	—	—	3E0 <sub>H</sub>	000FFFE0 <sub>H</sub>	—
System reserved	8	08	—	—	3DC <sub>H</sub>	000FFFDC <sub>H</sub>	—
System reserved	9	09	—	—	3D8 <sub>H</sub>	000FFFD8 <sub>H</sub>	—
System reserved	10	0A	—	—	3D4 <sub>H</sub>	000FFFD4 <sub>H</sub>	—
System reserved	11	0B	—	—	3D0 <sub>H</sub>	000FFFD0 <sub>H</sub>	—
System reserved	12	0C	—	—	3CC <sub>H</sub>	000FFFCC <sub>H</sub>	—
System reserved	13	0D	—	—	3C8 <sub>H</sub>	000FFFCC8 <sub>H</sub>	—
Undefined instruction exception	14	0E	—	—	3C4 <sub>H</sub>	000FFFC4 <sub>H</sub>	—
NMI request	15	0F	F <sub>H</sub> fixed		3C0 <sub>H</sub>	000FFFC0 <sub>H</sub>	—
External Interrupt 0	16	10	ICR00	440 <sub>H</sub>	3BC <sub>H</sub>	000FFFBC <sub>H</sub>	0, 16
External Interrupt 1	17	11			3B8 <sub>H</sub>	000FFFFB8 <sub>H</sub>	1, 17
External Interrupt 2	18	12	ICR01	441 <sub>H</sub>	3B4 <sub>H</sub>	000FFFFB4 <sub>H</sub>	2, 18
External Interrupt 3	19	13			3B0 <sub>H</sub>	000FFFFB0 <sub>H</sub>	3, 19
External Interrupt 4	20	14	ICR02	442 <sub>H</sub>	3AC <sub>H</sub>	000FFFAC <sub>H</sub>	20
External Interrupt 5	21	15			3A8 <sub>H</sub>	000FFFA8 <sub>H</sub>	21
External Interrupt 6	22	16	ICR03	443 <sub>H</sub>	3A4 <sub>H</sub>	000FFFA4 <sub>H</sub>	22
External Interrupt 7	23	17			3A0 <sub>H</sub>	000FFFA0 <sub>H</sub>	23
External Interrupt 8	24	18	ICR04	444 <sub>H</sub>	39C <sub>H</sub>	000FFF9C <sub>H</sub>	—
External Interrupt 9	25	19			398 <sub>H</sub>	000FFF98 <sub>H</sub>	—
External Interrupt 10	26	1A	ICR05	445 <sub>H</sub>	394 <sub>H</sub>	000FFF94 <sub>H</sub>	—
Reserved	27	1B			390 <sub>H</sub>	000FFF90 <sub>H</sub>	—
External Interrupt 12	28	1C	ICR06	446 <sub>H</sub>	38C <sub>H</sub>	000FFF8C <sub>H</sub>	—
External Interrupt 13	29	1D			388 <sub>H</sub>	000FFF88 <sub>H</sub>	—
External Interrupt 14	30	1E	ICR07	447 <sub>H</sub>	384 <sub>H</sub>	000FFF84 <sub>H</sub>	—
Reserved	31	1F			380 <sub>H</sub>	000FFF80 <sub>H</sub>	—

(Continued)

(Continued)

Interrupt	Interrupt number		Interrupt level <sup>*1</sup>		Interrupt vector <sup>*2</sup>		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Reload Timer 0	32	20	ICR08	448 <sub>H</sub>	37C <sub>H</sub>	000FFF7C <sub>H</sub>	4, 32
Reload Timer 1	33	21			378 <sub>H</sub>	000FFF78 <sub>H</sub>	5, 33
Reload Timer 2	34	22	ICR09	449 <sub>H</sub>	374 <sub>H</sub>	000FFF74 <sub>H</sub>	34
Reload Timer 3	35	23			370 <sub>H</sub>	000FFF70 <sub>H</sub>	35
Reload Timer 4	36	24	ICR10	44A <sub>H</sub>	36C <sub>H</sub>	000FFF6C <sub>H</sub>	36
Reload Timer 5	37	25			368 <sub>H</sub>	000FFF68 <sub>H</sub>	37
Reload Timer 6	38	26	ICR11	44B <sub>H</sub>	364 <sub>H</sub>	000FFF64 <sub>H</sub>	38
Reload Timer 7	39	27			360 <sub>H</sub>	000FFF60 <sub>H</sub>	39
Free Run Timer 0	40	28	ICR12	44C <sub>H</sub>	35C <sub>H</sub>	000FFF5C <sub>H</sub>	40
Free Run Timer 1	41	29			358 <sub>H</sub>	000FFF58 <sub>H</sub>	41
Free Run Timer 2	42	2A	ICR13	44D <sub>H</sub>	354 <sub>H</sub>	000FFF54 <sub>H</sub>	42
Free Run Timer 3	43	2B			350 <sub>H</sub>	000FFF50 <sub>H</sub>	43
Free Run Timer 4	44	2C	ICR14	44E <sub>H</sub>	34C <sub>H</sub>	000FFF4C <sub>H</sub>	44
Free Run Timer 5	45	2D			348 <sub>H</sub>	000FFF48 <sub>H</sub>	45
Free Run Timer 6	46	2E	ICR15	44F <sub>H</sub>	344 <sub>H</sub>	000FFF44 <sub>H</sub>	46
Free Run Timer 7	47	2F			340 <sub>H</sub>	000FFF40 <sub>H</sub>	47
CAN 0	48	30	ICR16	450 <sub>H</sub>	33C <sub>H</sub>	000FFF3C <sub>H</sub>	—
CAN 1	49	31			338 <sub>H</sub>	000FFF38 <sub>H</sub>	—
Reserved	50	32	ICR17	451 <sub>H</sub>	334 <sub>H</sub>	000FFF34 <sub>H</sub>	—
Reserved	51	33			330 <sub>H</sub>	000FFF30 <sub>H</sub>	—
Reserved	52	34	ICR18	452 <sub>H</sub>	32C <sub>H</sub>	000FFF2C <sub>H</sub>	—
Reserved	53	35			328 <sub>H</sub>	000FFF28 <sub>H</sub>	—
Reserved	54	36	ICR19	453 <sub>H</sub>	324 <sub>H</sub>	000FFF24 <sub>H</sub>	6, 48
Reserved	55	37			320 <sub>H</sub>	000FFF20 <sub>H</sub>	7, 49
Reserved	56	38	ICR20	454 <sub>H</sub>	31C <sub>H</sub>	000FFF1C <sub>H</sub>	8, 50
Reserved	57	39			318 <sub>H</sub>	000FFF18 <sub>H</sub>	9, 51
LIN-USART 2 RX	58	3A	ICR21	455 <sub>H</sub>	314 <sub>H</sub>	000FFF14 <sub>H</sub>	52
LIN-USART 2 TX LIN-USART (FIFO) 2 EoT	59	3B			310 <sub>H</sub>	000FFF10 <sub>H</sub>	53 —
Reserved	60	3C	ICR22	456 <sub>H</sub>	30C <sub>H</sub>	000FFF0C <sub>H</sub>	54
Reserved	61	3D			308 <sub>H</sub>	000FFF08 <sub>H</sub>	55
Reserved	62	3E	ICR23 <sup>*3</sup>	457 <sub>H</sub>	304 <sub>H</sub>	000FFF04 <sub>H</sub>	—
Delayed Interrupt	63	3F			300 <sub>H</sub>	000FFF00 <sub>H</sub>	—

(Continued)

# MB91460E Series

(Continued)

Interrupt	Interrupt number		Interrupt level <sup>*1</sup>		Interrupt vector <sup>*2</sup>		DMA Resource number
	Deci-mal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System reserved <sup>*4</sup>	64	40	(ICR24)	(458H)	2FC <sub>H</sub>	000FFEFCH	—
System reserved <sup>*4</sup>	65	41			2F8 <sub>H</sub>	000FFEF8H	—
LIN-USART (FIFO) 4 RX	66	42	ICR25	459H	2F4 <sub>H</sub>	000FFEF4H	10, 56
LIN-USART (FIFO) 4 TX LIN-USART (FIFO) 4 EoT	67	43			2F0 <sub>H</sub>	000FFEF0H	11, 57 —
LIN-USART (FIFO) 5 RX	68	44	ICR26	45AH	2EC <sub>H</sub>	000FFEECH	12, 58
LIN-USART (FIFO) 5 TX LIN-USART (FIFO) 5 EoT	69	45			2E8 <sub>H</sub>	000FFEE8H	13, 59 —
LIN-USART (FIFO) 6 RX	70	46	ICR27	45BH	2E4 <sub>H</sub>	000FFEE4H	60
LIN-USART (FIFO) 6 TX LIN-USART (FIFO) 6 EoT	71	47			2E0 <sub>H</sub>	000FFEE0H	61 —
LIN-USART (FIFO) 7 RX	72	48	ICR28	45CH	2DC <sub>H</sub>	000FFEDCH	62
LIN-USART (FIFO) 7 TX LIN-USART (FIFO) 7 EoT	73	49			2D8 <sub>H</sub>	000FFED8H	63 —
I <sup>2</sup> C 0 / I <sup>2</sup> C 2	74	4A	ICR29	45DH	2D4 <sub>H</sub>	000FFED4H	—
I <sup>2</sup> C 3	75	4B			2D0 <sub>H</sub>	000FFED0H	—
Reserved	76	4C	ICR30	45EH	2CC <sub>H</sub>	000FFECCH	64
Reserved	77	4D			2C8 <sub>H</sub>	000FFEC8H	65
Reserved	78	4E	ICR31	45FH	2C4 <sub>H</sub>	000FFEC4H	66
Reserved	79	4F			2C0 <sub>H</sub>	000FFEC0H	67
Reserved	80	50	ICR32	460H	2BC <sub>H</sub>	000FFEBCH	68
Reserved	81	51			2B8 <sub>H</sub>	000FFEB8H	69
Reserved	82	52	ICR33	461H	2B4 <sub>H</sub>	000FFEB4H	70
Reserved	83	53			2B0 <sub>H</sub>	000FFEB0H	71
Reserved	84	54	ICR34	462H	2AC <sub>H</sub>	000FFEACh	72
Reserved	85	55			2A8 <sub>H</sub>	000FFEA8H	73
Reserved	86	56	ICR35	463H	2A4 <sub>H</sub>	000FFEA4H	74
Reserved	87	57			2A0 <sub>H</sub>	000FFEA0H	75
Reserved	88	58	ICR36	464H	29C <sub>H</sub>	000FFE9CH	76
Reserved	89	59			298 <sub>H</sub>	000FFE98H	77
Reserved	90	5A	ICR37	465H	294 <sub>H</sub>	000FFE94H	78
Reserved	91	5B			290 <sub>H</sub>	000FFE90H	79

(Continued)

(Continued)

Interrupt	Interrupt number		Interrupt level <sup>*1</sup>		Interrupt vector <sup>*2</sup>		DMA Resource number
	Deci-mal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
Input Capture 0	92	5C	ICR38	466 <sub>H</sub>	28C <sub>H</sub>	000FFE8C <sub>H</sub>	80
Input Capture 1	93	5D			288 <sub>H</sub>	000FFE88 <sub>H</sub>	81
Input Capture 2	94	5E	ICR39	467 <sub>H</sub>	284 <sub>H</sub>	000FFE84 <sub>H</sub>	82
Input Capture 3	95	5F			280 <sub>H</sub>	000FFE80 <sub>H</sub>	83
Input Capture 4	96	60	ICR40	468 <sub>H</sub>	27C <sub>H</sub>	000FFE7C <sub>H</sub>	84
Input Capture 5	97	61			278 <sub>H</sub>	000FFE78 <sub>H</sub>	85
Input Capture 6	98	62	ICR41	469 <sub>H</sub>	274 <sub>H</sub>	000FFE74 <sub>H</sub>	86
Input Capture 7	99	63			270 <sub>H</sub>	000FFE70 <sub>H</sub>	87
Output Compare 0	100	64	ICR42	46A <sub>H</sub>	26C <sub>H</sub>	000FFE6C <sub>H</sub>	88
Output Compare 1	101	65			268 <sub>H</sub>	000FFE68 <sub>H</sub>	89
Output Compare 2	102	66	ICR43	46B <sub>H</sub>	264 <sub>H</sub>	000FFE64 <sub>H</sub>	90
Output Compare 3	103	67			260 <sub>H</sub>	000FFE60 <sub>H</sub>	91
Reserved	104	68	ICR44	46C <sub>H</sub>	25C <sub>H</sub>	000FFE5C <sub>H</sub>	92
Reserved	105	69			258 <sub>H</sub>	000FFE58 <sub>H</sub>	93
Reserved	106	6A	ICR45	46D <sub>H</sub>	254 <sub>H</sub>	000FFE54 <sub>H</sub>	94
Reserved	107	6B			250 <sub>H</sub>	000FFE50 <sub>H</sub>	95
Sound Generator	108	6C	ICR46	46E <sub>H</sub>	24C <sub>H</sub>	000FFE4C <sub>H</sub>	—
Phase Frequency Modulator	109	6D			248 <sub>H</sub>	000FFE48 <sub>H</sub>	—
Reserved	110	6E	ICR47 <sup>*3</sup>	46F <sub>H</sub>	244 <sub>H</sub>	000FFE44 <sub>H</sub>	—
Reserved	111	6F			240 <sub>H</sub>	000FFE40 <sub>H</sub>	—
Reserved	112	70	ICR48	470 <sub>H</sub>	23C <sub>H</sub>	000FFE3C <sub>H</sub>	15, 96
Reserved	113	71			238 <sub>H</sub>	000FFE38 <sub>H</sub>	97
Reserved	114	72	ICR49	471 <sub>H</sub>	234 <sub>H</sub>	000FFE34 <sub>H</sub>	98
Reserved	115	73			230 <sub>H</sub>	000FFE30 <sub>H</sub>	99
PPG4	116	74	ICR50	472 <sub>H</sub>	22C <sub>H</sub>	000FFE2C <sub>H</sub>	100
PPG5	117	75			228 <sub>H</sub>	000FFE28 <sub>H</sub>	101
PPG6	118	76	ICR51	473 <sub>H</sub>	224 <sub>H</sub>	000FFE24 <sub>H</sub>	102
PPG7	119	77			220 <sub>H</sub>	000FFE20 <sub>H</sub>	103
PPG8	120	78	ICR52	474 <sub>H</sub>	21C <sub>H</sub>	000FFE1C <sub>H</sub>	104
PPG9	121	79			218 <sub>H</sub>	000FFE18 <sub>H</sub>	105
PPG10	122	7A	ICR53	475 <sub>H</sub>	214 <sub>H</sub>	000FFE14 <sub>H</sub>	106
PPG11	123	7B			210 <sub>H</sub>	000FFE10 <sub>H</sub>	107

(Continued)

# MB91460E Series

(Continued)

Interrupt	Interrupt number		Interrupt level <sup>*1</sup>		Interrupt vector <sup>*2</sup>		DMA Resource number
	Deci-mal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
PPG12	124	7C	ICR54	476 <sub>H</sub>	20C <sub>H</sub>	000FFE0C <sub>H</sub>	108
PPG13	125	7D			208 <sub>H</sub>	000FFE08 <sub>H</sub>	109
PPG14	126	7E	ICR55	477 <sub>H</sub>	204 <sub>H</sub>	000FFE04 <sub>H</sub>	110
PPG15	127	7F			200 <sub>H</sub>	000FFE00 <sub>H</sub>	111
Up/Down Counter 0	128	80	ICR56	478 <sub>H</sub>	1FC <sub>H</sub>	000FFDFC <sub>H</sub>	—
Reserved	129	81			1F8 <sub>H</sub>	000FFDF8 <sub>H</sub>	—
Up/Down Counter 2	130	82	ICR57	479 <sub>H</sub>	1F4 <sub>H</sub>	000FFDF4 <sub>H</sub>	—
Up/Down Counter 3	131	83			1F0 <sub>H</sub>	000FFDF0 <sub>H</sub>	—
Real Time Clock	132	84	ICR58	47A <sub>H</sub>	1EC <sub>H</sub>	000FFDEC <sub>H</sub>	—
Calibration Unit	133	85			1E8 <sub>H</sub>	000FFDE8 <sub>H</sub>	—
A/D Converter 0	134	86	ICR59	47B <sub>H</sub>	1E4 <sub>H</sub>	000FFDE4 <sub>H</sub>	14, 112
Reserved	135	87			1E0 <sub>H</sub>	000FFDE0 <sub>H</sub>	—
Alarm Comparator 0	136	88	ICR60	47C <sub>H</sub>	1DC <sub>H</sub>	000FFDDC <sub>H</sub>	—
Reserved	137	89			1D8 <sub>H</sub>	000FFDD8 <sub>H</sub>	—
Low Voltage Detection	138	8A	ICR61	47D <sub>H</sub>	1D4 <sub>H</sub>	000FFDD4 <sub>H</sub>	—
SMC Comparator 0 to 5	139	8B			1D0 <sub>H</sub>	000FFDD0 <sub>H</sub>	—
Timebase Overflow	140	8C	ICR62	47E <sub>H</sub>	1CC <sub>H</sub>	000FFDCC <sub>H</sub>	—
PLL Clock Gear	141	8D			1C8 <sub>H</sub>	000FFDC8 <sub>H</sub>	—
DMA Controller	142	8E	ICR63	47F <sub>H</sub>	1C4 <sub>H</sub>	000FFDC4 <sub>H</sub>	—
Main/Sub OSC stability wait	143	8F			1C0 <sub>H</sub>	000FFDC0 <sub>H</sub>	—
Security vector	144	90	—	—	1BC <sub>H</sub>	000FFDBC <sub>H</sub>	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	1B8 <sub>H</sub> to 000 <sub>H</sub>	000FFDB8 <sub>H</sub> to 000FFC00 <sub>H</sub>	—

\*1 : The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

\*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (000FFC00<sub>H</sub>) . The TBR is initialized to this value by a reset. The TBR is set to 000FFC00<sub>H</sub> after the internal boot ROM is executed.

\*3 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0C03<sub>H</sub> : IOS[0])

\*4 : Used by REALOS

\*5 : Memory Protection Unit (MPU) support

## ■ RECOMMENDED SETTINGS

### 1. PLL and Clockgear settings

Please note that for MB91F467EA the core base clock frequencies are valid in the **1.9V** operation mode of the Main regulator and Flash.

#### Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG			
4	2	25	16	24	200	100	
4	2	24	16	24	192	96	.
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

# MB91460E Series

## 2. Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 98MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

**Clock Modulator settings, frequency range and supported supply voltage**

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	88	79.5	98.5	
1	3	026F	84	76.1	93.8	
1	3	026F	80	72.6	89.1	
1	5	02AE	80	68.7	95.8	
2	3	046E	80	68.7	95.8	
1	3	026F	76	69.1	84.5	
1	5	02AE	76	65.3	90.8	
1	7	02ED	76	62	98.1	
2	3	046E	76	65.3	90.8	
3	3	066D	76	62	98.1	
1	3	026F	72	65.5	79.9	
1	5	02AE	72	62	85.8	
1	7	02ED	72	58.8	92.7	
2	3	046E	72	62	85.8	
3	3	066D	72	58.8	92.7	
1	3	026F	68	62	75.3	
1	5	02AE	68	58.7	80.9	
1	7	02ED	68	55.7	87.3	
1	9	032C	68	53	95	
2	3	046E	68	58.7	80.9	
2	5	04AC	68	53	95	
3	3	066D	68	55.7	87.3	
4	3	086C	68	53	95	
1	3	026F	64	58.5	70.7	
1	5	02AE	64	55.3	75.9	
1	7	02ED	64	52.5	82	
1	9	032C	64	49.9	89.1	
1	11	036B	64	47.6	97.6	
2	3	046E	64	55.3	75.9	
2	5	04AC	64	49.9	89.1	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
3	3	066D	64	52.5	82	
4	3	086C	64	49.9	89.1	
5	3	0A6B	64	47.6	97.6	
1	3	026F	60	54.9	66.1	
1	5	02AE	60	51.9	71	
1	7	02ED	60	49.3	76.7	
1	9	032C	60	46.9	83.3	
1	11	036B	60	44.7	91.3	
2	3	046E	60	51.9	71	
2	5	04AC	60	46.9	83.3	
3	3	066D	60	49.3	76.7	
4	3	086C	60	46.9	83.3	
5	3	0A6B	60	44.7	91.3	
1	3	026F	56	51.4	61.6	
1	5	02AE	56	48.6	66.1	
1	7	02ED	56	46.1	71.4	
1	9	032C	56	43.8	77.6	
1	11	036B	56	41.8	84.9	
1	13	03AA	56	39.9	93.8	
2	3	046E	56	48.6	66.1	
2	5	04AC	56	43.8	77.6	
2	7	04EA	56	39.9	93.8	
3	3	066D	56	46.1	71.4	
3	5	06AA	56	39.9	93.8	
4	3	086C	56	43.8	77.6	
5	3	0A6B	56	41.8	84.9	
6	3	0C6A	56	39.9	93.8	
1	3	026F	52	47.8	57	
1	5	02AE	52	45.2	61.2	
1	7	02ED	52	42.9	66.1	
1	9	032C	52	40.8	71.8	
1	11	036B	52	38.8	78.6	
1	13	03AA	52	37.1	86.8	
1	15	03E9	52	35.5	96.9	
2	3	046E	52	45.2	61.2	

(Continued)

# MB91460E Series

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	5	04AC	52	40.8	71.8	
2	7	04EA	52	37.1	86.8	
3	3	066D	52	42.9	66.1	
3	5	06AA	52	37.1	86.8	
4	3	086C	52	40.8	71.8	
5	3	0A6B	52	38.8	78.6	
6	3	0C6A	52	37.1	86.8	
7	3	0E69	52	35.5	96.9	
1	3	026F	48	44.2	52.5	
1	5	02AE	48	41.8	56.4	
1	7	02ED	48	39.6	60.9	
1	9	032C	48	37.7	66.1	
1	11	036B	48	35.9	72.3	
1	13	03AA	48	34.3	79.9	
1	15	03E9	48	32.8	89.1	
2	3	046E	48	41.8	56.4	
2	5	04AC	48	37.7	66.1	
2	7	04EA	48	34.3	79.9	
3	3	066D	48	39.6	60.9	
3	5	06AA	48	34.3	79.9	
4	3	086C	48	37.7	66.1	
5	3	0A6B	48	35.9	72.3	
6	3	0C6A	48	34.3	79.9	
7	3	0E69	48	32.8	89.1	
1	3	026F	44	40.6	48.1	
1	5	02AE	44	38.4	51.6	
1	7	02ED	44	36.4	55.7	
1	9	032C	44	34.6	60.4	
1	11	036B	44	33	66.1	
1	13	03AA	44	31.5	73	
1	15	03E9	44	30.1	81.4	
2	3	046E	44	38.4	51.6	
2	5	04AC	44	34.6	60.4	
2	7	04EA	44	31.5	73	
2	9	0528	44	28.9	92.1	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
3	3	066D	44	36.4	55.7	
3	5	06AA	44	31.5	73	
4	3	086C	44	34.6	60.4	
4	5	08A8	44	28.9	92.1	
5	3	0A6B	44	33	66.1	
6	3	0C6A	44	31.5	73	
7	3	0E69	44	30.1	81.4	
8	3	1068	44	28.9	92.1	
1	3	026F	40	37	43.6	
1	5	02AE	40	34.9	46.8	
1	7	02ED	40	33.1	50.5	
1	9	032C	40	31.5	54.8	
1	11	036B	40	30	59.9	
1	13	03AA	40	28.7	66.1	
1	15	03E9	40	27.4	73.7	
2	3	046E	40	34.9	46.8	
2	5	04AC	40	31.5	54.8	
2	7	04EA	40	28.7	66.1	
2	9	0528	40	26.3	83.3	
3	3	066D	40	33.1	50.5	
3	5	06AA	40	28.7	66.1	
3	7	06E7	40	25.3	95.8	
4	3	086C	40	31.5	54.8	
4	5	08A8	40	26.3	83.3	
5	3	0A6B	40	30	59.9	
6	3	0C6A	40	28.7	66.1	
7	3	0E69	40	27.4	73.7	
8	3	1068	40	26.3	83.3	
9	3	1267	40	25.3	95.8	
1	3	026F	36	33.3	39.2	
1	5	02AE	36	31.5	42	
1	7	02ED	36	29.9	45.3	
1	9	032C	36	28.4	49.2	
1	11	036B	36	27.1	53.8	
1	13	03AA	36	25.8	59.3	

(Continued)

# MB91460E Series

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	15	03E9	36	24.7	66.1	
2	3	046E	36	31.5	42	
2	5	04AC	36	28.4	49.2	
2	7	04EA	36	25.8	59.3	
2	9	0528	36	23.7	74.7	
3	3	066D	36	29.9	45.3	
3	5	06AA	36	25.8	59.3	
3	7	06E7	36	22.8	85.8	
4	3	086C	36	28.4	49.2	
4	5	08A8	36	23.7	74.7	
5	3	0A6B	36	27.1	53.8	
6	3	0C6A	36	25.8	59.3	
7	3	0E69	36	24.7	66.1	
8	3	1068	36	23.7	74.7	
9	3	1267	36	22.8	85.8	
1	3	026F	32	29.7	34.7	
1	5	02AE	32	28	37.3	
1	7	02ED	32	26.6	40.2	
1	9	032C	32	25.3	43.6	
1	11	036B	32	24.1	47.7	
1	13	03AA	32	23	52.5	
1	15	03E9	32	22	58.6	
2	3	046E	32	28	37.3	
2	5	04AC	32	25.3	43.6	
2	7	04EA	32	23	52.5	
2	9	0528	32	21.1	66.1	
2	11	0566	32	19.5	89.1	
3	3	066D	32	26.6	40.2	
3	5	06AA	32	23	52.5	
3	7	06E7	32	20.3	75.9	
4	3	086C	32	25.3	43.6	
4	5	08A8	32	21.1	66.1	
5	3	0A6B	32	24.1	47.7	
5	5	0AA6	32	19.5	89.1	
6	3	0C6A	32	23	52.5	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
7	3	0E69	32	22	58.6	
8	3	1068	32	21.1	66.1	
9	3	1267	32	20.3	75.9	
10	3	1466	32	19.5	89.1	

# MB91460E Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	—	—	50	V/ms	
Power supply voltage 1* <sup>1</sup>	V <sub>DD5R</sub>	– 0.3	+ 6.0	V	
Power supply voltage 2* <sup>1</sup>	V <sub>DD5</sub>	– 0.3	+ 6.0	V	
Power supply voltage 3* <sup>1</sup>	HV <sub>DD5</sub>	– 0.3	+ 6.0	V	
Power supply voltage 4* <sup>1</sup>	V <sub>DD35</sub>	– 0.3	+ 6.0	V	
Relationship of the supply voltages	HV <sub>DD5</sub>	V <sub>DD5-0.3</sub>	V <sub>DD5+0.3</sub>	V	SMC mode
		V <sub>ss5-0.3</sub>	V <sub>DD5+0.3</sub>	V	General purpose port mode
	AV <sub>cc5</sub>	V <sub>DD5-0.3</sub>	V <sub>DD5+0.3</sub>	V	At least one pin of the Ports 25 to 29 (SMC, ANn) is used as digital input or output.
		V <sub>ss5-0.3</sub>	V <sub>DD5+0.3</sub>	V	All pins of the Ports 25 to 29 (SMC, ANn) follow the condition of V <sub>IA</sub>
Analog power supply voltage* <sup>1</sup>	AV <sub>cc5</sub>	– 0.3	+ 6.0	V	*2
Analog reference power supply voltage* <sup>1</sup>	AVRH5	– 0.3	+ 6.0	V	*2
Input voltage 1* <sup>1</sup>	V <sub>I1</sub>	V <sub>ss5</sub> – 0.3	V <sub>DD5</sub> + 0.3	V	
Input voltage 2* <sup>1</sup>	V <sub>I2</sub>	V <sub>ss5</sub> – 0.3	V <sub>DD35</sub> + 0.3	V	External bus
Input voltage 3* <sup>1</sup>	V <sub>I3</sub>	HV <sub>ss5</sub> – 0.3	HV <sub>DD5</sub> + 0.3	V	Stepper motor controller
Analog pin input voltage* <sup>1</sup>	V <sub>IA</sub>	AV <sub>ss5</sub> – 0.3	AV <sub>cc5</sub> + 0.3	V	
Output voltage 1* <sup>1</sup>	V <sub>O1</sub>	V <sub>ss5</sub> – 0.3	V <sub>DD5</sub> + 0.3	V	
Output voltage 2* <sup>1</sup>	V <sub>O2</sub>	V <sub>ss5</sub> – 0.3	V <sub>DD35</sub> + 0.3	V	External bus
Output voltage 3* <sup>1</sup>	V <sub>O3</sub>	HV <sub>ss5</sub> – 0.3	HV <sub>DD5</sub> + 0.3	V	Stepper motor controller
Maximum clamp current	I <sub>CLAMP</sub>	– 4.0	+ 4.0	mA	*3
Total maximum clamp current	$\Sigma  I_{CLAMP} $	—	20	mA	*3
“L” level maximum output current* <sup>4</sup>	I <sub>OL</sub>	—	10	mA	
		—	40	mA	Stepper motor controller
“L” level average output current* <sup>5</sup>	I <sub>OLAV</sub>	—	8	mA	
		—	30	mA	Stepper motor controller
“L” level total maximum output current	$\Sigma I_{OL}$	—	100	mA	
		—	360	mA	Stepper motor controller
“L” level total average output current* <sup>6</sup>	$\Sigma I_{OLAV}$	—	50	mA	
		—	230	mA	Stepper motor controller
“H” level maximum output current* <sup>4</sup>	I <sub>OH</sub>	—	– 10	mA	
		—	– 40	mA	Stepper motor controller

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"H" level average output current* <sup>5</sup>	I <sub>OHAV</sub>	—	— 4	mA	
		—	— 30	mA	Stepper motor controller
"H" level total maximum output current	ΣI <sub>OH</sub>	—	— 100	mA	
		—	— 360	mA	Stepper motor controller
"H" level total average output current* <sup>6</sup>	ΣI <sub>OHAV</sub>	—	— 25	mA	
		—	— 230	mA	Stepper motor controller
Permitted power dissipation * <sup>7</sup>	P <sub>D</sub>	—	1100 * <sup>8</sup>	mW	at T <sub>A</sub> ≤ 85 °C
		—	1100 * <sup>8</sup>	mW	at T <sub>A</sub> ≤ 105 °C, no Flash program/erase * <sup>9</sup>
		—	555 * <sup>8</sup>	mW	at T <sub>A</sub> ≤ 105 °C
Operating temperature	T <sub>A</sub>	— 40	+ 105	°C	
Storage temperature	T <sub>Stg</sub>	— 55	+ 150	°C	

\*1 : The parameter is based on V<sub>SS5</sub> = HV<sub>SS5</sub> = AV<sub>SS5</sub> = 0.0 V.

\*2 : AV<sub>CC5</sub> and AVR<sub>H5</sub> must not exceed V<sub>DD5</sub> + 0.3 V.

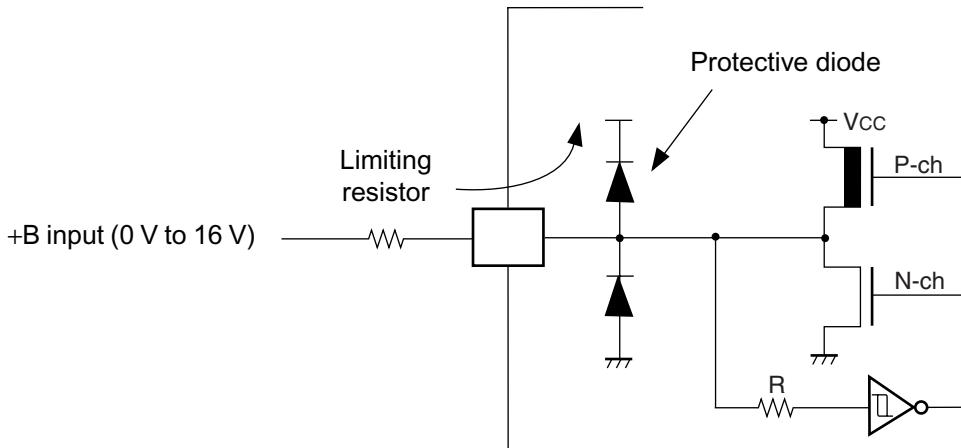
\*3 :

- Use within recommended operating conditions.
- Use with DC voltage (current).
- +B signals are input signals that exceed the V<sub>DD5</sub> voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time, either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.

# MB91460E Series

- Do not leave +B input pins open.
- Example of recommended circuit :

- Input/output equivalent circuit



\*4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

\*5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

\*6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

\*7 : The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$$P_D = P_{IO} + P_{INT}$$

$P_{IO} = \sum (|V_{SS}-V_{OL}| * I_{OL} + |V_{DD}-V_{OH}| * I_{OH})$  (IO load power dissipation, sum is performed on all IO ports)

$$P_{INT} = V_{DD5}R * I_{CC} + A V_{CC5} * I_A + A V_{RH5} * I_R$$
 (internal power dissipation)

\*8 : Worst case value for the QFP package mounted on a 4-layer PCB at specified  $T_A$  without air flow.

\*9 : Please contact Fujitsu for reliability limitations when using under these conditions.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended operating conditions

(V<sub>SS5</sub> = AV<sub>SS5</sub> = 0.0 V)

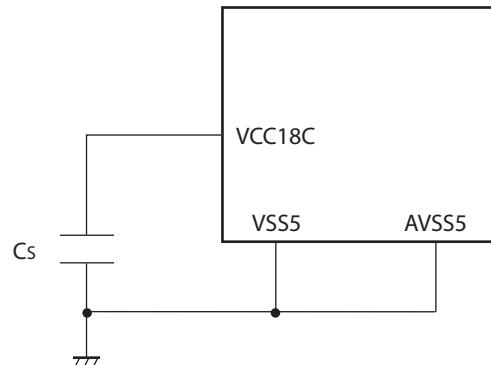
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V <sub>DD5</sub>	3.0	—	5.5	V	
	V <sub>DD5R</sub>	3.0	—	5.5	V	Internal regulator
	V <sub>DD35</sub>	3.0	—	5.5	V	External bus
	HV <sub>DD5</sub>	4.5	—	5.5	V	Stepper motor controller
		3.0	—	5.5	V	Stepper motor controller (when all pins are used as general-purpose ports)
	AV <sub>cc5</sub>	3.0	—	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C <sub>s</sub>	—	4.7	—	μF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		—	—	50	V/ms	
Operating temperature	T <sub>A</sub>	– 40	—	+ 105	°C	
Stepper motor control slew rate			40		ns	C <sub>load</sub> = 0 pF
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz → 16 ... 100MHz)				0.6	ms	
ESD Protection (Human body model)	V <sub>surge</sub>	2			kV	R <sub>discharge</sub> = 1.5kΩ C <sub>discharge</sub> = 100pF
RC Oscillator	f <sub>RC100kHz</sub>	50	100	200	kHz	V <sub>DDCORE</sub> ≥ 1.65V
	f <sub>RC2MHz</sub>	1	2	4	MHz	

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

# MB91460E Series



### 3. DC characteristics

Note: In the following tables, "V<sub>DD</sub>" means V<sub>DD35</sub> for pins of ext. bus or HV<sub>DD5</sub> for SMC pins or V<sub>DD5</sub> for other pins.

In the following tables, "V<sub>ss</sub>" means HV<sub>ss5</sub> for ground Pins of the stepper motor and V<sub>ss5</sub> for the other pins.

(V<sub>DD5</sub> = AV<sub>CC5</sub> = 3.0 V to 5.5 V, V<sub>ss5</sub> = AV<sub>ss5</sub> = 0 V, T<sub>A</sub> = -40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V <sub>IH</sub>	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	0.8 × V <sub>DD</sub>	—	V <sub>DD</sub> + 0.3	V	CMOS hysteresis input
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	0.7 × V <sub>DD</sub>	—	V <sub>DD</sub> + 0.3	V	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V
		—	AUTOMOTIVE Hysteresis input is selected	0.74 × V <sub>DD</sub>	—	V <sub>DD</sub> + 0.3	V	3 V ≤ V <sub>DD</sub> < 4.5 V
		—	Port inputs if TTL input is selected	2.0	—	V <sub>DD</sub> + 0.3	V	
	V <sub>IHR</sub>	INITX	—	0.8 × V <sub>DD</sub>	—	V <sub>DD</sub> + 0.3	V	INITX input pin (CMOS Hysteresis)
	V <sub>IHM</sub>	MD_2 to MD_0	—	V <sub>DD</sub> - 0.3	—	V <sub>DD</sub> + 0.3	V	Mode input pins
	V <sub>IHXOS</sub>	X0, X0A	—	2.5	—	V <sub>DD</sub> + 0.3	V	External clock in "Oscillation mode"
Input "L" voltage	V <sub>IL</sub>	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	V <sub>ss</sub> - 0.3	—	0.2 × V <sub>DD</sub>	V	
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	V <sub>ss</sub> - 0.3	—	0.3 × V <sub>DD</sub>	V	
		—	Port inputs if AUTOMOTIVE Hysteresis input is selected	V <sub>ss</sub> - 0.3	—	0.5 × V <sub>DD</sub>	V	4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V
		—	Port inputs if TTL input is selected	V <sub>ss</sub> - 0.3	—	0.46 × V <sub>DD</sub>	V	3 V ≤ V <sub>DD</sub> < 4.5 V
	V <sub>ILR</sub>	INITX	—	V <sub>ss</sub> - 0.3	—	0.8	V	
	V <sub>ILM</sub>	MD_2 to MD_0	—	V <sub>ss</sub> - 0.3	—	V <sub>ss</sub> + 0.3	V	Mode input pins
	V <sub>ILXDS</sub>	X0, X0A	—	V <sub>ss</sub> - 0.3	—	0.5	V	External clock in "Oscillation mode"

# MB91460E Series

( $V_{DD5} = AV_{CC5} = 3.0\text{ V}$  to  $5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "L" voltage	$V_{ILXDF}$	X0	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	External clock in "Fast Clock Input mode"
Output "H" voltage	$V_{OH2}$	Normal outputs	$4.5V \leq V_{DD} \leq 5.5V$ , $I_{OH} = -2\text{mA}$	$V_{DD} - 0.5$	—	—	V	Driving strength set to 2 mA
			$3.0V \leq V_{DD} \leq 4.5V$ , $I_{OH} = -1.6\text{mA}$		—	—		
	$V_{OH5}$	Normal outputs	$4.5V \leq V_{DD} \leq 5.5V$ , $I_{OH} = -5\text{mA}$	$V_{DD} - 0.5$	—	—	V	Driving strength set to 5 mA
			$3.0V \leq V_{DD} \leq 4.5V$ , $I_{OH} = -3\text{mA}$		—	—		
Output "L" voltage	$V_{OH3}$	$I^2C$ outputs	$3.0V \leq V_{DD} \leq 5.5V$ , $I_{OH} = -3\text{mA}$	$V_{DD} - 0.5$	—	—	V	
	$V_{OH30}$	High current outputs	$4.5V \leq V_{DD} \leq 5.5V$ , $T_A = -40\text{ }^\circ\text{C}$ , $I_{OH} = -40\text{mA}$	$V_{DD} - 0.5$	—	—	V	Driving strength set to 30mA
			$4.5V \leq V_{DD} \leq 5.5V$ , $I_{OH} = -30\text{mA}$		—	—		
			$3.0V \leq V_{DD} \leq 4.5V$ , $I_{OH} = -20\text{mA}$		—	—		
Input leakage current	$I_{IL}$	$P_{nn\_m}$ *1	$3.0V \leq V_{DD} \leq 5.5V$ $V_{SS5} < V_I < V_{DD}$ $T_A=25\text{ }^\circ\text{C}$	—	—	0.4	$\mu\text{A}$	Driving strength set to 2 mA
			$3.0V \leq V_{DD} \leq 5.5V$ $V_{SS5} < V_I < V_{DD}$ $T_A=105\text{ }^\circ\text{C}$	—	—	0.4		
	$I_{IL}$	$P_{nn\_m}$ *1	$3.0V \leq V_{DD} \leq 5.5V$ $V_{SS5} < V_I < V_{DD}$ $T_A=25\text{ }^\circ\text{C}$	— 1	—	+ 1	$\mu\text{A}$	Driving strength set to 5 mA
			$3.0V \leq V_{DD} \leq 5.5V$ $V_{SS5} < V_I < V_{DD}$ $T_A=105\text{ }^\circ\text{C}$	— 3	—	+ 3		

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Analog input leakage current	I <sub>AIN</sub>	ANn <sup>*2</sup>	3.0V ≤ V <sub>DD</sub> ≤ 5.5V T <sub>A</sub> =25 °C	- 1	—	+ 1	μA	
			3.0V ≤ V <sub>DD</sub> ≤ 5.5V T <sub>A</sub> =105 °C	- 3	—	+ 3	μA	
Sum input leakage current	Σ I <sub>L</sub>	P <sub>nn_m</sub> <sup>*3</sup> , ALARM <sub>-0</sub>	V <sub>DD5</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS5</sub> , AV <sub>CC5</sub> ≥ V <sub>IN</sub> ≥ AV <sub>SS5</sub> Σ (1 to n) [max( I <sub>LHil</sub>  ,  I <sub>LLil</sub>  )]	-	8	30	μA	n = number of IO = 65 GPIO + 1 ALARM I <sub>LH</sub> : leakage at high level input; I <sub>LL</sub> : leakage at low level input
Pull-up resistance	R <sub>UP</sub>	P <sub>nn_m</sub> <sup>*4</sup> INITX	3.0V ≤ V <sub>DD</sub> ≤ 3.6V	40	100	160	kΩ	
			4.5V ≤ V <sub>DD</sub> ≤ 5.5V	25	50	100		
Pull-down resistance	R <sub>DOWN</sub>	P <sub>nn_m</sub> <sup>*5</sup>	3.0V ≤ V <sub>DD</sub> ≤ 3.6V	40	100	180	kΩ	
			4.5V ≤ V <sub>DD</sub> ≤ 5.5V	25	50	100		
Input capacitance	C <sub>IN</sub>	All except V <sub>DD5</sub> , V <sub>DD5R</sub> , V <sub>SS5</sub> , AV <sub>CC5</sub> , AV <sub>SS</sub> , AVRH5	f = 1 MHz	-	5	15	pF	

1. P<sub>nn\_m</sub> includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
2. ANn includes all pins where AN channels are enabled.
3. P<sub>nn\_m</sub> includes all GPIO pins beside the external bus pins (P00 to P13) and Stepper Motor pins (P25, P26, P27). Analog (AN) channels and PullUp/PullDown are disabled.
4. P<sub>nn\_m</sub> includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
5. P<sub>nn\_m</sub> includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.

(Continued)

# MB91460E Series

(Continued)

( $V_{DD5} = AV_{CC5} = 3.0\text{ V to }5.5\text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current MB91F467EA	I <sub>cc</sub>	V <sub>DD5R</sub>	MB91F467EA: CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	—	110	140	mA	Code fetch from Flash
	I <sub>ccH</sub>	V <sub>DD5R</sub> * <sup>1</sup>	T <sub>A</sub> = + 25 °C	—	10	30	μA	ShutDown mode with RTC running on 32 kHz Sub clock * <sup>2</sup>
			T <sub>A</sub> = + 85 °C	—	80	150	μA	
			T <sub>A</sub> = + 105 °C	—	160	300	μA	
			T <sub>A</sub> = + 25 °C	—	15	35	μA	
			T <sub>A</sub> = + 85 °C	—	85	160	μA	
			T <sub>A</sub> = + 105 °C	—	170	320	μA	
			T <sub>A</sub> = + 25 °C	—	30	100	μA	At STOP mode * <sup>4</sup>
			T <sub>A</sub> = + 85 °C	—	450	1000	μA	
			T <sub>A</sub> = + 105 °C	—	1000	2200	μA	
			T <sub>A</sub> = + 25 °C	—	140	300	μA	RTC : 4 MHz mode * <sup>5</sup>
			T <sub>A</sub> = + 85 °C	—	500	1200	μA	
			T <sub>A</sub> = + 105 °C	—	1000	2400	μA	
			T <sub>A</sub> = + 25 °C	—	120	200	μA	RTC : 100 kHz mode * <sup>6</sup>
			T <sub>A</sub> = + 85 °C	—	500	1100	μA	
			T <sub>A</sub> = + 105 °C	—	1000	2300	μA	
	I <sub>LVE</sub>	V <sub>DD5</sub>	—	—	70	150	μA	External low voltage detection
	I <sub>LVI</sub>	V <sub>DD5R</sub>	—	—	50	100	μA	Internal low voltage detection
	I <sub>osc</sub>	V <sub>DD5</sub>	—	—	250	500	μA	Main clock (4 MHz)
			—	—	20	40	μA	Sub clock (32 kHz)

1. Current on regulator supply pin V<sub>DD5R</sub> does not include I<sub>osc</sub> and I<sub>cc</sub> of the I/O ring.
2. ShutDown mode with standby RAM enabled, sub regulator set to 1.2V, Low voltage detection disabled. Same current consumption if RTC and Sub oscillator are disabled.
3. ShutDown mode with standby RAM enabled, sub regulator set to 1.2V, Low voltage detection disabled, RC oscillator enabled 100 kHz.
4. STOP mode, sub regulator set to 1.2V, Low voltage detection disabled, RC oscillator disabled.
5. STOP mode, sub regulator set to 1.2V, Low voltage detection disabled, RC oscillator disabled, Main oscillator enabled.
6. STOP mode, sub regulator set to 1.2V, Low voltage detection disabled, RC oscillator enabled 100 kHz.

## 4. A/D converter characteristics

( $V_{DD5} = AV_{CC5} = 3.0 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	-3	—	+3	LSB	
Nonlinearity error	—	—	-2.5	—	+2.5	LSB	
Differential nonlinearity error	—	—	-1.9	—	+1.9	LSB	
Zero reading voltage	$V_{OT}$	ANn	AVRL - 1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	$V_{FST}$	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	$T_{comp}$	—	0.6	—	t.b.d. <sup>1</sup>	$\mu\text{s}$	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$
			2.0	—	t.b.d. <sup>1</sup>	$\mu\text{s}$	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$
Sampling time	$T_{samp}$	—	0.4	—	—	$\mu\text{s}$	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$ , $R_{EXT} < 2 \text{ k}\Omega$
			1.0	—	—	$\mu\text{s}$	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$ , $R_{EXT} < 1 \text{ k}\Omega$
Conversion time	$T_{conv}$	—	1.0	—	—	$\mu\text{s}$	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$
			3.0	—	—	$\mu\text{s}$	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$
Input capacitance	$C_{IN}$	ANn	—	—	11	pF	
Input resistance	$R_{IN}$	ANn	—	—	2.6	$\text{k}\Omega$	$4.5 \text{ V} \leq AV_{CC5} \leq 5.5 \text{ V}$
			—	—	12.1	$\text{k}\Omega$	$3.0 \text{ V} \leq AV_{CC5} \leq 4.5 \text{ V}$
Analog input leakage current	$I_{AIN}$	ANn	-1	—	+1	$\mu\text{A}$	$T_A = +25 \text{ }^\circ\text{C}$
			-3	—	+3	$\mu\text{A}$	$T_A = +105 \text{ }^\circ\text{C}$
Analog input voltage range	$V_{AIN}$	ANn	AVRL	—	AVRH	V	
Offset between input channels	—	ANn	—	—	4	LSB	

1. Parameter is under re-evaluation.

(Continued)

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

# MB91460E Series

(Continued)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	0.75 × AV <sub>cc5</sub>	—	AV <sub>cc5</sub>	V	
	AVRL	AVss5	AVss5	—	AV <sub>cc5</sub> × 0.25	V	
Power supply current	I <sub>A</sub>	AV <sub>cc5</sub>	—	2.5	5	mA	A/D Converter active
	I <sub>AH</sub>	AV <sub>cc5</sub>	—	—	5	μA	A/D Converter not operated <sup>*1</sup>
Reference voltage current	I <sub>R</sub>	AVRH5	—	0.7	1	mA	A/D Converter active
	I <sub>RH</sub>	AVRH5	—	—	5	μA	A/D Converter not operated <sup>*2</sup>

<sup>\*1</sup> : Supply current at AV<sub>cc5</sub>, if A/D converter and ALARM comparator are not operating,  
(V<sub>DD5</sub> = AV<sub>cc5</sub> = AVRH = 5.0 V)

<sup>\*2</sup> : Input current at AVRH5, if A/D converter is not operating, (V<sub>DD5</sub> = AV<sub>cc5</sub> = AVRH = 5.0 V)

## Sampling Time Calculation

$$T_{\text{samp}} = (2.6 \text{ kOhm} + R_{\text{EXT}}) \times 11\text{pF} \times 7; \text{ for } 4.5V \leq AV_{\text{cc5}} \leq 5.5V$$

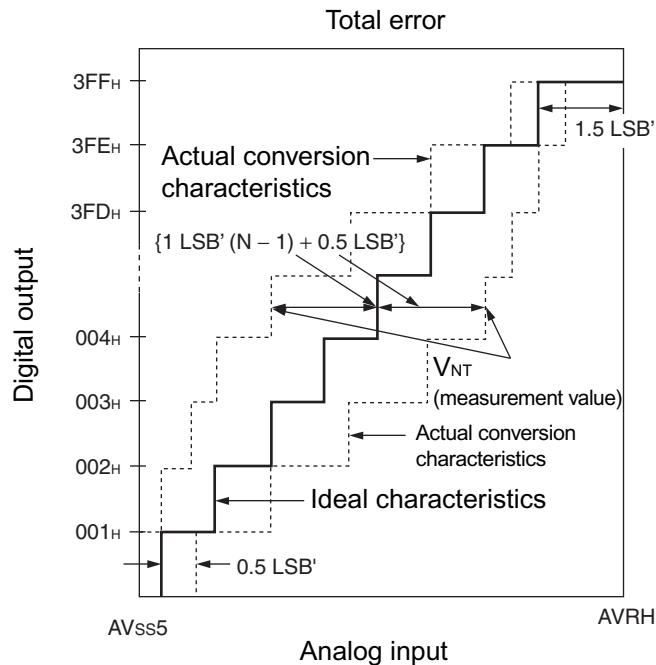
$$T_{\text{samp}} = (12.1 \text{ kOhm} + R_{\text{EXT}}) \times 11\text{pF} \times 7; \text{ for } 3.0V \leq AV_{\text{cc5}} \leq 4.5V$$

## Conversion Time Calculation

$$T_{\text{conv}} = T_{\text{samp}} + T_{\text{comp}}$$

## Definition of A/D converter terms

- Resolution  
Analog variation that is recognizable by the A/D converter.
- Nonlinearity error  
Deviation between actual conversion characteristics and a straight line connecting the zero transition point (00 0000 0000<sub>B</sub> ↔ 00 0000 0001<sub>B</sub>) and the full scale transition point (11 1111 1110<sub>B</sub> ↔ 11 1111 1111<sub>B</sub>).
- Differential nonlinearity error  
Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.
- Total error  
This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



$$1\text{LSB}' \text{ (ideal value)} = \frac{\text{AVRH} - \text{AV}_{ss5}}{1024} \text{ [V]}$$

$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{LSB}' \times (N - 1) + 0.5 \text{LSB}'\}}{1 \text{LSB}'}$$

$N$  : A/D converter digital output value

$$V_{ot}' \text{ (ideal value)} = \text{AV}_{ss5} + 0.5 \text{LSB}' \text{ [V]}$$

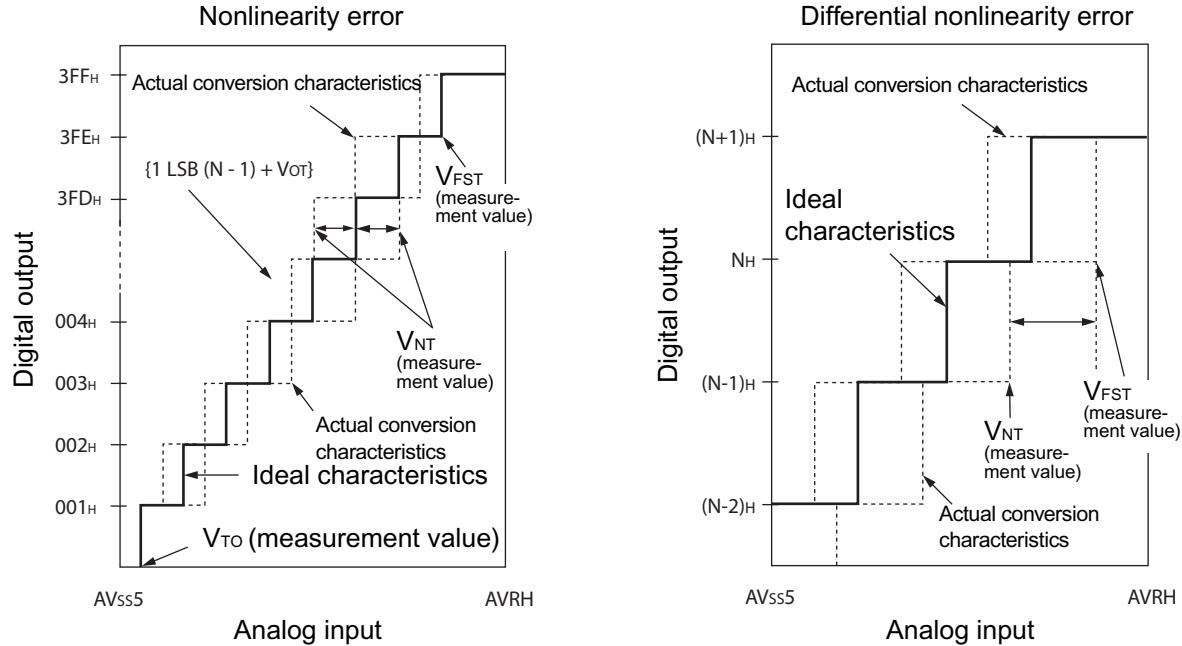
$$V_{fst}' \text{ (ideal value)} = \text{AVRH} - 1.5 \text{LSB}' \text{ [V]}$$

$V_{NT}$  : Voltage at which the digital output changes from  $(N + 1)_H$  to  $N_H$

(Continued)

# MB91460E Series

(Continued)



$$\text{Nonlinearity error of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{OT}\}}{1\text{LSB}} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 \text{ [LSB]}$$

$$1\text{LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

$V_{OT}$  : Voltage at which the digital output changes from 000H to 001H.

$V_{FST}$  : Voltage at which the digital output changes from 3FEH to 3FFH.

## 5. Alarm comparator characteristics

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I <sub>A5ALMF</sub>	AV <sub>cc5</sub>	—	25	40	µA	Alarm comparator enabled in fast mode (per channel) *1
	I <sub>A5ALMS</sub>		—	7	10	µA	Alarm comparator enabled in normal mode (per channel) *1
	I <sub>A5ALMH</sub>		—	—	5	µA	Alarm comparator disabled
ALARM pin input current	I <sub>ALIN</sub>	ALARM_n	— 1	—	+ 1	µA	T <sub>A</sub> =25 °C
			— 3	—	+ 3	µA	T <sub>A</sub> =105 °C
ALARM pin input voltage range	V <sub>ALIN</sub>		0	—	AV <sub>cc5</sub>	V	
Alarm upper limit voltage	V <sub>IAH</sub>		AV <sub>cc5</sub> × 0.78 — 3%	AV <sub>cc5</sub> × 0.78	AV <sub>cc5</sub> × 0.78 + 3%	V	
Alarm lower limit voltage	V <sub>IAL</sub>		AV <sub>cc5</sub> × 0.36 — 5%	AV <sub>cc5</sub> × 0.36	AV <sub>cc5</sub> × 0.36 + 5%	V	
Alarm hysteresis voltage	V <sub>IAHYS</sub>		50	—	250	mV	
Alarm input resistance	R <sub>IN</sub>		5	—	—	MΩ	
Comparison time	t <sub>COMPF</sub>		—	0.1	0.2	µs	Alarm comparator enabled in fast mode *1
	t <sub>COMPS</sub>		—	1	2	µs	Alarm comparator enabled in normal mode *1

Note: \*1 : The fast Alarm Comparator mode is enabled by setting ACSR.MD=1  
Setting ACSR.MD=0 sets the normal mode.

# MB91460E Series

## 6. FLASH memory program/erase characteristics

### 6.1. MB91F467EA

( $T_A = 25^\circ\text{C}$ ,  $V_{\text{cc}} = 5.0\text{V}$ )

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.5	2.0	s	Erasure programming time not included
Chip erase time	-	$n \times 0.5$	$n \times 2.0$	s	$n$ is the number of Flash sector of the device
Word (16 or 32-bit width) programming time	-	6	100	$\mu\text{s}$	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

\*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at  $85^\circ\text{C}$ )

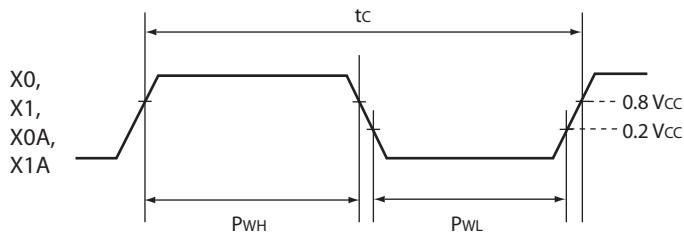
## 7. AC characteristics

### 7.1. Clock timing

( $V_{DD5} = 3.0$  V to  $5.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to  $+105$  °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	fc	X0	3.5	4	16	MHz	Opposite phase external supply or crystal
		X1	3.5	4	8	MHz	Opposite phase external supply or ceramic resonator
		X0A X1A	32	32.768	100	kHz	

- Clock timing condition

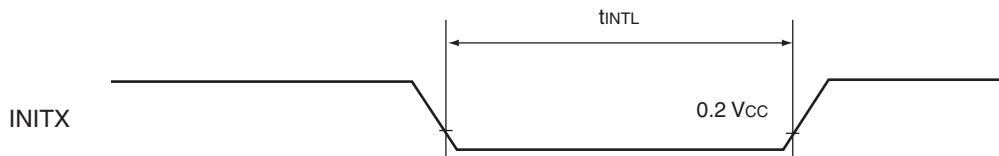


# MB91460E Series

## 7.2. Reset input ratings

( $V_{DD5} = 3.0 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	$t_{INTL}$	INITX	—	10	—	ms
				20	—	$\mu\text{s}$



### 7.3. LIN-USART Timings at $V_{DD5} = 3.0$ to $5.5$ V

- Conditions during AC measurements
- All AC tests were measured under the following conditions:
  - $-I_{O\text{drive}} = 5$  mA
  - $-V_{DD5} = 3.0$  V to  $5.5$  V,  $I_{\text{load}} = 3$  mA
  - $-V_{SS5} = 0$  V
  - $-T_a = -40$  °C to  $+105$  °C
  - $-C_l = 50$  pF (load capacity value of pins when testing)
  - $-V_{OL} = 0.2 \times V_{DD5}$
  - $-V_{OH} = 0.8 \times V_{DD5}$
  - $-EPILR = 0$ ,  $PILR = 1$  (Automotive Level = worst case)

( $V_{DD5} = 3.0$  V to  $5.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_a = -40$  °C to  $+105$  °C)

Parameter	Symbol	Pin name	Condition	$V_{DD5} = 3.0$ V to $4.5$ V		$V_{DD5} = 4.5$ V to $5.5$ V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	$t_{SCYCI}$	SCKn	Internal clock operation (master mode)	$4 t_{CLKP}$	—	$4 t_{CLKP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVI}$	SCKn SOTn		— 30	30	— 20	20	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{OVSHI}$	SCKn SOTn		$m \times t_{CLKP} - 30^*$	—	$m \times t_{CLKP} - 20^*$	—	ns
Valid SIN $\rightarrow$ SCK $\uparrow$ setup time	$t_{IVSHI}$	SCKn SINn		$t_{CLKP} + 55$	—	$t_{CLKP} + 45$	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	$t_{SHIXI}$	SCKn SINn		0	—	0	—	ns
Serial clock "H" pulse width	$t_{SHSLE}$	SCKn	External clock operation (slave mode)	$t_{CLKP} + 10$	—	$t_{CLKP} + 10$	—	ns
Serial clock "L" pulse width	$t_{LSLSE}$	SCKn		$t_{CLKP} + 10$	—	$t_{CLKP} + 10$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVE}$	SCKn SOTn		—	$2 t_{CLKP} + 55$	—	$2 t_{CLKP} + 45$	ns
Valid SIN $\rightarrow$ SCK $\uparrow$ setup time	$t_{IVSHE}$	SCKn SINn		10	—	10	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	$t_{SHIXE}$	SCKn SINn		$t_{CLKP} + 10$	—	$t_{CLKP} + 10$	—	ns
SCK rising time	$t_{FE}$	SCKn		—	20	—	20	ns
SCK falling time	$t_{RE}$	SCKn		—	20	—	20	ns

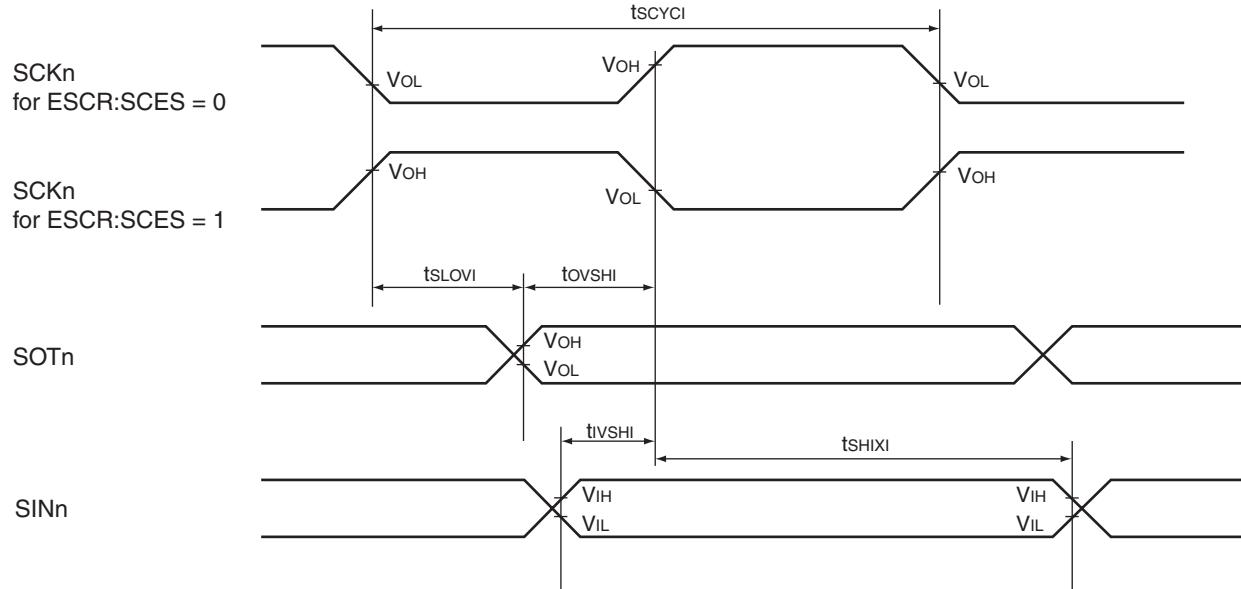
\* : Parameter m depends on  $t_{SCYCI}$  and can be calculated as :

- if  $t_{SCYCI} = 2^*k*t_{CLKP}$ , then  $m = k$ , where k is an integer  $> 2$
- if  $t_{SCYCI} = (2^*k + 1)*t_{CLKP}$ , then  $m = k + 1$ , where k is an integer  $> 1$

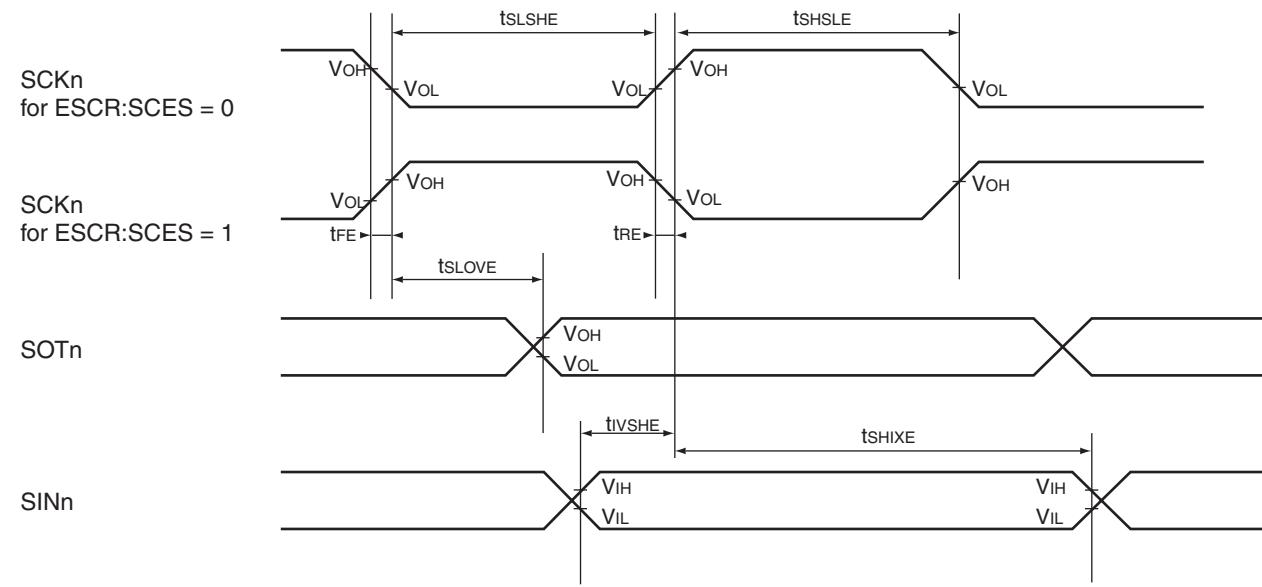
Notes : • The above values are AC characteristics for CLK synchronous mode.  
•  $t_{CLKP}$  is the cycle time of the peripheral clock.

# MB91460E Series

- Internal clock mode (master mode)



- External clock mode (slave mode)



#### 7.4. I<sup>2</sup>C AC Timings at V<sub>DD5</sub> = 3.0 to 5.5 V

- Conditions during AC measurements

All AC tests were measured under the following conditions:

- I<sub>drive</sub> = 3 mA
- V<sub>DD5</sub> = 3.0 V to 5.5 V, I<sub>load</sub> = 3 mA
- V<sub>SS5</sub> = 0 V
- T<sub>A</sub> = -40 °C to +105 °C
- C<sub>I</sub> = 50 pF
- V<sub>OL</sub> = 0.3 × V<sub>DD5</sub>
- V<sub>OH</sub> = 0.7 × V<sub>DD5</sub>
- EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × V<sub>DD5</sub>/0.7 × V<sub>DD5</sub>)

Fast mode:

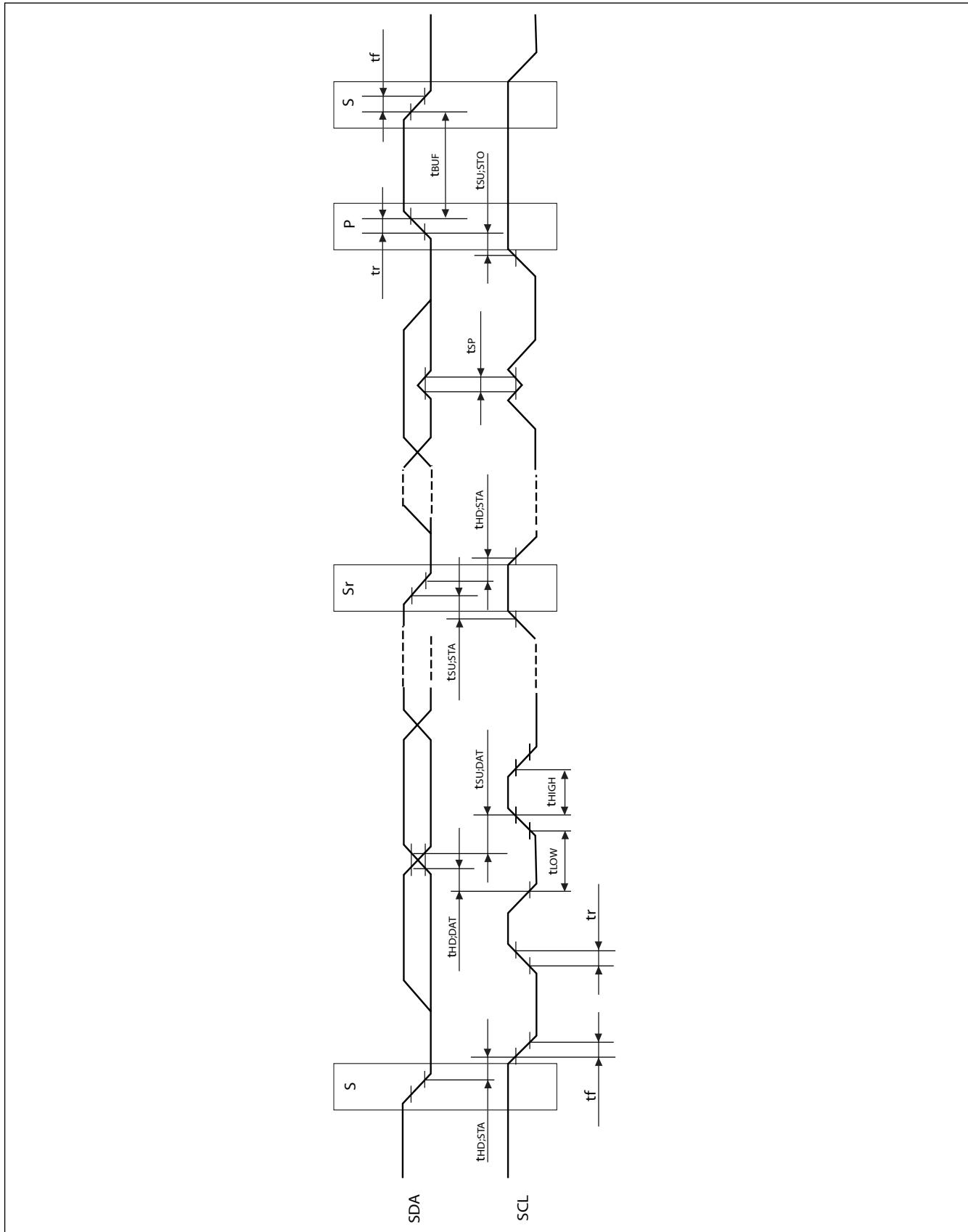
(V<sub>DD5</sub> = 3.0 V to 5.5 V, V<sub>SS5</sub> = AV<sub>SS5</sub> = 0 V, T<sub>A</sub> = -40 °C to +105 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f <sub>SCL</sub>	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t <sub>HD;STA</sub>	SCLn, SDAn	0.6	—	μs	
LOW period of the SCL clock	t <sub>LOW</sub>	SCLn	1.3	—	μs	
HIGH period of the SCL clock	t <sub>HIGH</sub>	SCLn	0.6	—	μs	
Setup time for a repeated START condition	t <sub>SU;STA</sub>	SCLn, SDAn	0.6	—	μs	
Data hold time for I <sup>2</sup> C-bus devices	t <sub>HD;DAT</sub>	SCLn, SDAn	0	0.9	μs	
Data setup time	t <sub>SU;DAT</sub>	SCLn SDAn	100	—	ns	
Rise time of both SDA and SCL signals	t <sub>r</sub>	SCLn, SDAn	20 + 0.1C <sub>b</sub>	300	ns	
Fall time of both SDA and SCL signals	t <sub>f</sub>	SCLn, SDAn	20 + 0.1C <sub>b</sub>	300	ns	
Setup time for STOP condition	t <sub>SU;STO</sub>	SCLn, SDAn	0.6	—	μs	
Bus free time between a STOP and START condition	t <sub>BUF</sub>	SCLn, SDAn	1.3	—	μs	
Capacitive load for each bus line	C <sub>b</sub>	SCLn, SDAn	—	400	pF	
Pulse width of spike suppressed by input filter	t <sub>SP</sub>	SCLn, SDAn	0	(1..1.5) × t <sub>CLKP</sub>	ns	*1

1. The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I<sup>2</sup>C signals (SDA, SCL) and peripheral clock

Note: t<sub>CLKP</sub> is the cycle time of the peripheral clock.

# MB91460E Series

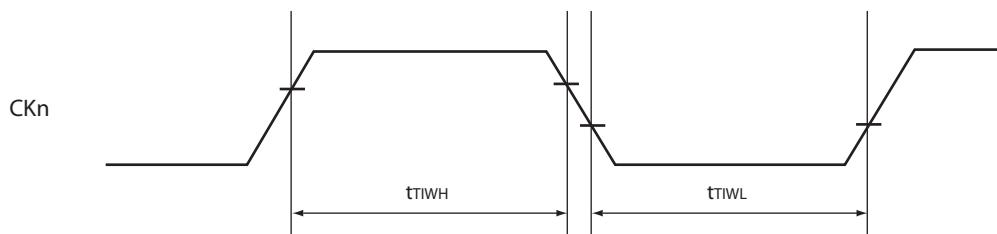


## 7.5. Free-run timer clock

( $V_{DD5} = 3.0 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	$t_{TIWH}$ $t_{TIWL}$	CKn	—	$4t_{CLKP}$	—	ns

Note :  $t_{CLKP}$  is the cycle time of the peripheral clock.

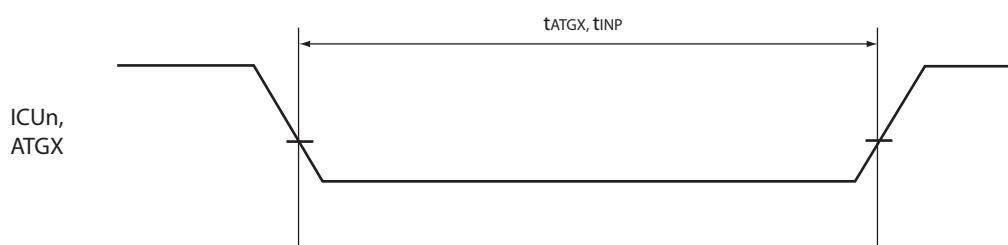


## 7.6. Trigger input timing

( $V_{DD5} = 3.0 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	$t_{INP}$	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	$t_{ATGX}$	ATGX	—	$5t_{CLKP}$	—	ns

Note :  $t_{CLKP}$  is the cycle time of the peripheral clock.



## 7.7. External Bus AC Timings at $V_{DD35} = 4.5$ to $5.5$ V

- Conditions during AC measurements

All AC tests were measured under the following conditions:

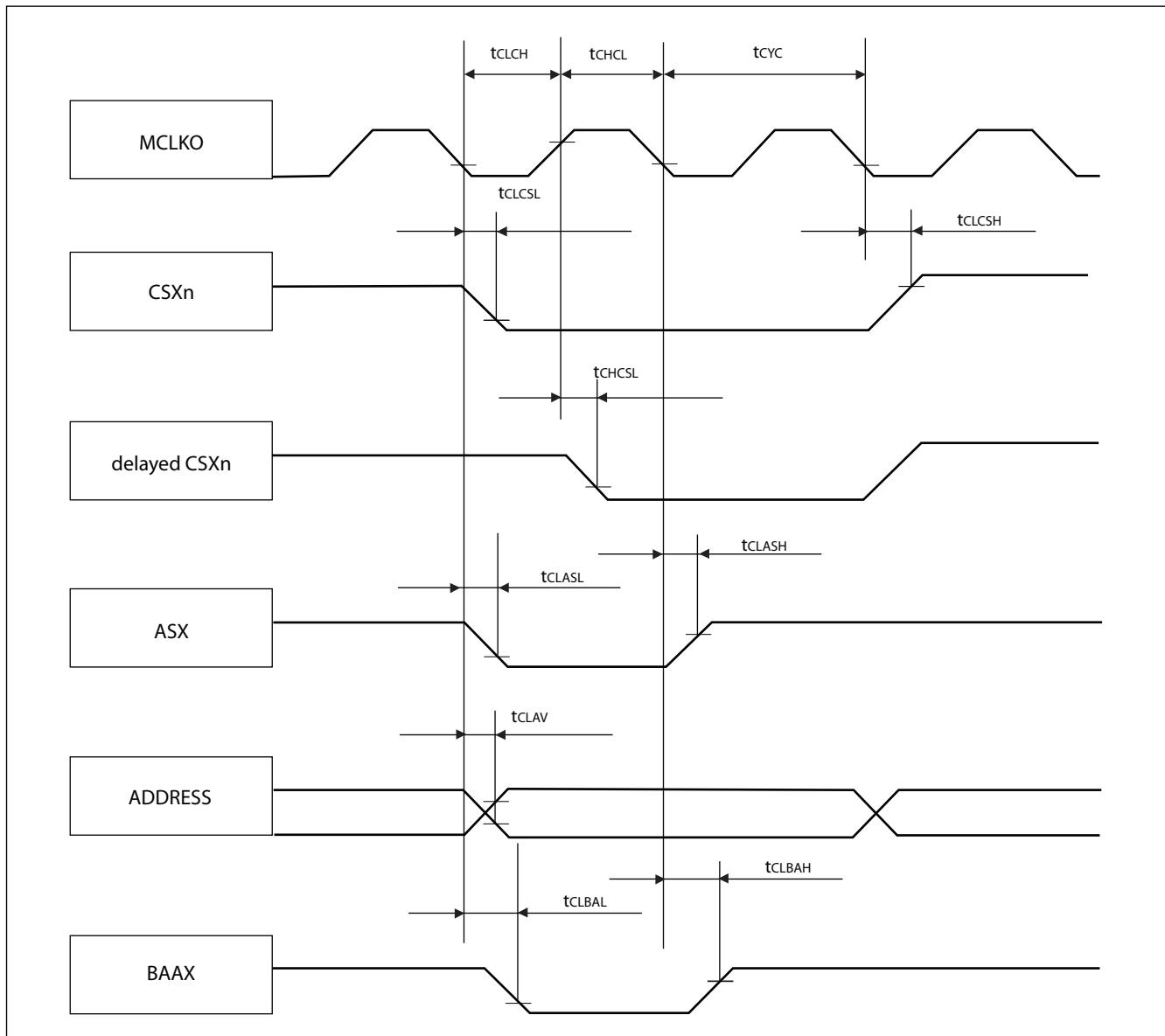
- $IO_{drive} = 5$  mA
- $V_{DD35} = 4.5$  V to  $5.5$  V,  $I_{load} = 5$  mA
- $V_{SS5} = 0$  V
- $T_a = -40$  °C to  $+105$  °C
- $C_l = 50$  pF
- $V_{OL} = 0.5 \times V_{DD35}$
- $V_{OH} = 0.5 \times V_{DD35}$
- $EPILR = 0$ ,  $PILR = 1$  (Automotive Level = worst case)

### 7.7.1. Basic Timing

( $V_{DD35} = 4.5$  V to  $5.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_a = -40$  °C to  $+105$  °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO	$t_{CLCH}$	MCLKO	$1/2 \times t_{CLKT} - 2$	$1/2 \times t_{CLKT} + 2$	ns
	$t_{CHCL}$		$1/2 \times t_{CLKT} - 2$	$1/2 \times t_{CLKT} + 2$	ns
MCLKO $\downarrow$ to CSXn delay time	$t_{CLCSL}$	MCLKO CSXn	—	7	ns
	$t_{CLCSH}$		—	7	ns
MCLKO $\uparrow$ to CSXn delay time (Addr $\rightarrow$ CS delay)	$t_{CHCSL}$		— 1	+ 6	ns
MCLKO $\downarrow$ to ASX delay time	$t_{CLASL}$	MCLKO ASX	—	7	ns
	$t_{CLASH}$		—	7	ns
MCLKO $\downarrow$ to BAAX delay time	$t_{CLBAL}$	MCLKO BAAX	—	7	ns
	$t_{CLBAH}$		2	—	ns
MCLKO $\downarrow$ to Address valid delay time	$t_{CLAV}$	MCLKO A25 to A0	—	8	ns

Note :  $t_{CLKT}$  is the cycle time of the external bus clock.

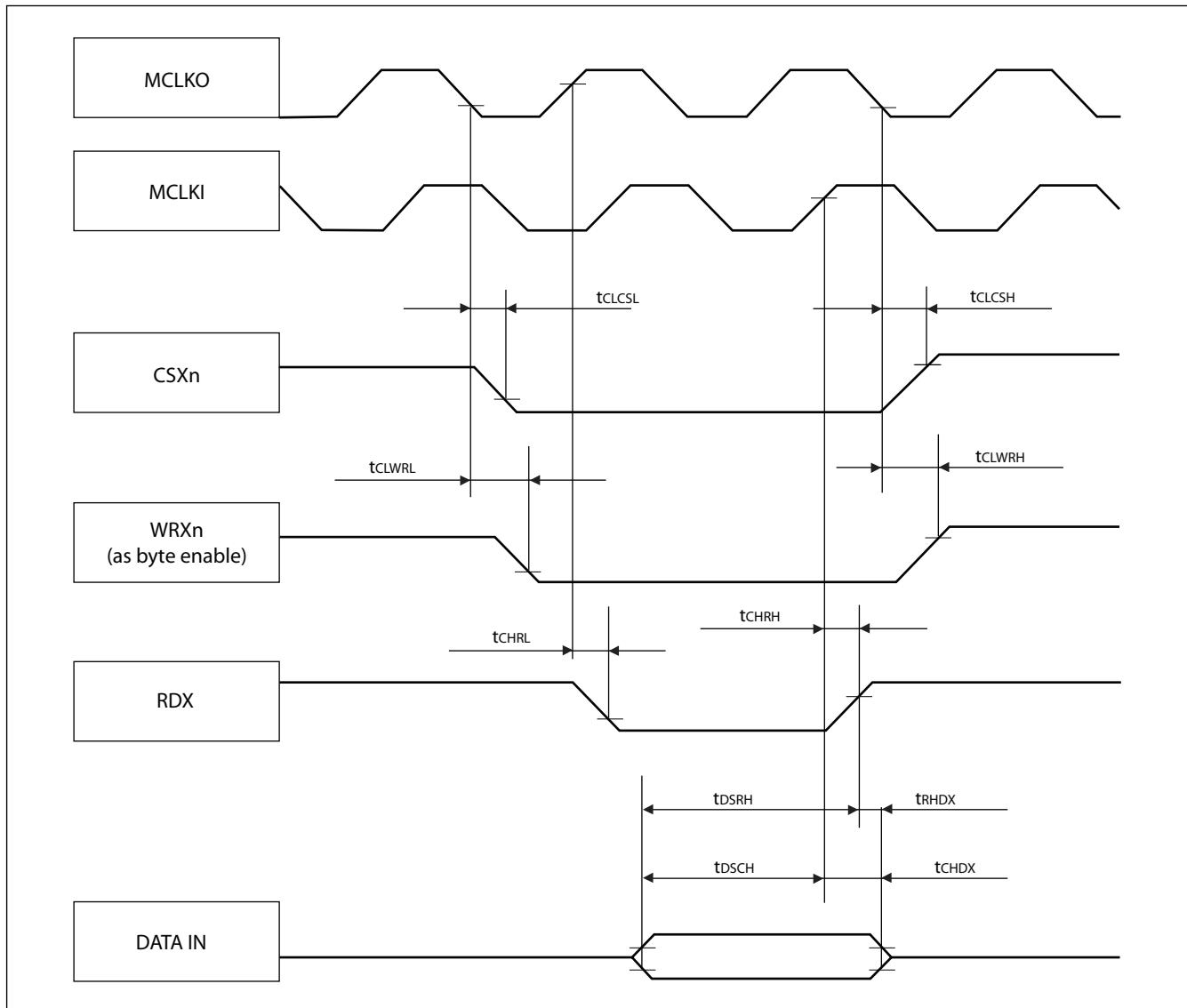


## 7.7.2. Synchronous/Asynchronous read access with external MCLKI input

( $V_{DD35} = 4.5$  V to 5.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑ /MCLKI ↑ to RDX delay time	t <sub>CHRL</sub>	MCLKO RDX	- 1	6	ns
	t <sub>CHRH</sub>	MCLKI RDX	8	16	ns
Data valid to RDX ↑ setup time	t <sub>DSRH</sub>	RDX D31 to D0	19	—	ns
RDX ↑ to Data valid hold time (external MCLKI input)	t <sub>RHDX</sub>	RDX D31 to D0	0	—	ns
Data valid to MCLKI ↑ setup time	t <sub>DSCH</sub>	MCLKI D31 to D0	3	—	ns
MCLKI ↑ to Data valid hold time	t <sub>CHDX</sub>	MCLKI D31 to D0	1	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	t <sub>CLWRL</sub>	MCLKO WRXn	—	9	ns
	t <sub>CLWRH</sub>		- 1	—	ns
MCLKO ↓ to CSXn delay time	t <sub>CLCSL</sub>	MCLKO CSXn	—	7	ns
	t <sub>CLCSH</sub>		—	7	ns

Note: The usage of the external feedback from MCLKO to MCLKI is not recommended.

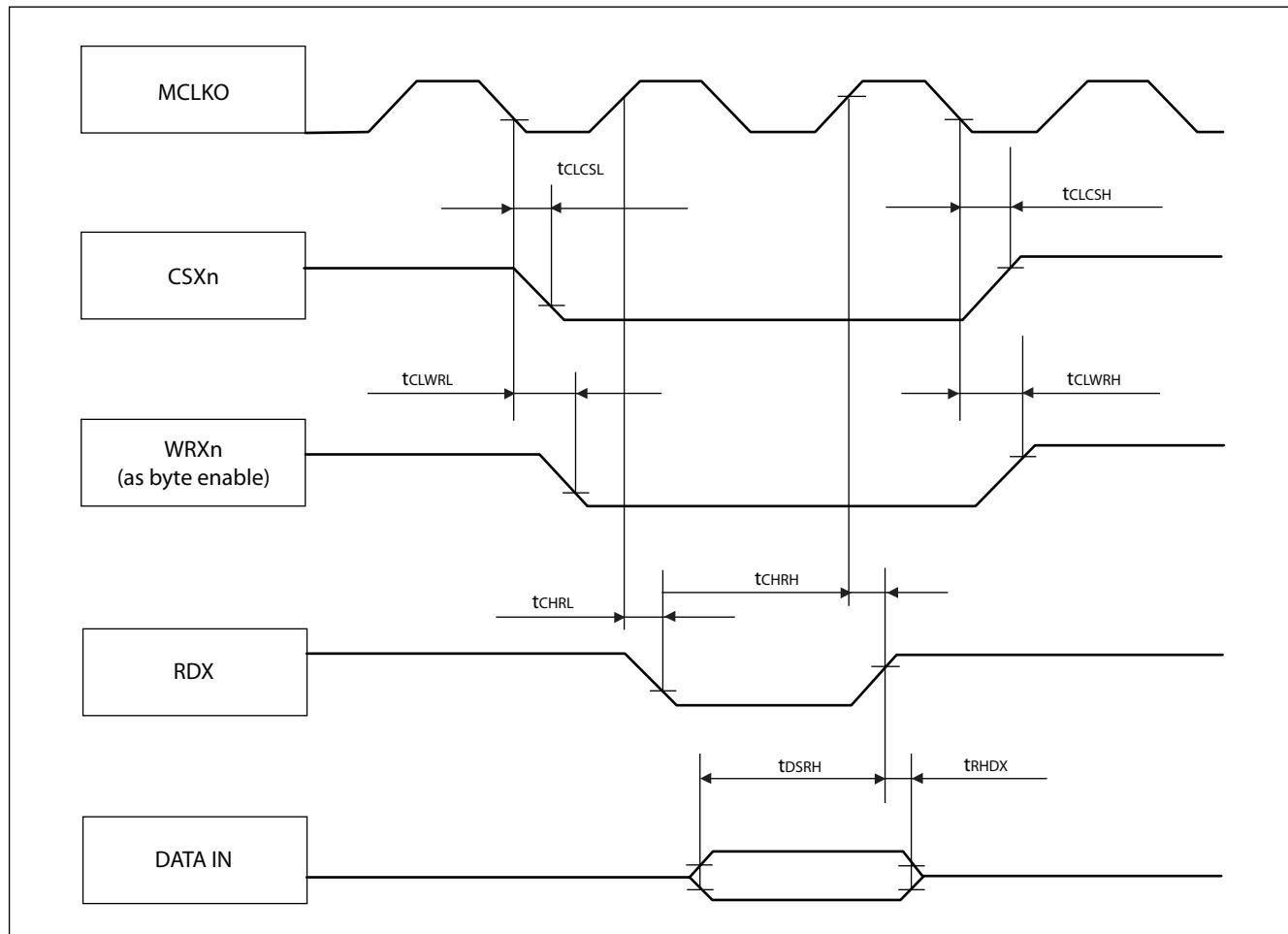


# MB91460E Series

## 7.7.3. Synchronous/Asynchronous read access with internal MCLKO --> MCLKI feedback

( $V_{DD35} = 4.5$  V to 5.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

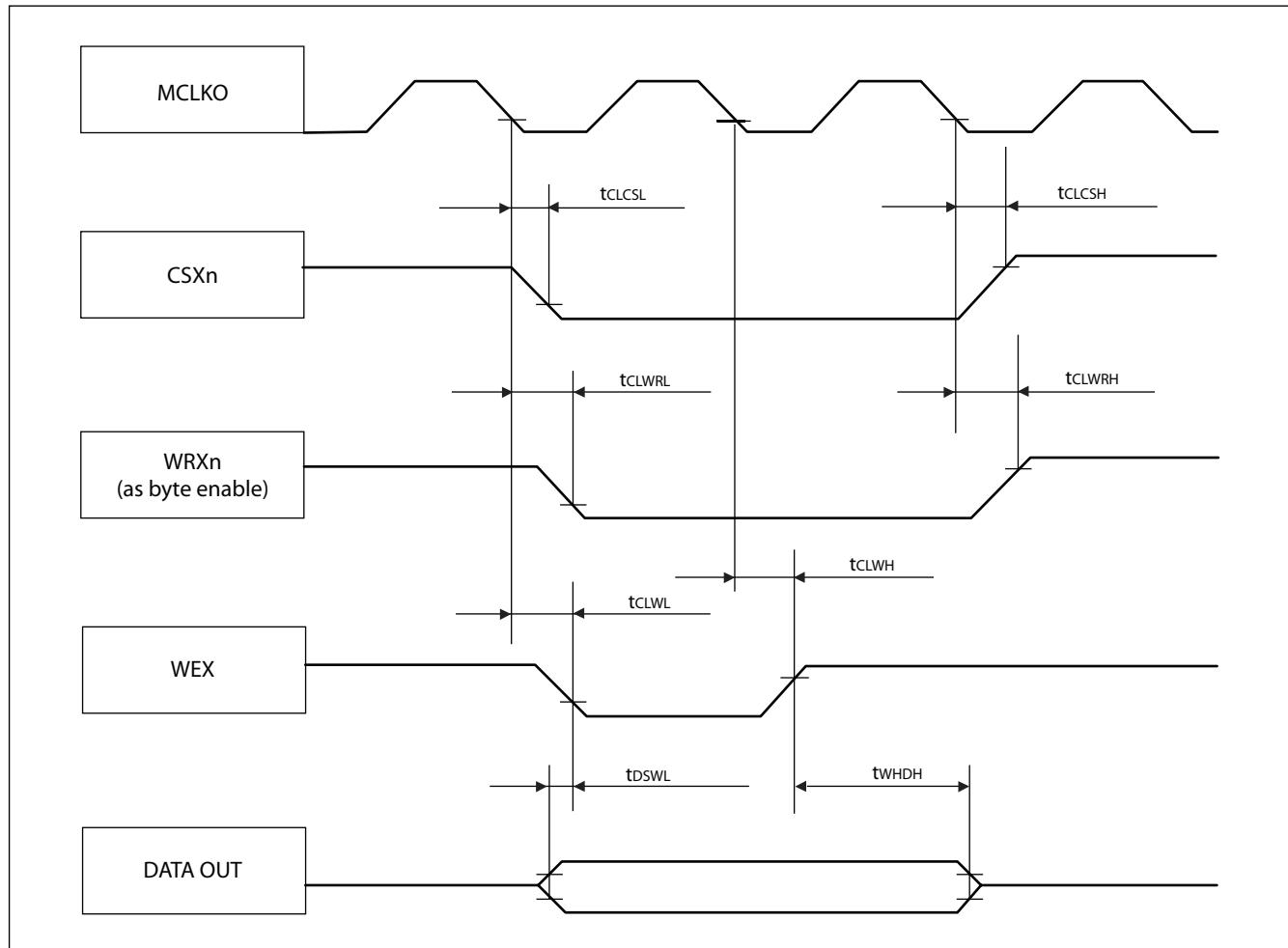
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO $\uparrow$ to RDX delay time	$t_{CHRL}$	MCLKO RDX	- 1	6	ns
	$t_{CHRH}$		- 1	7	ns
Data valid to RDX $\uparrow$ setup time	$t_{DSRH}$	RDX D31 to D0	16	—	ns
RDX $\uparrow$ to Data valid hold time (internal MCLKO $\rightarrow$ MCLKI / /MCLKI feedback)	$t_{RHDX}$	RDX D31 to D0	0	—	ns
MCLKO $\downarrow$ to WRXn (as byte enable) delay time	$t_{CLWRL}$	MCLKO WRXn	—	9	ns
	$t_{CLWRH}$		- 1	—	ns
MCLKO $\downarrow$ to CSXn delay time	$t_{CLCSL}$	MCLKO CSXn	—	7	ns
	$t_{CLCSH}$		—	7	ns



## 7.7.4. Synchronous write access - byte control type

( $V_{DD35} = 4.5$  V to 5.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

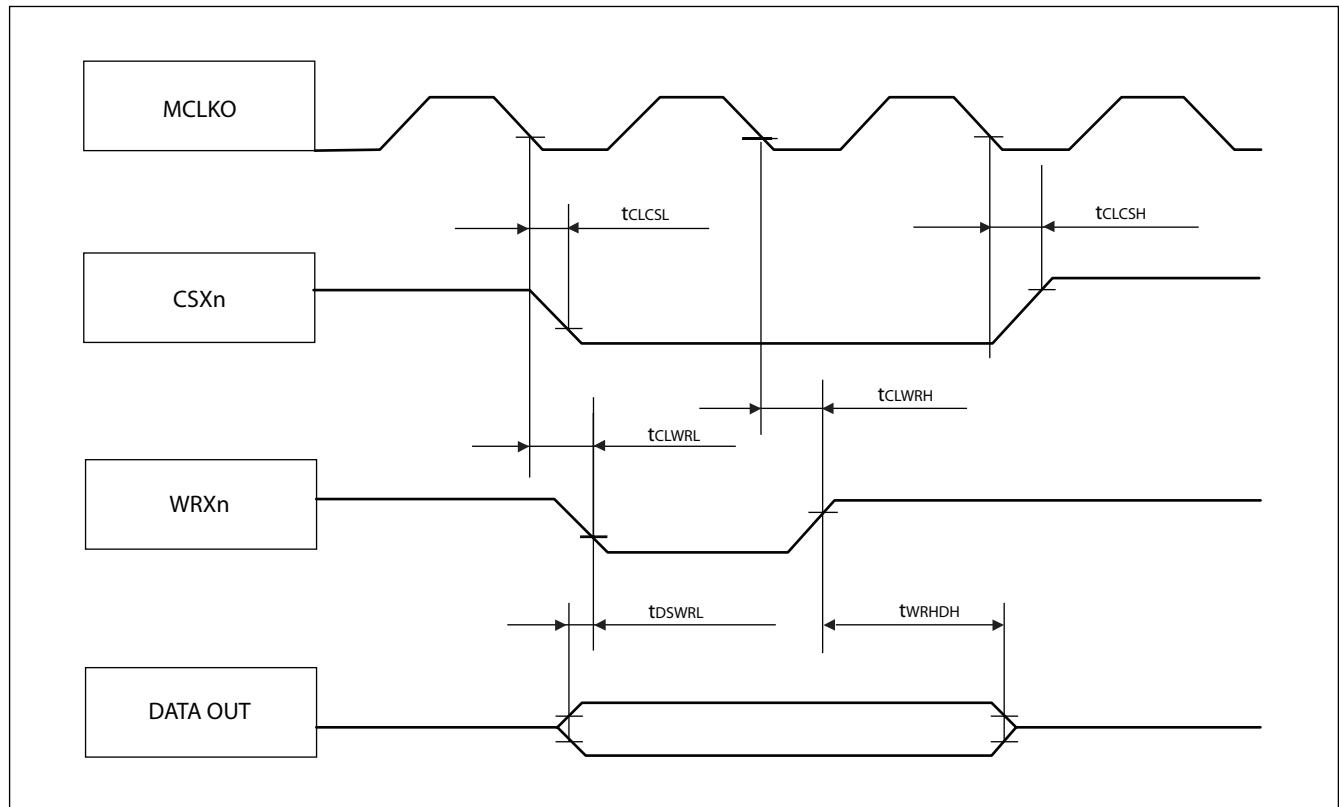
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WEX delay time	$t_{CLWL}$	MCLKO WEX	—	7	ns
	$t_{CLWH}$		2	—	ns
Data valid to WEX ↓ setup time	$t_{DSWL}$	WEX D31 to D0	- 4	—	ns
WEX ↑ to Data valid hold time	$t_{WHDH}$	WEX D31 to D0	$t_{CLKT} - 5$	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	$t_{CLWRL}$	MCLKO WRXn	—	9	ns
	$t_{CLWRH}$		- 1	—	ns
MCLKO ↓ to CSXn delay time	$t_{CLCSL}$	MCLKO CSXn	—	7	ns
	$t_{CLCSH}$		—	7	ns



## 7.7.5. Synchronous write access - no byte control type

( $V_{DD35} = 4.5$  V to 5.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

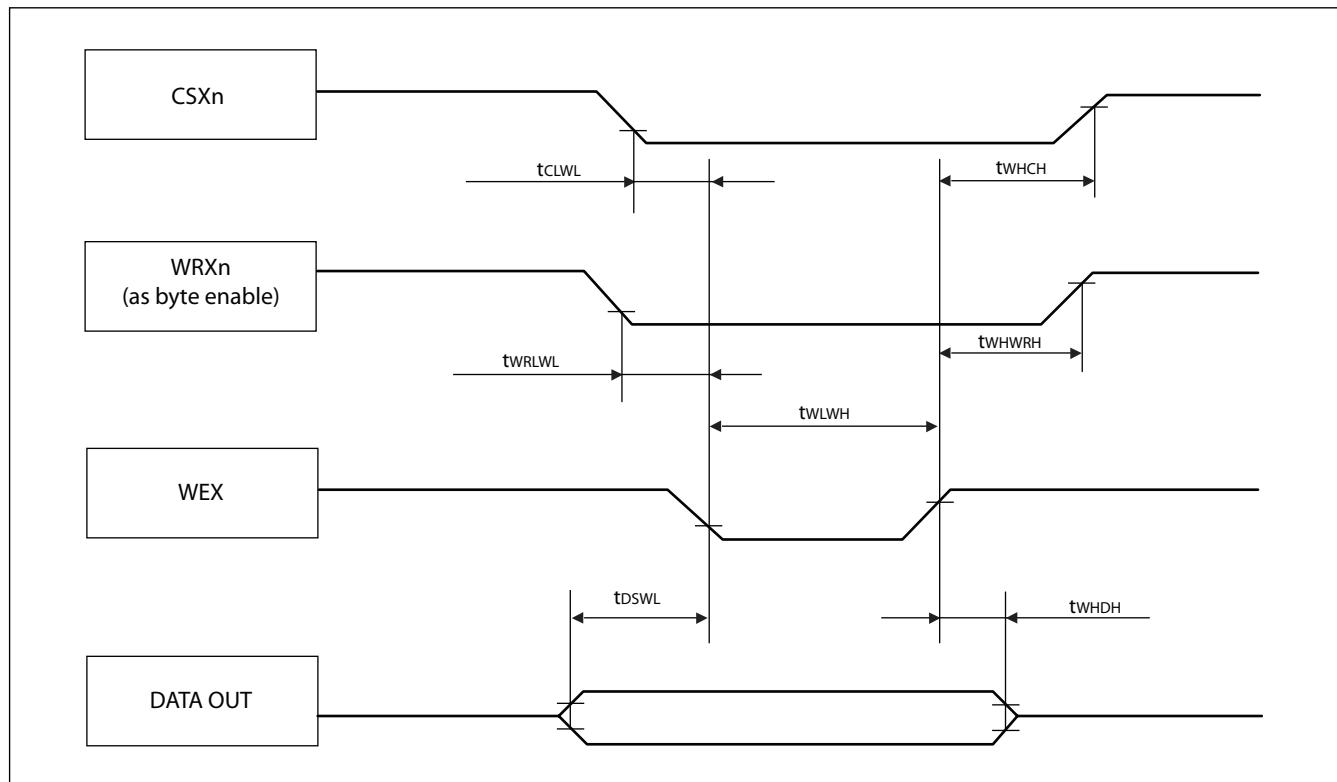
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WRXn delay time	$t_{CLWRL}$	MCLKO WRXn	—	9	ns
	$t_{CLWRH}$		— 1	—	ns
Data valid to WRXn ↓ setup time	$t_{DSWRL}$	WRXn D31 to D0	— 6	—	ns
WRXn ↑ to Data valid hold time	$t_{WRHDH}$	WRXn D31 to D0	$t_{CLKT} - 6$	—	ns
MCLKO ↓ to CSXn delay time	$t_{CLCSL}$	MCLKO CSXn	—	7	ns
	$t_{CLCSH}$		—	7	ns



## 7.7.6. Asynchronous write access - byte control type

( $V_{DD35} = 4.5$  V to 5.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	$t_{WLWH}$	WEX	$t_{CLKT} - 2$	—	ns
Data valid to WEX ↓ setup time	$t_{DSWL}$	WEX D31 to D0	$1/2 \times t_{CLKT} - 16$	—	ns
WEX ↑ to Data valid hold time	$t_{WHDH}$	WEX D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WEX to WRXn delay time	$t_{WLWL}$	WEX WRXn	—	$1/2 \times t_{CLKT} + 2$	ns
	$t_{WHWRH}$		$1/2 \times t_{CLKT} - 1$	—	ns
WEX to CSXn delay time	$t_{CLWL}$	WEX CSXn	—	$1/2 \times t_{CLKT} + 1$	ns
	$t_{WHCH}$		$1/2 \times t_{CLKT} - 1$	—	ns

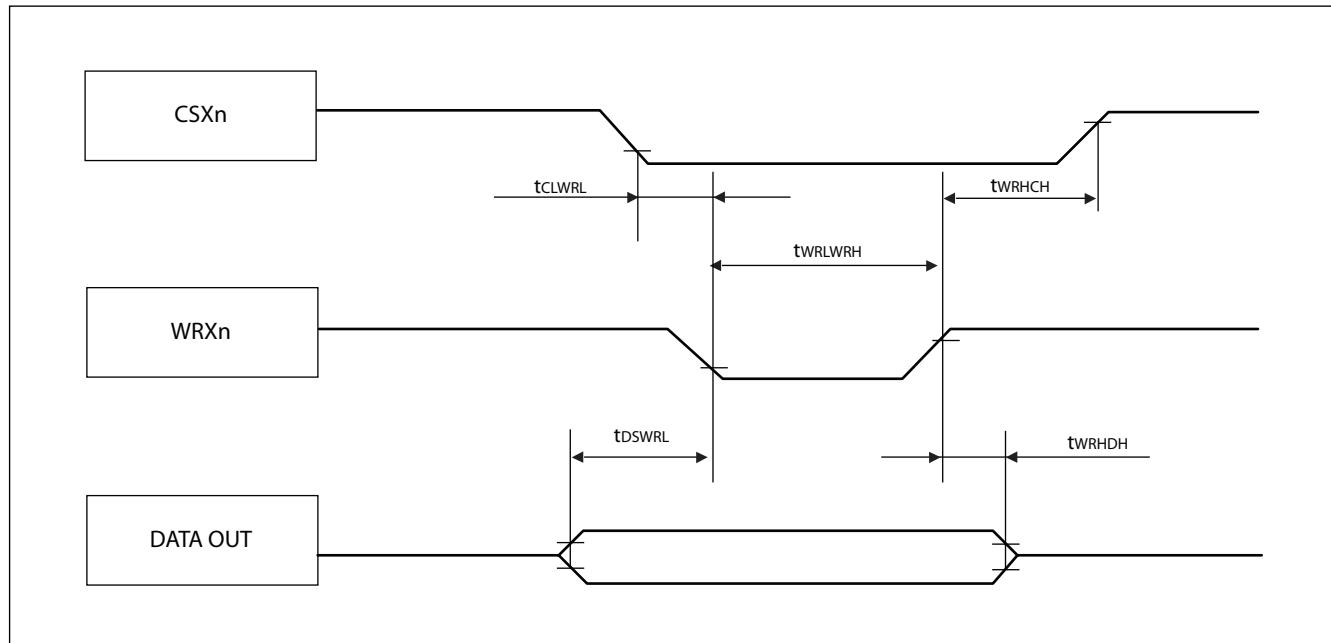


# MB91460E Series

## 7.7.7. Asynchronous write access - no byte control type

( $V_{DD35} = 4.5$  V to 5.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

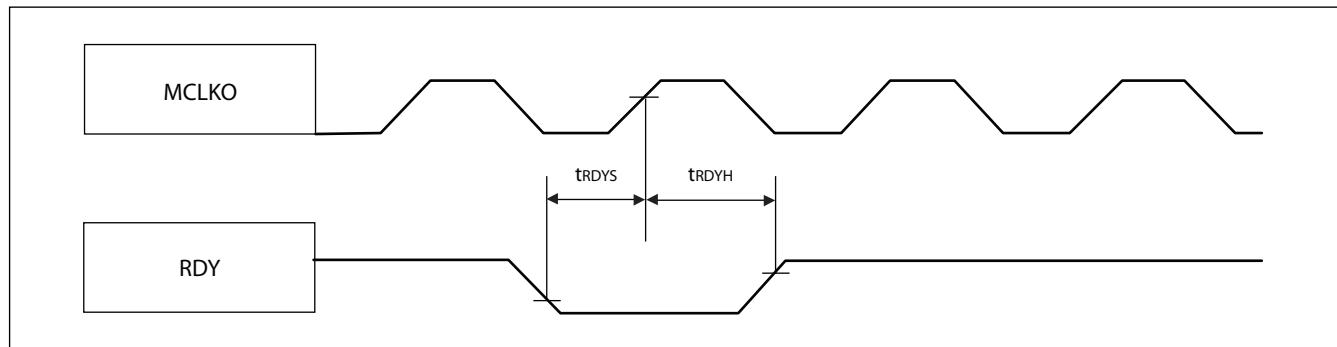
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	$t_{WLWRH}$	WRXn	$t_{CLKT} - 1$	—	ns
Data valid to WRXn ↓ setup time	$t_{DSWRL}$	WRXn D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WRXn ↑ to Data valid hold time	$t_{WRDH}$	WRXn D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WRXn to CSXn delay time	$t_{CLWRL}$ $t_{WRHCH}$	WRXn CSXn	— $1/2 \times t_{CLKT} - 2$	$1/2 \times t_{CLKT} - 1$ —	ns



## 7.7.8. RDY waitcycle insertion

( $V_{DD35} = 4.5$  V to  $5.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to +105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	$t_{RDYS}$	MCLKO RDY	12	—	ns
RDY hold time	$t_{RDYH}$	MCLKO RDY	0	—	ns



# MB91460E Series

## 7.7.9. Bus hold timing

( $V_{DD35} = 4.5 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO $\downarrow$ to BGRNTX delay time	$t_{CLBGL}$	MCLKO BGRNTX	—	5	ns
	$t_{CLBGH}$		—	6	ns
Bus HIZ to BGRNTX $\downarrow$	$t_{AXBGL}$	BGRNTX MCLK* A0 to An RDX, ASX WRXn, WEX CSXn, BAAX	$t_{CLKT} + 5$	—	ns
BGRNTX $\uparrow$ to Bus drive	$t_{BGHAV}$		$t_{CLKT} + 6$	—	ns

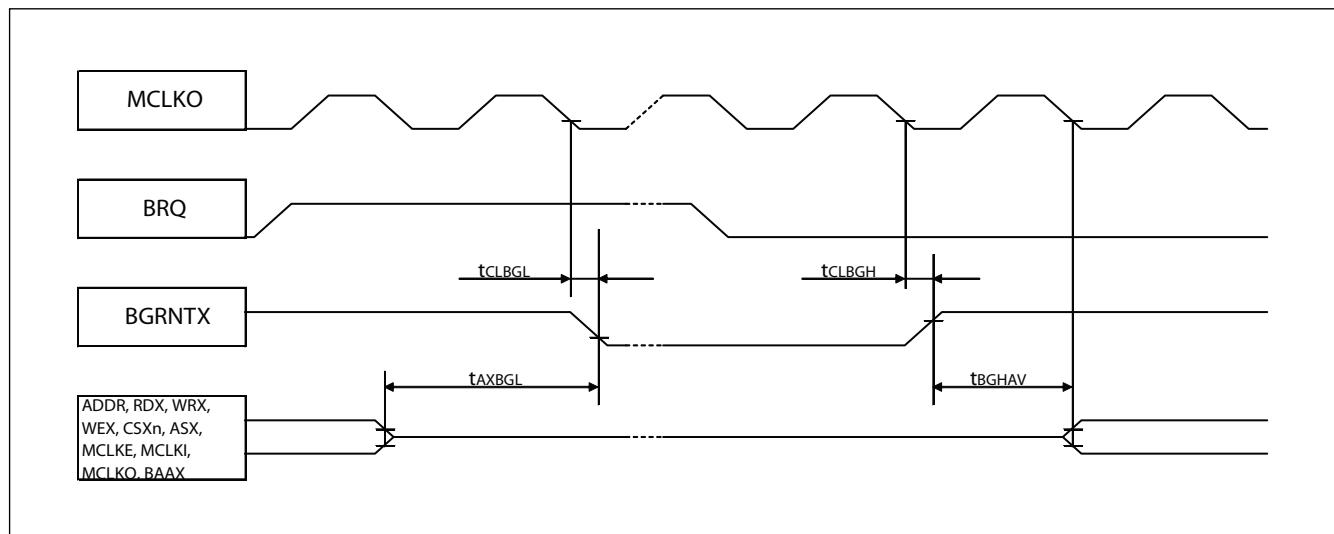
Note : BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX).

It must be kept High as long as the bus shall be hold.

After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.

Note : Condition for  $t_{AXBGL}$  and  $t_{BGHAV}$  :

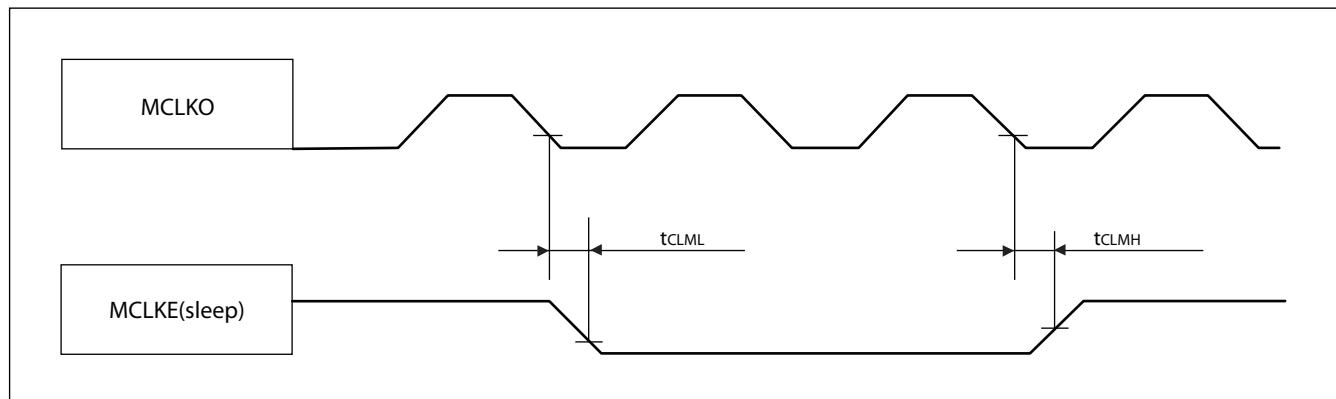
- $V_{OL} = 0.2 \times V_{DD35}$
- $V_{OH} = 0.8 \times V_{DD35}$



## 7.7.10. Clock relationships

( $V_{DD35} = 4.5$  V to  $5.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to  $+105$  °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to MCLKE (in sleep mode)	$t_{CLML}$	MCLKO	—	7	ns
	$t_{CLMH}$	MCLKE	— 1	—	ns



# MB91460E Series

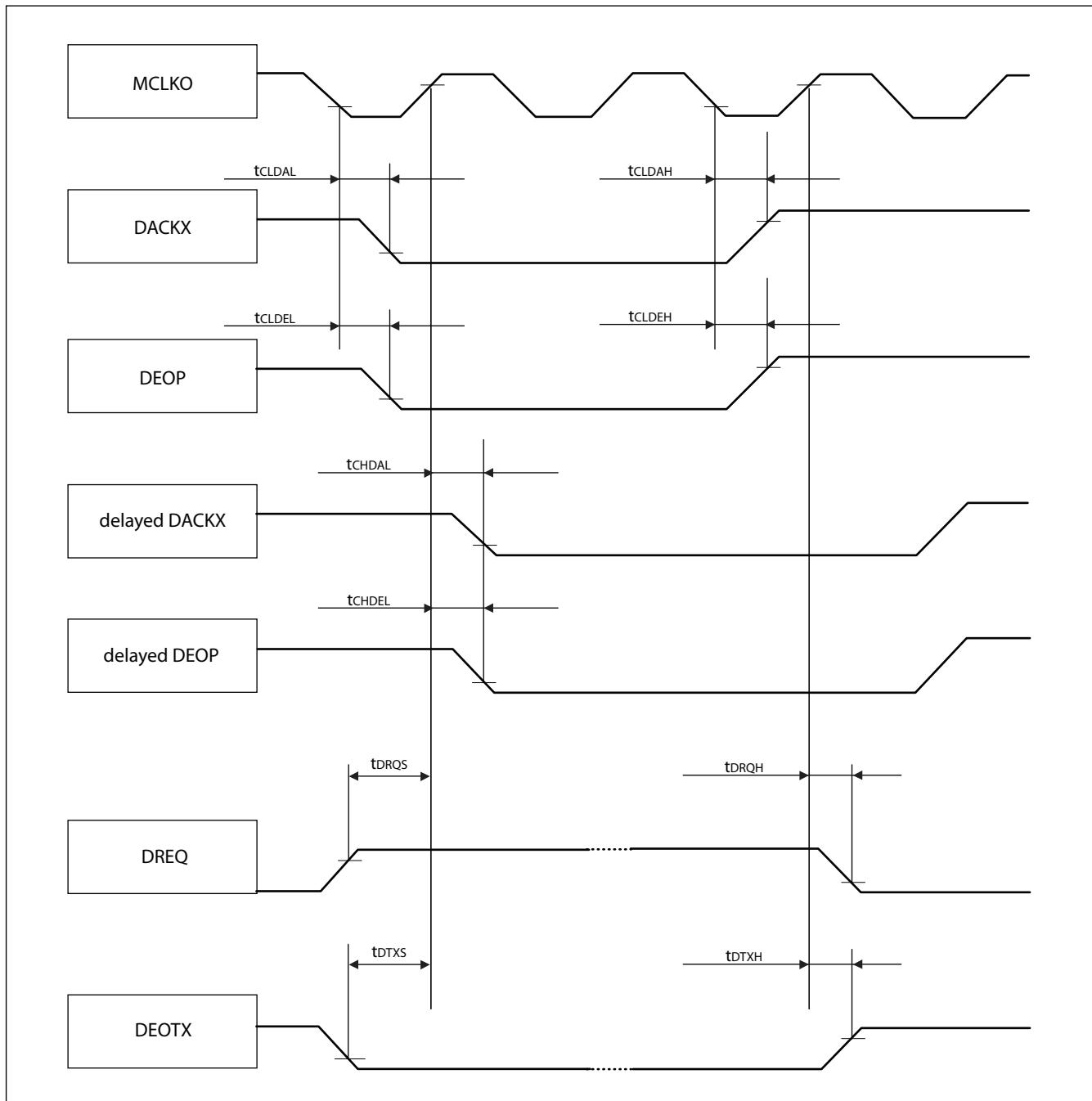
## 7.7.11. DMA transfer

( $V_{DD35} = 4.5$  V to  $5.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to +  $105$  °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to DACKX delay time	$t_{CLDAL}$	MCLKO DACKXn	—	7	ns
	$t_{CLDAH}$		—	7	ns
MCLKO ↓ to DEOP delay time	$t_{CLDEL}$	MCLKO DEOPn	—	9	ns
	$t_{CLDEH}$		—	9	ns
MCLKO ↑ to DACKX delay time (ADDR → delayed CS)	$t_{CHDAL}$	MCLKO DACKXn	1	6	ns
MCLKO ↑ to DEOP delay time (ADDR → delayed CS)	$t_{CHDEL}$	MCLKO DEOPn	1	8	ns
DREQ setup time	$t_{DRQS}$	MCLKO DREQn	12	—	ns
DREQ hold time	$t_{DRQH}$	MCLKO DREQn	0	—	ns
DEOTXn setup time	$t_{DTXS}$	MCLKO DEOTXn	12	—	ns
DEOTXn hold time	$t_{DTXH}$	MCLKO DEOTXn	0	—	ns

Note : DREQ and DEOTX must be applied for at least  $5 \times t_{CLKT}$  to ensure that they are really sampled and evaluated.

Under best case conditions (DMA not busy) only setup and hold times are required.



## 7.8. External Bus AC Timings at $V_{DD35} = 3.0$ to $4.5$ V

- Conditions during AC measurements

All AC tests were measured under the following conditions:

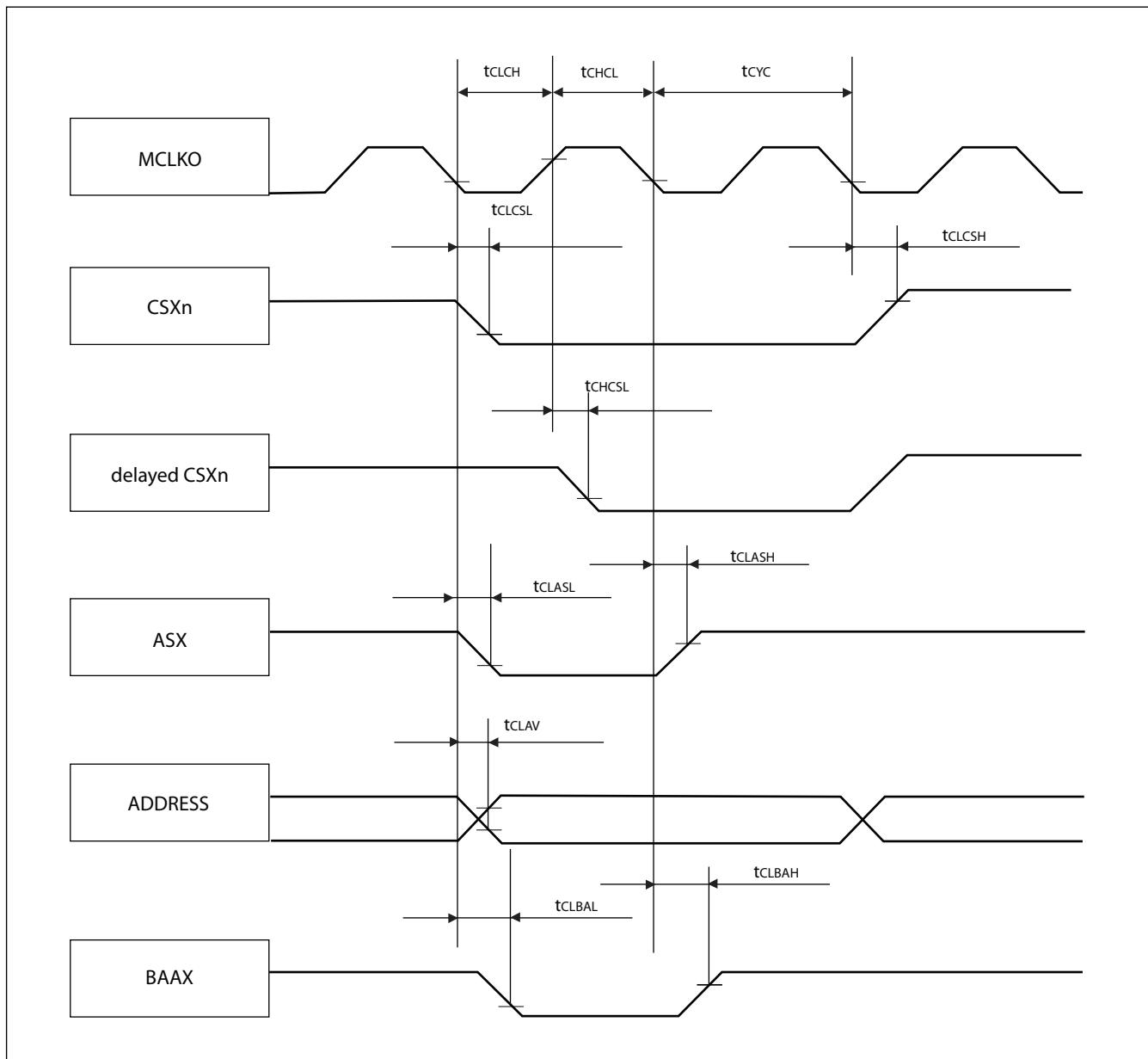
- $IO_{drive} = 5$  mA
- $V_{DD35} = 3.0$  V to  $4.5$  V,  $I_{load} = 3$  mA
- $V_{SS5} = 0$  V
- $T_A = -40$  °C to  $+105$  °C
- $C_I = 50$  pF
- $V_{OL} = 0.5 \times V_{DD35}$
- $V_{OH} = 0.5 \times V_{DD35}$
- $EPILR = 0$ ,  $PILR = 1$  (Automotive Level = worst case)

### 7.8.1. Basic Timing

( $V_{DD35} = 3.0$  V to  $4.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to  $+105$  °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO	$t_{CLCH}$	MCLKO	$1/2 \times t_{CLKT} - 2$	$1/2 \times t_{CLKT} + 4$	ns
	$t_{CHCL}$		$1/2 \times t_{CLKT} - 4$	$1/2 \times t_{CLKT} + 2$	ns
MCLKO $\downarrow$ to CSXn delay time	$t_{CLCSL}$	MCLKO CSXn	—	6	ns
	$t_{CLCSH}$		—	8	ns
MCLKO $\uparrow$ to CSXn delay time (Addr $\rightarrow$ CS delay)	$t_{CHCSL}$		— 1	+ 5	ns
MCLKO $\downarrow$ to ASX delay time	$t_{CLASL}$	MCLKO ASX	—	7	ns
	$t_{CLASH}$		—	9	ns
MCLKO $\downarrow$ to BAAX delay time	$t_{CLBAL}$	MCLKO BAAX	—	7	ns
	$t_{CLBAH}$		2	—	ns
MCLKO $\downarrow$ to Address valid delay time	$t_{CLAV}$	MCLKO A25 to A0	—	13	ns

Note :  $t_{CLKT}$  is the cycle time of the external bus clock.

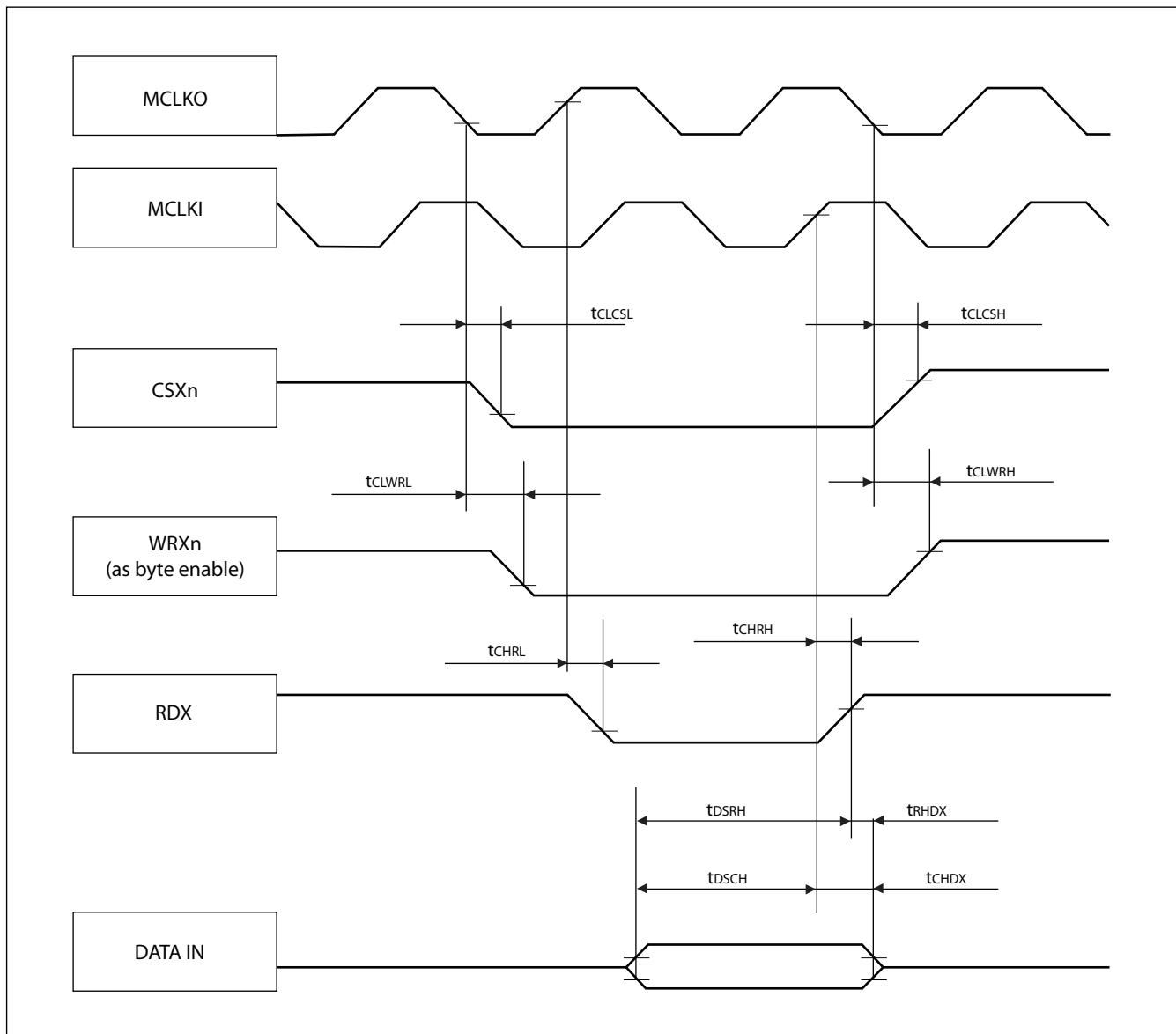


## 7.8.2. Synchronous/Asynchronous read access with external MCLKI input

( $V_{DD35} = 3.0$  V to 4.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑/MCLKI ↑ to RDX delay time	t <sub>CHRL</sub>	MCLKO RDX	– 1	5	ns
	t <sub>CHRH</sub>	MCLKI RDX	8	16	ns
Data valid to RDX ↑ setup time	t <sub>DSRH</sub>	RDX D31 to D0	19	—	ns
RDX ↑ to Data valid hold time (external MCLKI input)	t <sub>RHDX</sub>	RDX D31 to D0	0	—	ns
Data valid to MCLKI ↑ setup time	t <sub>DSCH</sub>	MCLKI D31 to D0	3	—	ns
MCLKI ↑ to Data valid hold time	t <sub>CHDX</sub>	MCLKI D31 to D0	1	—	ns
MCLKO ↓ to WRX <sub>n</sub> (as byte enable) delay time	t <sub>CLWRL</sub>	MCLKO WRX <sub>n</sub>	—	12	ns
	t <sub>CLWRH</sub>		0	—	ns
MCLKO ↓ to CSX <sub>n</sub> delay time	t <sub>CLCSL</sub>	MCLKO CSX <sub>n</sub>	—	6	ns
	t <sub>CLCSH</sub>		—	9	ns

Note: The usage of the external feedback from MCLKO to MCLKI is not recommended.

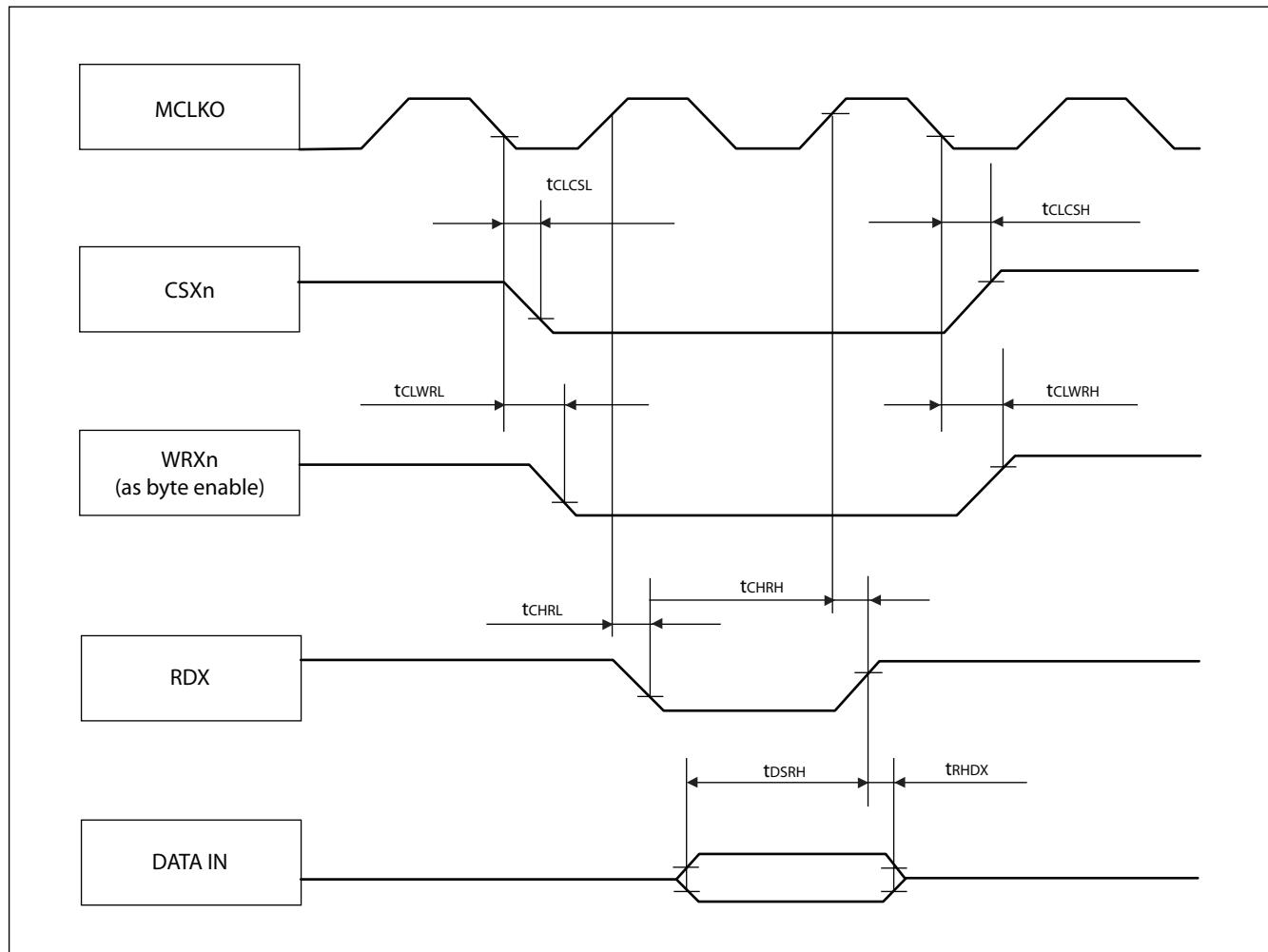


# MB91460E Series

## 7.8.3. Synchronous/Asynchronous read access with internal MCLKO --> MCLKI feedback

( $V_{DD35} = 3.0$  V to 4.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

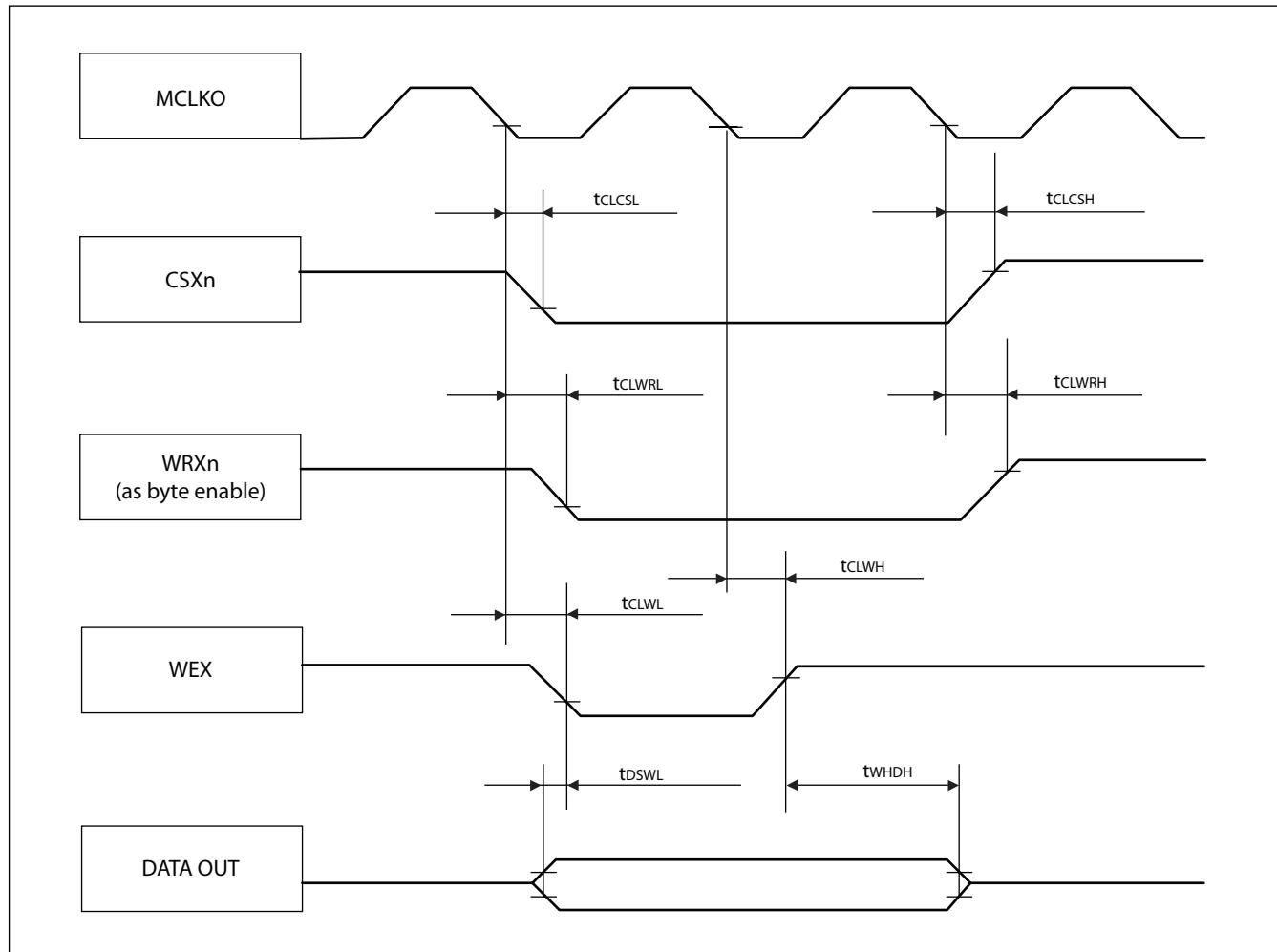
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO $\uparrow$ to RDX delay time	$t_{CHRL}$	MCLKO RDX	- 1	5	ns
	$t_{CHRH}$		- 1	7	ns
Data valid to RDX $\uparrow$ setup time	$t_{DSRH}$	RDX D31 to D0	18	—	ns
RDX $\uparrow$ to Data valid hold time (internal MCLKO $\rightarrow$ MCLKI / /MCLKI feedback)	$t_{RHDX}$	RDX D31 to D0	0	—	ns
MCLKO $\downarrow$ to WRXn (as byte enable) delay time	$t_{CLWRL}$	MCLKO WRXn	—	12	ns
	$t_{CLWRH}$		0	—	ns
MCLKO $\downarrow$ to CSXn delay time	$t_{CLCSL}$	MCLKO CSXn	—	6	ns
	$t_{CLCSH}$		—	8	ns



## 7.8.4. Synchronous write access - byte control type

( $V_{DD35} = 3.0$  V to  $4.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to  $+105$  °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WEX delay time	tCLWL	MCLKO WEX	—	7	ns
	tCLWH		1	—	ns
Data valid to WEX ↓ setup time	tDSWL	WEX D31 to D0	-11	—	ns
WEX ↑ to Data valid hold time	tWHDH	WEX D31 to D0	tCLKT - 5	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	tCLWRL	MCLKO WRXn	—	12	ns
	tCLWRH		0	—	ns
MCLKO ↓ to CSXn delay time	tCLCSL	MCLKO CSXn	—	6	ns
	tCLCSH		—	8	ns

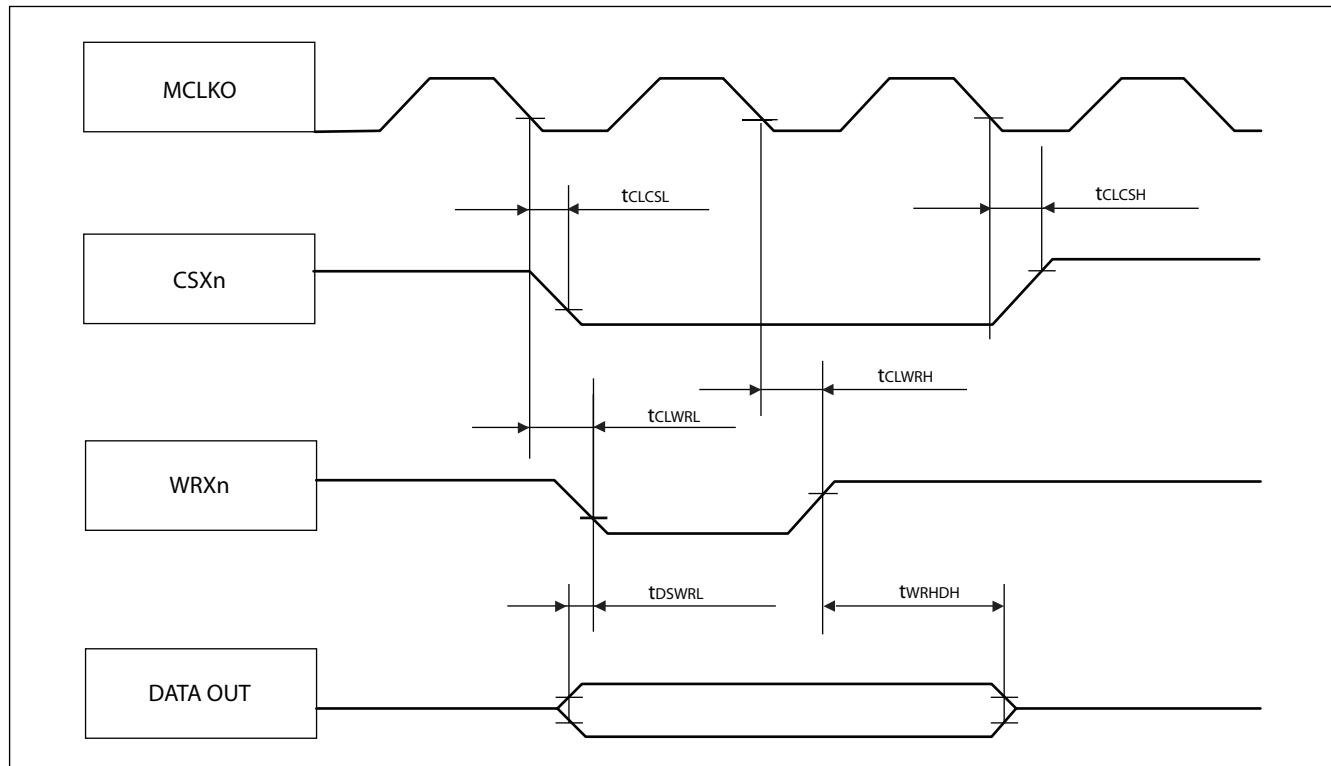


# MB91460E Series

## 7.8.5. Synchronous write access - no byte control type

( $V_{DD35} = 3.0$  V to 4.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

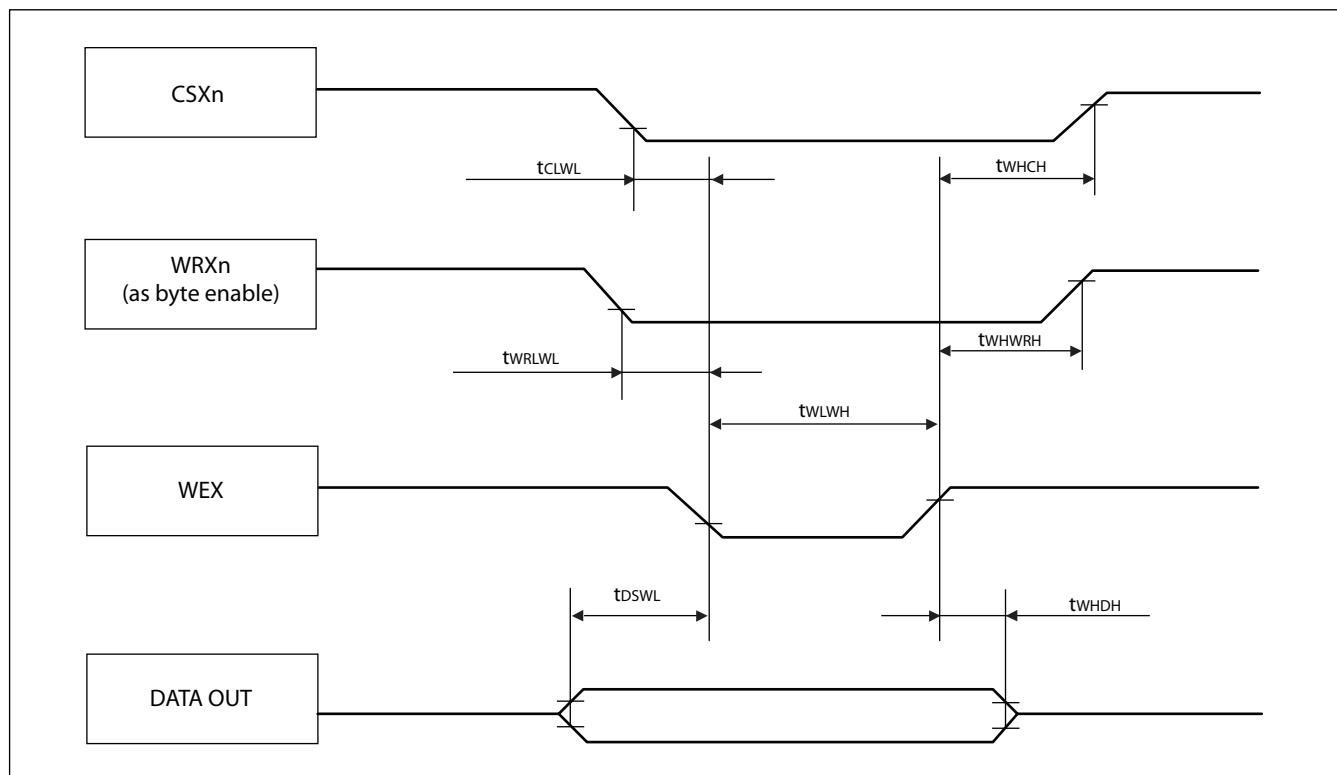
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WRXn delay time	$t_{CLWRL}$	MCLKO WRXn	—	12	ns
	$t_{CLWRH}$		0	—	ns
Data valid to WRXn ↓ setup time	$t_{DSWRL}$	WRXn D31 to D0	- 11	—	ns
WRXn ↑ to Data valid hold time	$t_{WRHDH}$	WRXn D31 to D0	$t_{CLKT} - 6$	—	ns
MCLKO ↓ to CSXn delay time	$t_{CLCSL}$	MCLKO CSXn	—	6	ns
	$t_{CLCSH}$		—	8	ns



## 7.8.6. Asynchronous write access - byte control type

( $V_{DD35} = 3.0 \text{ V to } 4.5 \text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	$t_{WLWH}$	WEX	$t_{CLKT} - 2$	—	ns
Data valid to WEX ↓ setup time	$t_{DSWL}$	WEX D31 to D0	$1/2 \times t_{CLKT} - 11$	—	ns
WEX ↑ to Data valid hold time	$t_{WHDH}$	WEX D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WEX to WRXn delay time	$t_{WRWL}$	WEX WRXn	—	$1/2 \times t_{CLKT} + 3$	ns
	$t_{WHWRH}$		$1/2 \times t_{CLKT} - 3$	—	ns
WEX to CSXn delay time	$t_{CLWL}$	WEX CSXn	—	$1/2 \times t_{CLKT} - 3$	ns
	$t_{WHCH}$		$1/2 \times t_{CLKT} - 3$	—	ns

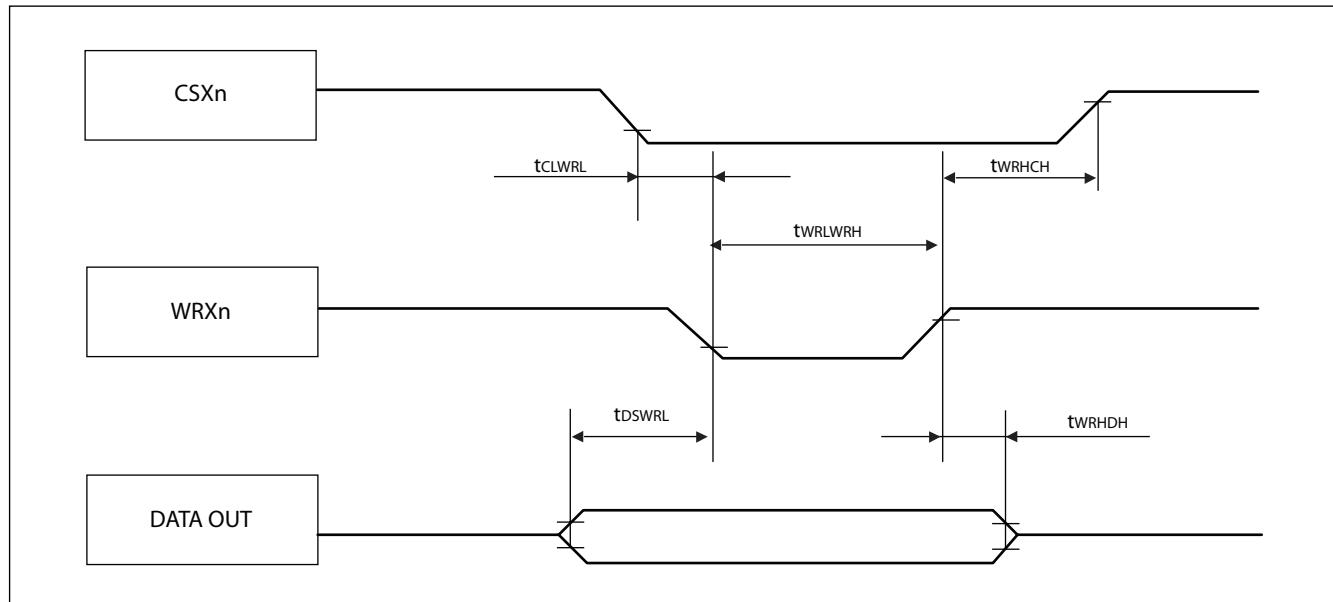


# MB91460E Series

## 7.8.7. Asynchronous write access - no byte control type

( $V_{DD35} = 3.0$  V to 4.5 V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to + 105 °C)

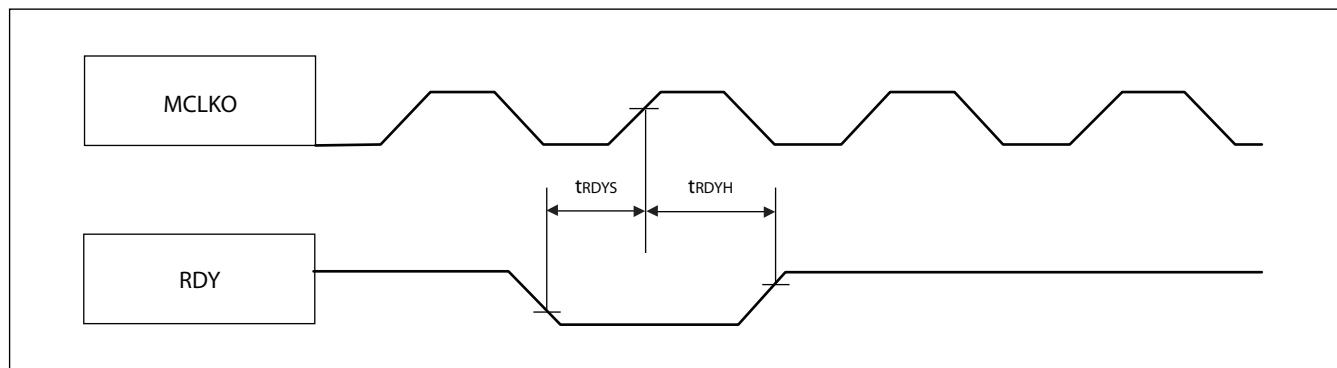
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	$t_{WRWLWRH}$	WRXn	$t_{CLKT} - 2$	—	ns
Data valid to WRXn ↓ setup time	$t_{DSWRL}$	WRXn D31 to D0	$1/2 \times t_{CLKT} - 11$	—	ns
WRXn ↑ to Data valid hold time	$t_{WRHDH}$	WRXn D31 to D0	$1/2 \times t_{CLKT} - 6$	—	ns
WRXn to CSXn delay time	$t_{CLWRL}$	WRXn CSXn	—	$1/2 \times t_{CLKT} - 2$	ns
	$t_{WRHCH}$		$1/2 \times t_{CLKT} - 3$	—	ns



## 7.8.8. RDY waitcycle insertion

(V<sub>DD35</sub> = 3.0 V to 4.5 V, V<sub>SS5</sub> = AV<sub>SS5</sub> = 0 V, T<sub>A</sub> = -40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	t <sub>RDYS</sub>	MCLKO RDY	14	—	ns
RDY hold time	t <sub>RDYH</sub>	MCLKO RDY	0	—	ns



# MB91460E Series

## 7.8.9. Bus hold timing

( $V_{DD35} = 3.0 \text{ V to } 4.5 \text{ V}$ ,  $V_{SS5} = AV_{SS5} = 0 \text{ V}$ ,  $T_A = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO $\downarrow$ to BGRNTX delay time	$t_{CLBGL}$	MCLKO BGRNTX	—	5	ns
	$t_{CLBGH}$		—	6	ns
Bus HIZ to BGRNTX $\downarrow$	$t_{AXBGL}$	BGRNTX MCLK*	$t_{CLKT} + 8$	—	ns
BGRNTX $\uparrow$ to Bus drive	$t_{BGHAV}$	A0 to An RDX, ASX WRXn, WEX CSXn, BAAX	$t_{CLKT} + 1$	—	ns

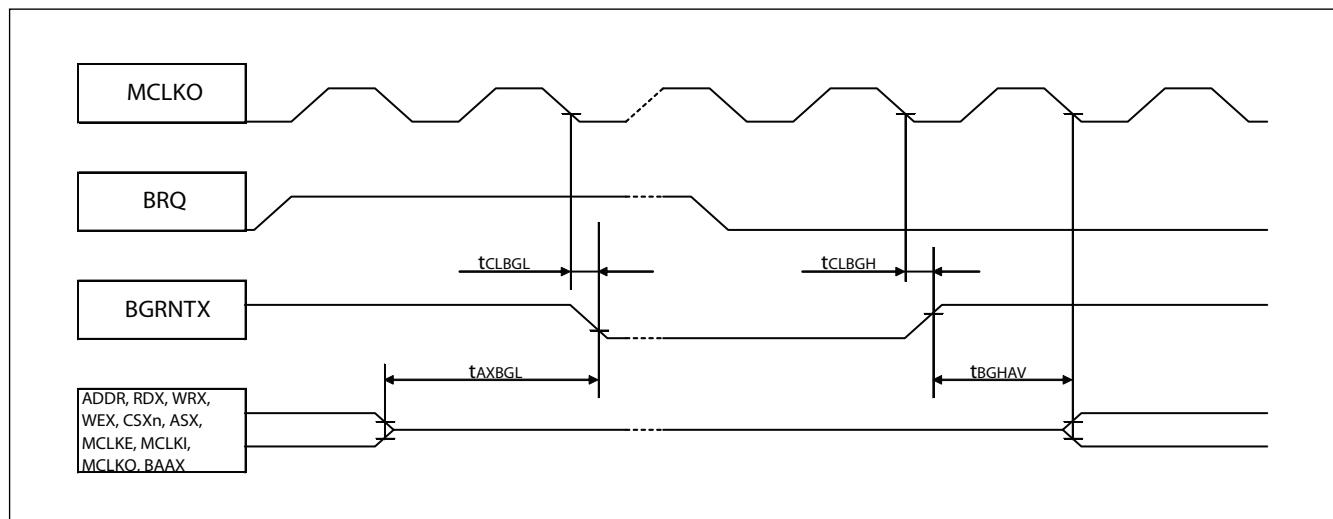
Note : BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX).

It must be kept High as long as the bus shall be hold.

After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.

Note : Condition for  $t_{AXBGL}$  and  $t_{BGHAV}$  :

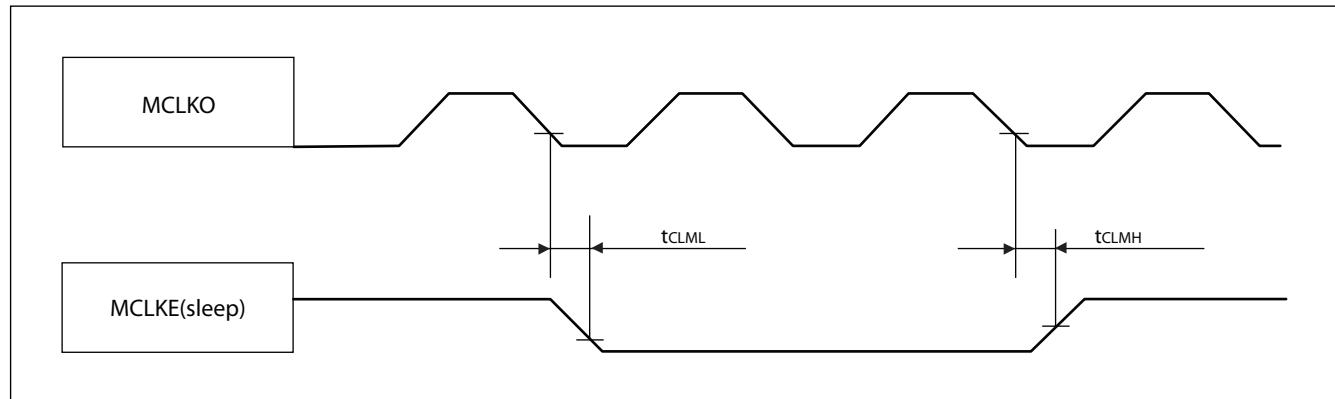
- $V_{OL} = 0.2 \times V_{DD35}$
- $V_{OH} = 0.8 \times V_{DD35}$



## 7.8.10. Clock relationships

( $V_{DD35} = 3.0$  V to  $4.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to  $+105$  °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to MCLKE (in sleep mode)	$t_{CLML}$	MCLKO MCLKE	—	3	ns
	$t_{CLMH}$		0	—	ns



# MB91460E Series

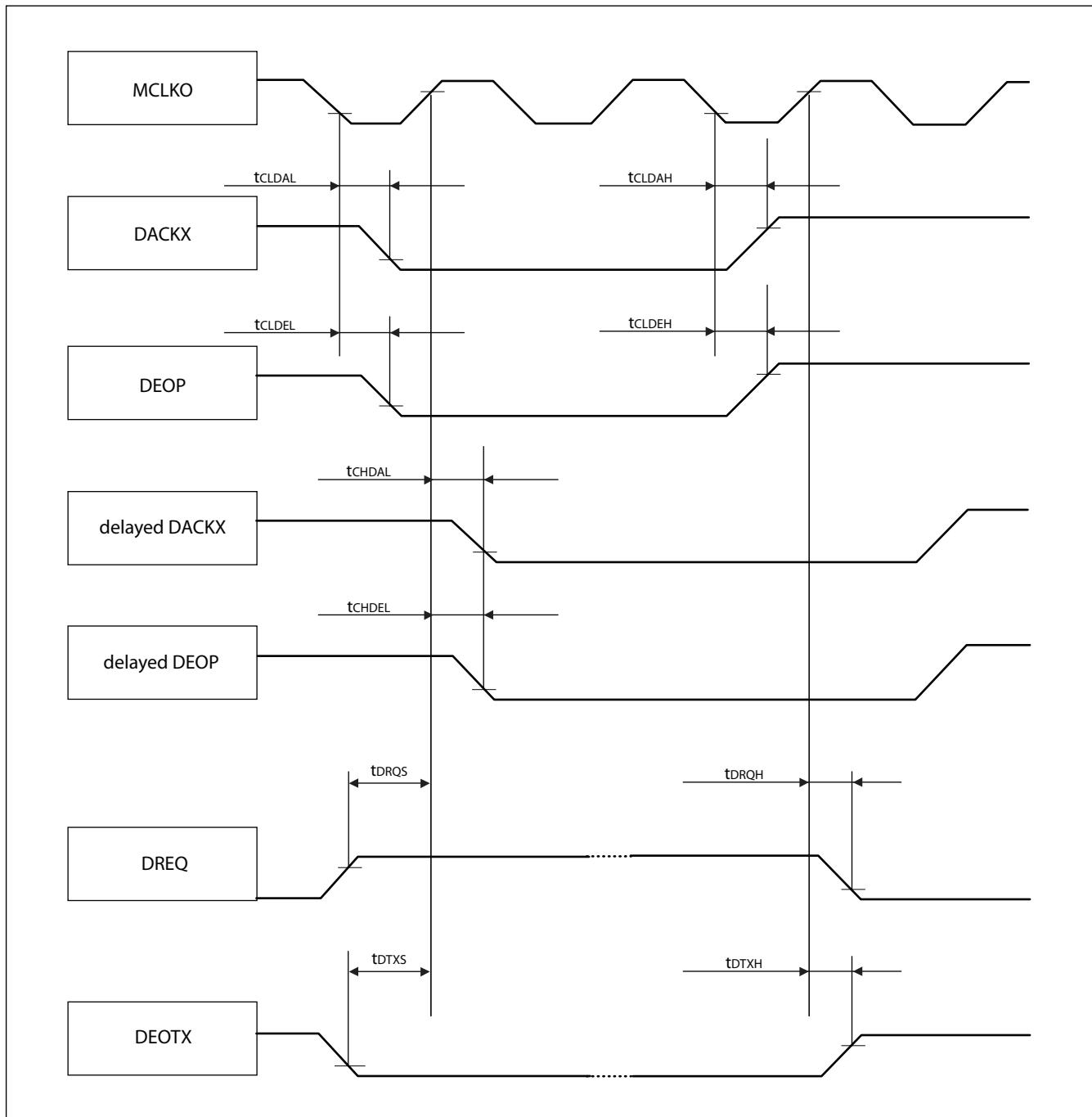
## 7.8.11. DMA transfer

( $V_{DD35} = 3.0$  V to  $4.5$  V,  $V_{SS5} = AV_{SS5} = 0$  V,  $T_A = -40$  °C to  $+105$  °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to DACKX delay time	$t_{CLDAL}$	MCLKO DACKXn	—	7	ns
	$t_{CLDAH}$		—	8	ns
MCLKO ↓ to DEOP delay time	$t_{CLDEL}$	MCLKO DEOPn	—	7	ns
	$t_{CLDEH}$		—	11	ns
MCLKO ↑ to DACKX delay time (ADDR → delayed CS)	$t_{CHDAL}$	MCLKO DACKXn	– 1	4	ns
MCLKO ↑ to DEOP delay time (ADDR → delayed CS)	$t_{CHDEL}$	MCLKO DEOPn	– 1	6	ns
DREQ setup time	$t_{DRQS}$	MCLKO DREQn	16	—	ns
DREQ hold time	$t_{DRQH}$	MCLKO DREQn	0	—	ns
DEOTXn setup time	$t_{DTXS}$	MCLKO DEOTXn	16	—	ns
DEOTXn hold time	$t_{DTXH}$	MCLKO DEOTXn	0	—	ns

Note : DREQ and DEOTX must be applied for at least  $5 \times t_{CLKT}$  to ensure that they are really sampled and evaluated.

Under best case conditions (DMA not busy) only setup and hold times are required.

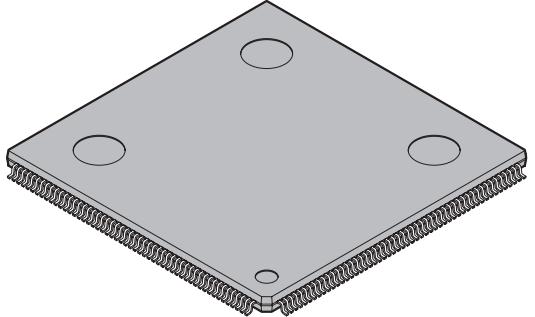


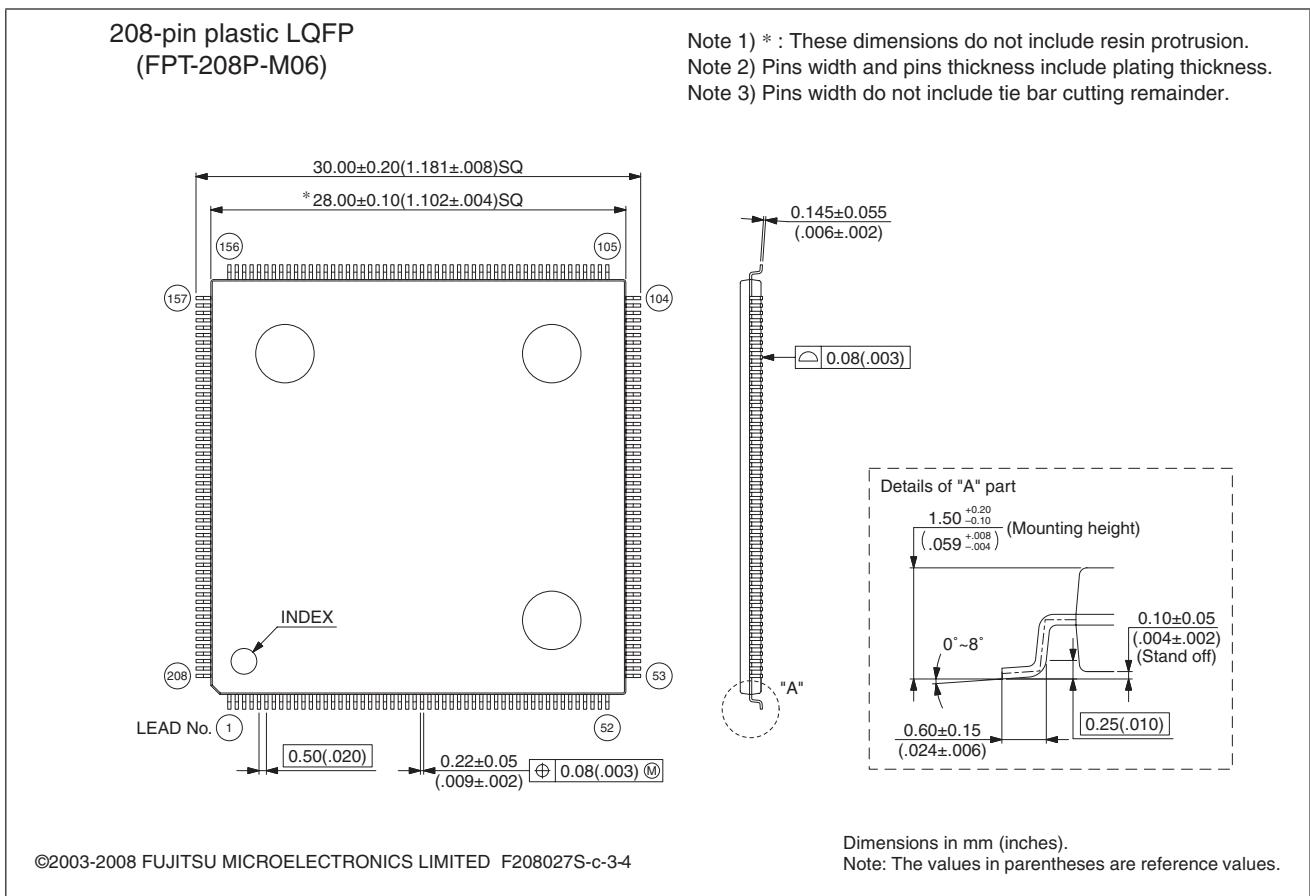
# MB91460E Series

## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB91F467EAPMC-GSE2	208-pin low profile QFP (FPT-208P-M06)	Lead-free package

## ■ PACKAGE DIMENSION

208-pin plastic LQFP    (FPT-208P-M06)	Lead pitch	0.50 mm
	Package width × package length	28.0 × 28.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	2.55g
	Code (Reference)	P-LFQFP208-28×28-0.50



Please confirm the latest Package dimension by following URL.  
<http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpkv.html>

# MB91460E Series

## ■ REVISION HISTORY

Version/ Date	Page	Section	Change Results
Ver. 0.01 2009-04-16	-	-	Initial version based on MB91F467D
Ver. 0.2 2009-07-03	all	all	Various updates following the proof read results on other MB91460 series datasheets
	76	Shutdown Mode	Chapter "Shutdown Mode" added
Ver. 0.3 2009-08-03	4	Product Lineup	Corrected that the software watchdog cannot be activated in SLEEP/STOP
	76-92	Chapter Shutdown Mode	Total update
	120	IO Map; SHDINT register	Removed bits [3:2]
	151	ELECTRICAL CHARACTERISTICS, Absolute maximum ratings	Permitted power dissipation (calculated) added
	157	DC Characteristics	Added Sum input leakage current
	159	A/D converter characteristics; Zero reading voltage, Full scale reading voltage	Changed the units from "LSB" into "V" and the values from <value>+<n> into <value>+<n> LSB
	165	AC Characteristics	Removed the AC specification temporary
	201	Package Dimension	Updated the drawing of FPT-208P-M04 into FPT-208P-M06, updated the URL for download
Ver. 0.4 2009-08-04	all	Total update after first spec review	No change bars in this revision!
Ver. 0.5 2009-08-19	73	USART LIN/FIFO (Extension)	This chapter added for "End of Transmission" IRQ
	108	I/O Map	Marked all differences versus MB91F467D with colors
	138	Interrupt Vector Table	Added the USART "End of Transmission" IRQs
Ver. 0.6 2009-09-08	87	Shutdown mode: External Interrupts: Level or Edge Setting	Added this section
	86	Shutdown mode: Input Voltage Selection	Added this section
	80	Shutdown mode: SHDINT register	Re-added bits [3:2] HWWDF, HWWDE for hardware watchdog
	78	Shutdown mode: All registers	Updated the bit descriptions of all flags, updated the reset conditions of all registers
	89	Shutdown mode: Determining the reset source	Figure updated, Hardware watchdog + Clock supervisor updated
	85	Shutdown mode: Hardware watchdog	Updated the parts about Hardware watchdog, Clock Supervisor completely
	86	Shutdown mode: Clock Supervisor	

Version/ Date	Page	Section	Change Results
Ver. 0.8 2009-10-19	77	Shutdown Mode: Standby RAM	Changed: 1 wait cycle for read, 0 wait cycles for write
	78	Hardware Watchdog: Caution	Updated "Difference between watchdog reset, external reset and Power-on reset"
	84	Shutdown Mode: Precautions	Add setting of EXTE and EXTLV; removed this from Deep Shutdown settings
	90	Shutdown Mode: Registers which are not initialized by Shutdown Recovery	Added this section
	26	Block Diagram	Corrected the connection of Standby RAM (to extended D-bus)
Ver. 0.9 2009-11-24	56	Clock Supervisor, CSVCR register	Added note that bit SCKS must not be changed during CPU runs in Sub clock.
Ver. 1.0 2009-12-15	all	Header	Changed from "Preliminary Short Specification" into "Preliminary Datasheet"
	3	Features	Removed the note about PHILIPS I2C license
	15	Pin Description : Power supply/Ground pins	Added pin 208 to the list of VDD35 pins
	77	Shutdown Mode: Standby RAM	StandBy RAM 1 wait state for read and write
	125	I/O Map	Added note about external bus PFR initial values
	137	I/O Map	StandBy RAM 1 wait state for read and write
	138	Interrupt Vector Table	Re-arranged the table to set correct page breaks
	201	Package Dimension	Link to package database corrected
	74	USART LIN/FIFO (Extension) : FIFO status register for End of Transmission interrupt control	Bits [12:8] of FSR register named NVFD[5:0] (Number of valid FIFO data), name is needed for Softune header file.
Ver. 1.1 2010-01-21	77	Shutdown Mode: Standby RAM	Added notes that, if CLKP is slower than CLKB, there must be a wait time between setting RAMEN and Standby RAM access.
	78	Shutdown Mode: SHDE Register	
	76	Shutdown Mode: Overview	Added notes that reset by external pin INITX=0 will kill the Shutdown state and restart the device like at power-on.
	88	Shutdown Mode: Recovery	
	90	Shutdown Mode: Registers which are not initialized by Shutdown Recovery	
Ver 1.11 2010-06-02	4	Product Lineup	Changed max. CLKB frequency to 100 MHz
	143	Recommended Settings PLL and Clockgear settings	Enabled / allowed the settings which reach CLKB up to 100MHz
	144	Recommended Settings Clock modulator settings	
	158	Electrical Characteristics DC Characteristics	Changed Icc max for CLKB:P:T:CAN = 100:50:50:50 MHz; Updated all current consumption characteristics
	165	Electrical Characteristics AC Characteristics	Chapter AC Characteristics added

# MB91460E Series

DS705-00002-1v2-E		2010-08-15
Page	Section	Changes
1	■ DESCRIPTION	Fujitsu Microelectronics --> Fujitsu Semiconductor
22	■ HANDLING DEVICES 3. Power supply pins	Changed "MB91460D series" --> "MB91460 series"
55	■ CLOCK SUPERVISOR 2.1. Clock Supervisor Control Register (CSVCR)	Description of SCKS bit: On single clock devices always 0
57	■ CLOCK SUPERVISOR 3. Block Diagram Clock Supervisor	Changed input EXT_RST ---> EXT_RST_IN in the drawing
73	■ CLOCK SUPERVISOR 4.11. Check if reset was asserted by the Clock Supervisor	Changed the cross reference text "RSRR: Reset Cause Register" so that the hardware manual is mentioned.
157	■ ELECTRICAL CHARACTERISTICS 3. DC characteristics Sum input leakage current	Changed from max. 40 $\mu$ A to max. 30 $\mu$ A
158	■ ELECTRICAL CHARACTERISTICS 3. DC characteristics Power supply current MB91 F467EA	Updated all I <sub>ccH</sub> values according to evaluation results
159	■ ELECTRICAL CHARACTERISTICS 4. A/D converter characteristics Compare time	Changed T <sub>comp</sub> max from 16,500 $\mu$ s to "t.b.d." because this parameter is under re-evaluation.
172 186	■ ELECTRICAL CHARACTERISTICS 7. AC characteristics 7.7. External Bus AC Timings at VDD35 = 4.5 to 5.5 V 7.8. External Bus AC Timings at VDD35 = 3.0 to 4.5 V	Changed all symbol names from upper case strings to the commonly used style. Example: Changed TCLCH into t <sub>CLCH</sub>
172	■ ELECTRICAL CHARACTERISTICS 7. AC characteristics 7.7. External Bus AC Timings at VDD35 = 4.5 to 5.5 V	Updated all timing information according to the evaluation results
186	■ ELECTRICAL CHARACTERISTICS 7. AC characteristics 7.8. External Bus AC Timings at VDD35 = 3.0 to 4.5 V	Updated all timing information according to the evaluation results
200	■ ORDERING INFORMATION	Removed the remark that the "device is under development"

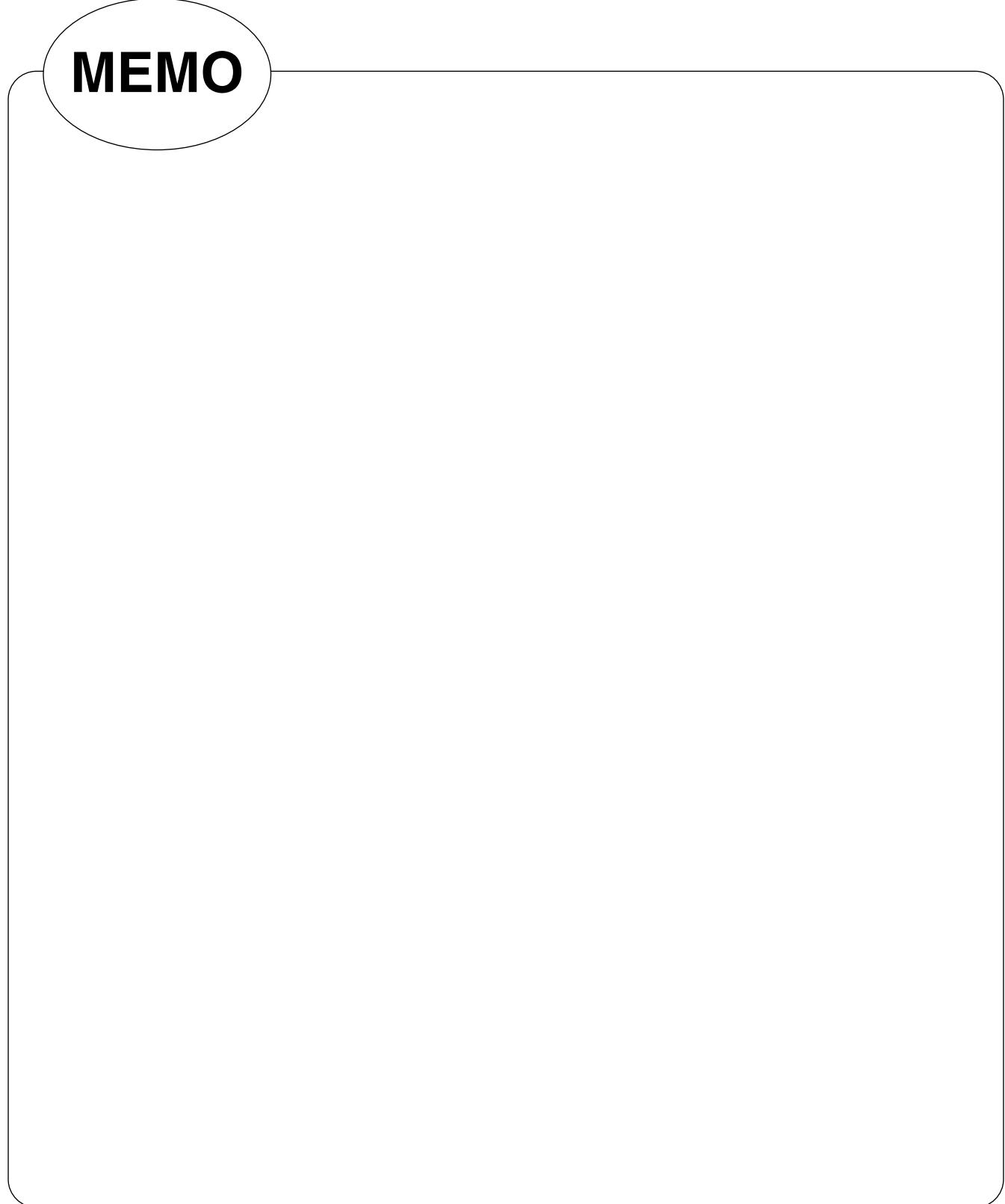
## ■ CHANGES IN THIS EDITION

DS705-00002-1v3-E		2010-10-01
Page	Section	Changes
172 186	■ ELECTRICAL CHARACTERISTICS 7. AC characteristics 7.7. External Bus AC Timings at VDD35 = 4.5 to 5.5 V 7.8. External Bus AC Timings at VDD35 = 3.0 to 4.5 V	Corrected the condition of VOL from $0.2 \times V_{DD35}$ into $0.5 \times V_{DD35}$ VOH from $0.8 \times V_{DD35}$ into $0.5 \times V_{DD35}$
182 196	■ ELECTRICAL CHARACTERISTICS 7. AC characteristics 7.7.9. Bus hold timing 7.8.9. Bus hold timing	Added note about condition for $t_{AXBGL}$ and $t_{BGHAV}$ : - VOL = $0.2 \times V_{DD35}$ - VOH = $0.8 \times V_{DD35}$
200	■ ORDERING INFORMATION	Corrected the product number from MB91F467EAPFVS-GSE2 into MB91F467EAPMC-GSE2

## ■ MEMO AND DISCLAIMER

**MEMO**

**MEMO**



## FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,

Kohoku-ku Yokohama Kanagawa 222-0033, Japan

Tel: +81-45-415-5858

<http://jp.fujitsu.com/fsl/en/>

For further information please contact:

### North and South America

FUJITSU SEMICONDUCTOR AMERICA, INC.

1250 E. Arques Avenue, M/S 333

Sunnyvale, CA 94085-5401, U.S.A.

Tel: +1-408-737-5600 Fax: +1-408-737-5999

<http://www.fma.fujitsu.com/>

### Europe

FUJITSU SEMICONDUCTOR EUROPE GmbH

Pittlerstrasse 47, 63225 Langen, Germany

Tel: +49-6103-690-0 Fax: +49-6103-690-122

<http://emea.fujitsu.com/semiconductor/>

### Korea

FUJITSU SEMICONDUCTOR KOREA LTD.

206 Kosmo Tower Building, 1002 Daechi-Dong,

Gangnam-Gu, Seoul 135-280, Republic of Korea

Tel: +82-2-3484-7100 Fax: +82-2-3484-7111

<http://kr.fujitsu.com/fmk/>

### Asia Pacific

FUJITSU SEMICONDUCTOR ASIA PTE. LTD.

151 Lorong Chuan,

#05-08 New Tech Park 556741 Singapore

Tel : +65-6281-0770 Fax : +65-6281-0220

<http://www.fmal.fujitsu.com/>

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.

Rm. 3102, Bund Center, No.222 Yan An Road (E),

Shanghai 200002, China

Tel : +86-21-6146-3688 Fax : +86-21-6335-1605

<http://cn.fujitsu.com/fmc/>

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.

10/F, World Commerce Centre, 11 Canton Road,

Tsimshatsui, Kowloon, Hong Kong

Tel : +852-2377-0226 Fax : +852-2376-3269

<http://cn.fujitsu.com/fmc/en/>

Specifications are subject to change without notice. For further information please contact each office.

### All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU SEMICONDUCTOR device; FUJITSU SEMICONDUCTOR does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.

FUJITSU SEMICONDUCTOR assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU SEMICONDUCTOR or any third party or does FUJITSU SEMICONDUCTOR warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU SEMICONDUCTOR assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that FUJITSU SEMICONDUCTOR will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.

Edited: Fujitsu Semiconductor Europe GmbH

