

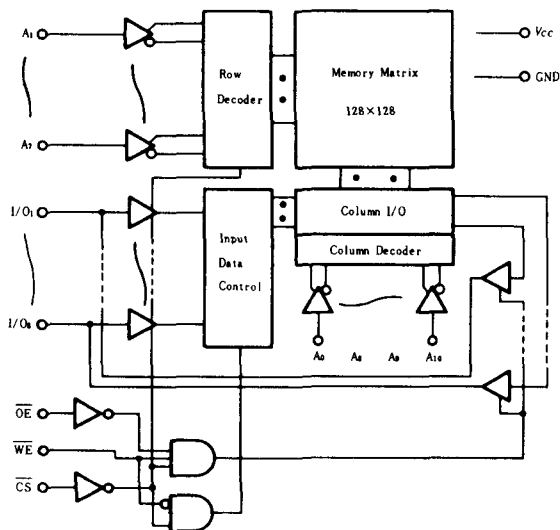
HM6116-2, HM6116-3, HM6116-4 HM6116P-2, HM6116P-3, HM6116P-4

2048-word × 8-bit High Speed Static CMOS RAM

FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 100μW (typ.)
- Low Power Operation Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

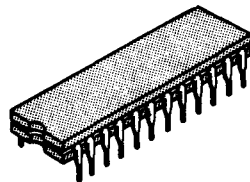
Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	-55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	-65 to +150	°C
Temperature Under Bias	T_{hstg}	-10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns; $-3.5V$

TRUTH TABLE

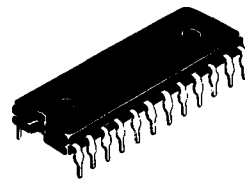
CS	OE	WE	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SS}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

HM6116-2, HM6116-3,
HM6116-4



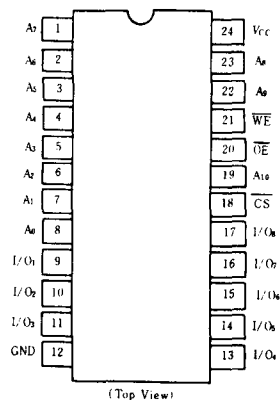
(DG-24)

HM6116P-2, HM6116P-3,
HM6116P-4



(DP-24)

PIN ARRANGEMENT



(Top View)

RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^{\circ}\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-3.0^*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V}\pm 10\%$, GND=0V, $T_a=0$ to $+70^{\circ}\text{C}$)

Item	Symbol	Test Conditions	HM6116/P-2			HM6116/P-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5\text{V}$, $V_{in}=\text{GND to } V_{CC}$	—	—	10	—	—	10	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}=V_{IH}$ or $\overline{\text{OE}}=V_{IH}$, $V_{LO}=\text{GND to } V_{CC}$	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}=V_{IL}$, $I_{LO}=0\text{mA}$	—	40	80	—	35	70	mA
	I_{CC1}^{**}	$V_{IH}=3.5\text{V}$, $V_{IL}=0.6\text{V}$, $I_{LO}=0\text{mA}$	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty = 100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{\text{CS}}\geq V_{CC}-0.2\text{V}$, $V_{in}\geq V_{CC}-0.2\text{V}$ or $V_{in}\leq 0.2\text{V}$	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	$I_{OL}=4\text{mA}$	—	—	0.4	—	—	—	V
		$I_{OL}=2.1\text{mA}$	—	—	—	—	—	0.4	V
	V_{OH}	$I_{OH}=1.0\text{mA}$	2.4	—	—	2.4	—	—	V

* $V_{CC}=5\text{V}$, $T_a=25^{\circ}\text{C}$

** Reference Only

AC CHARACTERISTICS ($V_{CC}=5\text{V}\pm 10\%$, $T_a=0$ to $+70^{\circ}\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

READ CYCLE

Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{ONZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116/P-2		HM6116/P-3		HM6116/P-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

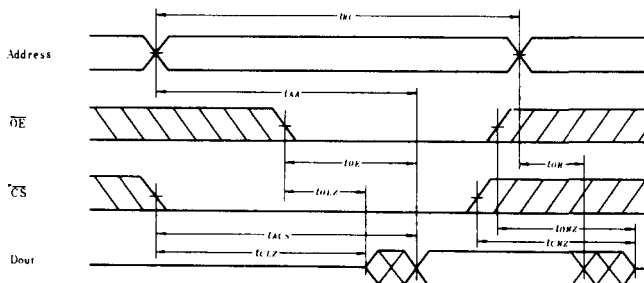
■ CAPACITANCE ($f=1\text{MHz}$, $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{iA}	$V_{iA}=0\text{V}$	3	5	pF
Input/Output Capacitance	C_{iO}	$V_{iO}=0\text{V}$	5	7	pF

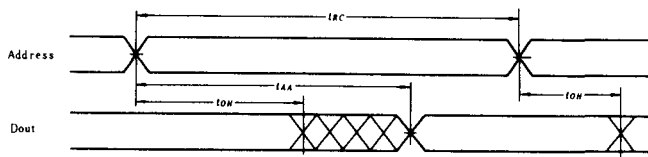
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

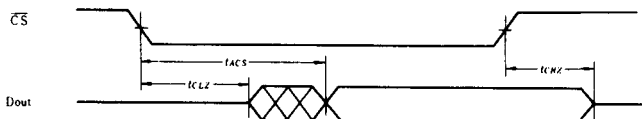
● READ CYCLE (1) ⁽¹⁾



● READ CYCLE (2) ⁽¹⁾⁽²⁾⁽⁴⁾

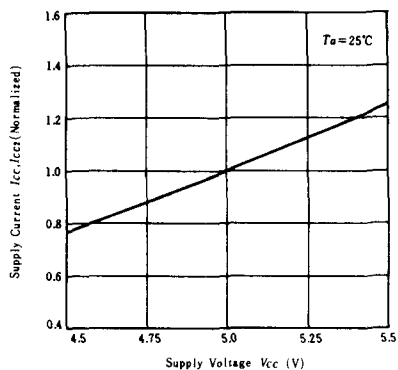


● READ CYCLE (3) ⁽¹⁾⁽³⁾⁽⁴⁾

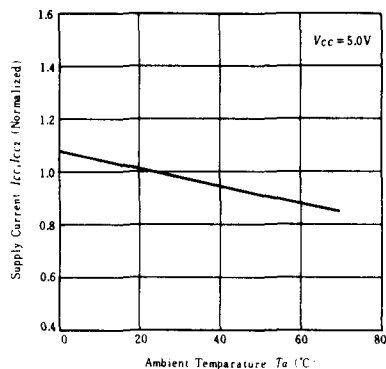


- NOTES:
1. $\overline{WE}$ is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
 4. $\overline{OE} = V_{IL}$.

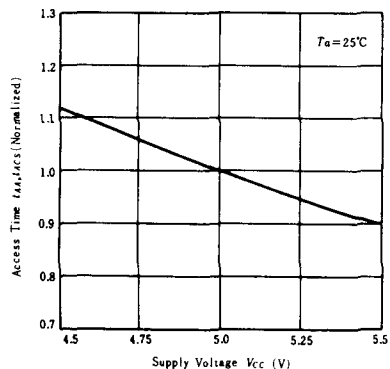
**SUPPLY CURRENT
vs. SUPPLY VOLTAGE**



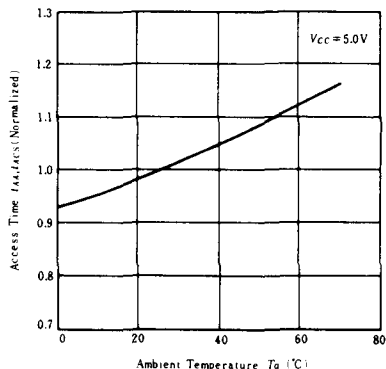
**SUPPLY CURRENT
vs. AMBIENT TEMPERATURE**



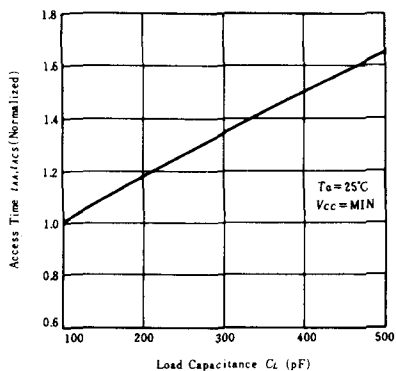
**ACCESS TIME
vs. SUPPLY VOLTAGE**



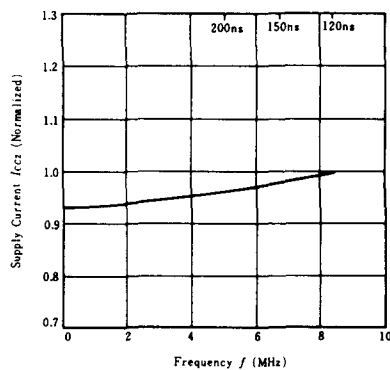
**ACCESS TIME
vs. AMBIENT TEMPERATURE**



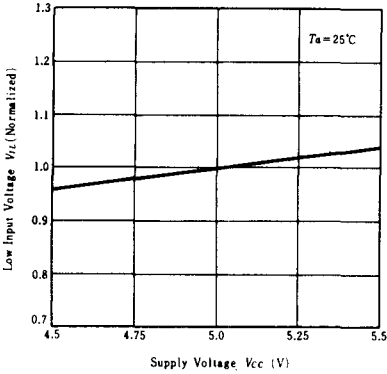
**ACCESS TIME
vs. LOAD CAPACITANCE**



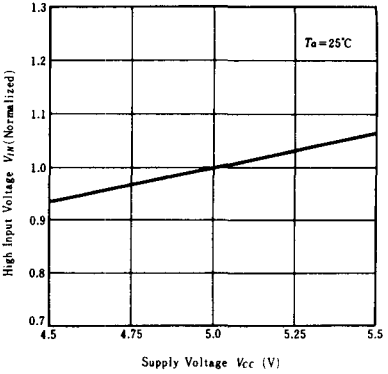
**SUPPLY CURRENT
vs. FREQUENCY**



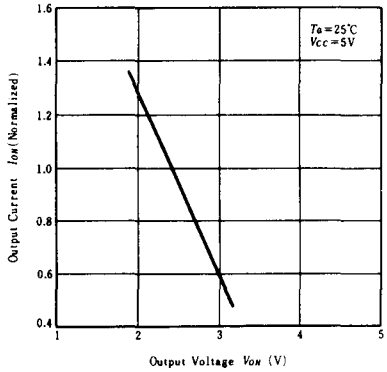
**LOW INPUT VOLTAGE
vs. SUPPLY VOLTAGE**



**HIGH INPUT VOLTAGE
vs. SUPPLY VOLTAGE**



**OUTPUT CURRENT
vs. OUTPUT VOLTAGE**



**OUTPUT CURRENT
vs. OUTPUT VOLTAGE**

