

FEATURES

- 400 mV $\pm$ 1.5% threshold**
- Supply range: 1.7 V to 5.5 V**
- Low quiescent current: 6.5 μ A typical**
- Input range includes ground**
- Internal hysteresis: 8.9 mV typical**
- Low input bias current: $\pm$ 10 nA maximum**
- Open-drain outputs**
- Supports wire-AND connections**
- Input polarities: one inverting and one noninverting**
- Low profile (1 mm) TSOT package**
- Drop-in replacement for the LT6700-1**

APPLICATIONS

- Li-Ion monitoring**
- Portable applications**
- Hand-held instruments**
- Window comparators**
- LED/relay driving**
- Optoisolator driving**
- Control systems**

GENERAL DESCRIPTION

The ADCMP670 consists of two low power, high accuracy, comparator and reference circuits in a 6-lead TSOT package. The internal 400 mV reference provides the ability to monitor low voltage supplies. The device operates on a supply voltage from 1.7 V to 5.5 V and draws only 6.5 μ A typical, making it suitable for low power system monitoring and portable applications. Hysteresis is included in the comparators. The comparator outputs are open-drain and the output can be pulled up to any voltage up to 5.5 V. The output stage is guaranteed to sink greater than 5 mA over temperature.

The ADCMP670 is currently available in one model, the ADCMP670-1. This model has one inverting input and one noninverting input, making it suitable for use as a window comparator. The device is suitable for portable, commercial, industrial, and automotive applications.

FUNCTIONAL BLOCK DIAGRAM

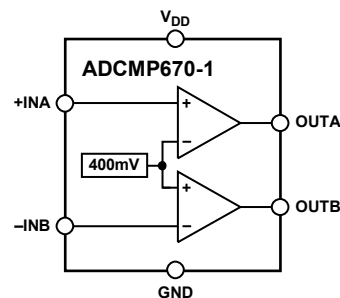


Figure 1.

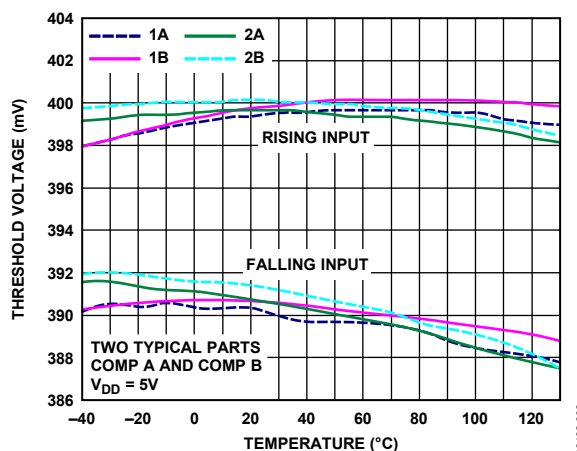


Figure 2. Comparator Thresholds vs. Temperature

Rev. A

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ADCMP670* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADCMP670: Dual Low Power 1.5% Comparator With 400 mV Reference Data Sheet

REFERENCE DESIGNS

- CN0190
- CN0343

REFERENCE MATERIALS

Product Selection Guide

- Comparators Product Brochure 2007

DESIGN RESOURCES

- ADCMP670 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADCMP670 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

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REVISION HISTORY

7/09—Rev. 0 to Rev. A	
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2/07—Revision 0: Initial Version	

SPECIFICATIONS

$V_{DD} = 1.7 \text{ V to } 5.5 \text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLDS¹					
Rising Input Threshold Voltage	394	400	406	mV	$V_{DD} = 1.7 \text{ V}$
	395	400	405	mV	$V_{DD} = 5.5 \text{ V}$
Falling Input Threshold Voltage	386	391.1	401	mV	$V_{DD} = 1.7 \text{ V}$
	387	391.1	400	mV	$V_{DD} = 5.5 \text{ V}$
Hysteresis = $V_{TH(R)} - V_{TH(F)}$	7	8.9	11	mV	
INPUT CHARACTERISTICS					
Input Bias Current		0.01	10	nA	$V_{DD} = 1.7 \text{ V}$, $V_{IN} = V_{DD}$
		4	10	nA	$V_{DD} = 1.7 \text{ V}$, $V_{IN} = 0.1 \text{ V}$
OPEN-DRAIN OUTPUTS					
Output Low Voltage ²		140	200	mV	$V_{DD} = 1.7 \text{ V}$, $I_{OUT} = 3 \text{ mA}$
		130	200	mV	$V_{DD} = 5.5 \text{ V}$, $I_{OUT} = 5 \text{ mA}$
Output Leakage Current ³		0.01	0.8	μA	$V_{DD} = 1.7 \text{ V}$, $V_{OUT} = V_{DD}$
		0.01	0.8	μA	$V_{DD} = 1.7 \text{ V}$, $V_{OUT} = 5.5 \text{ V}$
DYNAMIC PERFORMANCE^{2, 4}					
High-to-Low Propagation Delay		10		μs	$V_{DD} = 5.5 \text{ V}$, $V_{OL} = 400 \text{ mV}$
Low-to-High Propagation Delay		8		μs	$V_{DD} = 5.5 \text{ V}$, $V_{OH} = 0.9 \times V_{DD}$
Output Rise Time		0.5		μs	$V_{DD} = 5.5 \text{ V}$, $V_O = (0.1 \text{ to } 0.9) \times V_{DD}$
Output Fall Time		0.07		μs	$V_{DD} = 5.5 \text{ V}$, $V_O = (0.1 \text{ to } 0.9) \times V_{DD}$
POWER SUPPLY					
Supply Current ⁵		5.7	10	μA	$V_{DD} = 1.7 \text{ V}$
		6.5	11	μA	$V_{DD} = 5.5 \text{ V}$

¹ $R_L = 100 \text{ k}\Omega$, $V_O = 2 \text{ V}$ swing.

² 10 mV input overdrive.

³ $V_{IN} = 40 \text{ mV}$ overdrive.

⁴ $R_L = 10 \text{ k}\Omega$.

⁵ No load current.

ADCMP670

$V_{DD} = 1.7 \text{ V to } 5.5 \text{ V}$, $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLDS¹					
Rising Input Threshold Voltage	391		409	mV	$V_{DD} = 1.7 \text{ V}$
	392.5		407.5	mV	$V_{DD} = 5.5 \text{ V}$
Falling Input Threshold Voltage	383.5		403.5	mV	$V_{DD} = 1.7 \text{ V}$
	384.5		402.5	mV	$V_{DD} = 5.5 \text{ V}$
Hysteresis = $V_{TH(R)} - V_{TH(F)}$	6.5		12.5	mV	
INPUT CHARACTERISTICS					
Input Bias Current			15	nA	$V_{DD} = 1.7 \text{ V}$, $V_{IN} = V_{DD}$
			15	nA	$V_{DD} = 1.7 \text{ V}$, $V_{IN} = 0.1 \text{ V}$
OPEN-DRAIN OUTPUTS					
Output Low Voltage ²			250	mV	$V_{DD} = 1.7 \text{ V}$, $I_{OUT} = 3 \text{ mA}$
			250	mV	$V_{DD} = 5.5 \text{ V}$, $I_{OUT} = 5 \text{ mA}$
Output Leakage Current ³			1	μA	$V_{DD} = 1.7 \text{ V}$, $V_{OUT} = V_{DD}$
			1	μA	$V_{DD} = 1.7 \text{ V}$, $V_{OUT} = 5.5 \text{ V}$
POWER SUPPLY					
Supply Current ⁴			13	μA	$V_{DD} = 1.7 \text{ V}$
			14	μA	$V_{DD} = 5.5 \text{ V}$

¹ $R_L = 100 \text{ k}\Omega$, $V_O = 2 \text{ V}$ swing.

² 10 mV input overdrive.

³ $V_{IN} = 40 \text{ mV}$ overdrive.

⁴ No load.

$V_{DD} = 1.7 \text{ V to } 5.5 \text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLDS¹					
Rising Input Threshold Voltage	390		410	mV	$V_{DD} = 1.7 \text{ V}$
	392		408	mV	$V_{DD} = 5.5 \text{ V}$
Falling Input Threshold Voltage	382.5		404.5	mV	$V_{DD} = 1.7 \text{ V}$
	383.5		403.5	mV	$V_{DD} = 5.5 \text{ V}$
Hysteresis = $V_{TH(R)} - V_{TH(F)}$	5.5		13.0	mV	
INPUT CHARACTERISTICS					
Input Bias Current			15	nA	$V_{DD} = 1.7 \text{ V}$, $V_{IN} = V_{DD}$
			15	nA	$V_{DD} = 1.7 \text{ V}$, $V_{IN} = 0.1 \text{ V}$
OPEN-DRAIN OUTPUTS					
Output Low Voltage ²			250	mV	$V_{DD} = 1.7 \text{ V}$, $I_{OUT} = 3 \text{ mA}$
			250	mV	$V_{DD} = 5.5 \text{ V}$, $I_{OUT} = 5 \text{ mA}$
Output Leakage Current ³			1	μA	$V_{DD} = 1.7 \text{ V}$, $V_{OUT} = V_{DD}$
			1	μA	$V_{DD} = 1.7 \text{ V}$, $V_{OUT} = 5.5 \text{ V}$
POWER SUPPLY					
Supply Current ⁴			14	μA	$V_{DD} = 1.7 \text{ V}$
			15	μA	$V_{DD} = 5.5 \text{ V}$

¹ $R_L = 100 \text{ k}\Omega$, $V_O = 2 \text{ V}$ swing.

² 10 mV input overdrive.

³ $V_{IN} = 40 \text{ mV}$ overdrive.

⁴ No load.

$V_{DD} = 1.7 \text{ V to } 5.5 \text{ V}$, $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
THRESHOLDS¹					
Rising Input Threshold Voltage	390		411	mV	$V_{DD} = 1.7 \text{ V}$
	392		410	mV	$V_{DD} = 5.5 \text{ V}$
Falling Input Threshold Voltage	381.5		405.5	mV	$V_{DD} = 1.7 \text{ V}$
	381.05		404.5	mV	$V_{DD} = 5.5 \text{ V}$
Hysteresis = $V_{TH(R)} - V_{TH(F)}$	2		13.5	mV	
INPUT CHARACTERISTICS					
Input Bias Current			45	nA	$V_{DD} = 1.7 \text{ V}, V_{IN} = V_{DD}$
			45	nA	$V_{DD} = 1.7 \text{ V}, V_{IN} = 0.1 \text{ V}$
OPEN-DRAIN OUTPUTS					
Output Low Voltage ²			250	mV	$V_{DD} = 1.7 \text{ V}, I_{OUT} = 3 \text{ mA}$
			250	mV	$V_{DD} = 5.5 \text{ V}, I_{OUT} = 5 \text{ mA}$
Output Leakage Current ³			1	μA	$V_{DD} = 1.7 \text{ V}, V_{OUT} = V_{DD}$
			1	μA	$V_{DD} = 1.7 \text{ V}, V_{OUT} = 5.5 \text{ V}$
POWER SUPPLY					
Supply Current ⁴			16	μA	$V_{DD} = 1.7 \text{ V}$
			17	μA	$V_{DD} = 5.5 \text{ V}$

¹ $R_L = 100 \text{ k}\Omega$, $V_O = 2 \text{ V}$ swing.

² 10 mV input overdrive.

³ $V_{IN} = 40 \text{ mV}$ overdrive.

⁴ No load.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Range
V _{DD}	−0.3 V to +6 V
+INA, −INB	−0.3 V to +6 V
OUTA, OUTB	−0.3 V to +6 V
Output Short Circuit Duration ¹	Indefinite
Input Current	−10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

¹ When the output is shorted indefinitely, the use of a heat sink may be required to keep the junction temperature within the absolute maximum ratings.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Lead TSOT	200	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

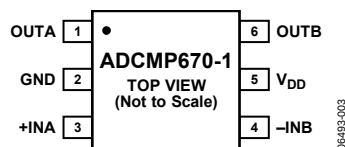


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUTA	Open-Drain Output for Comparator A.
2	GND	Ground.
3	+INA	Monitors analog input voltage on Comparator A. Connected to noninverting input. The other input of Comparator A is connected to a 400 mV reference.
4	-INB	Monitors analog input voltage on Comparator B. Connected to inverting input. The other input of Comparator B is connected to a 400 mV reference.
5	V _{DD}	Power Supply Pin.
6	OUTB	Open-Drain Output for Comparator B.

TYPICAL PERFORMANCE CHARACTERISTICS

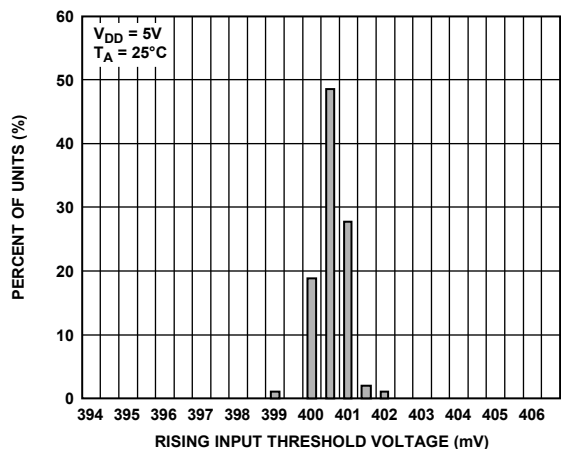


Figure 4. Distribution of Rising Input Threshold Voltage

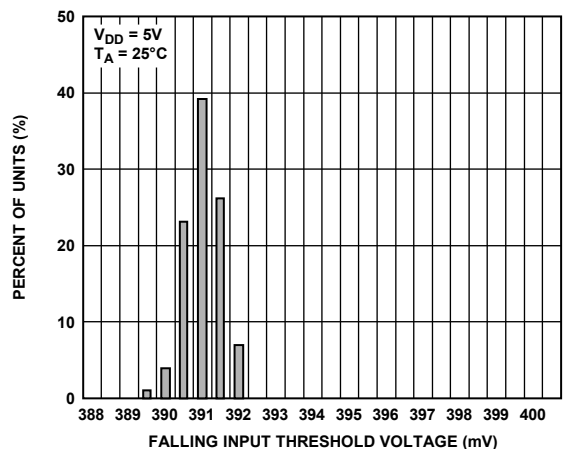


Figure 7. Distribution of Falling Input Threshold Voltage

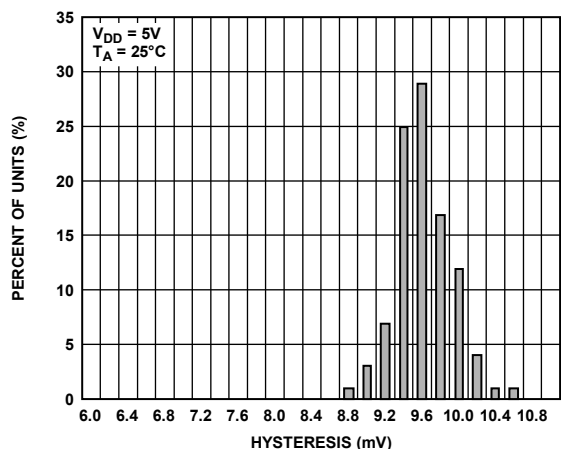


Figure 5. Distribution of Hysteresis

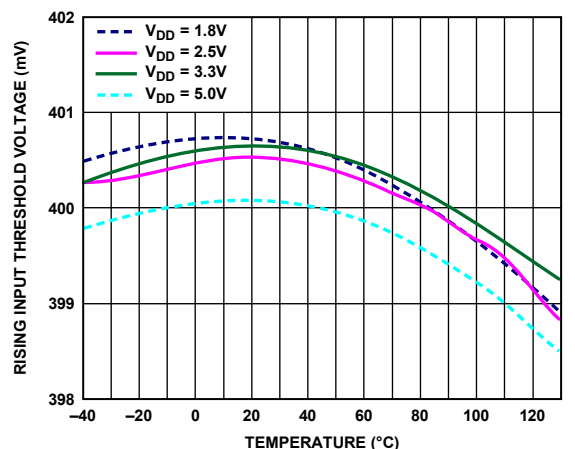


Figure 8. Rising Input Threshold Voltage vs. Temperature

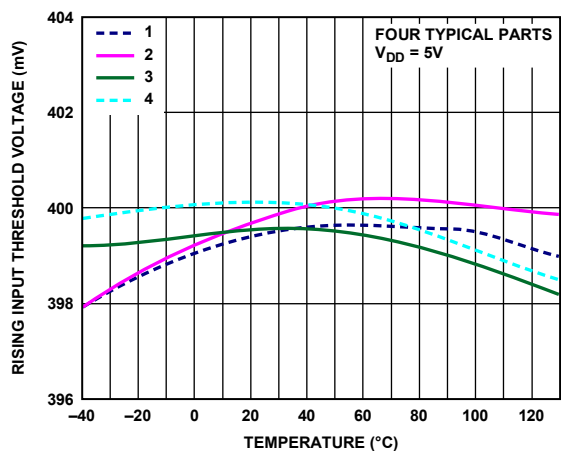


Figure 6. Rising Input Threshold Voltage vs. Temperature

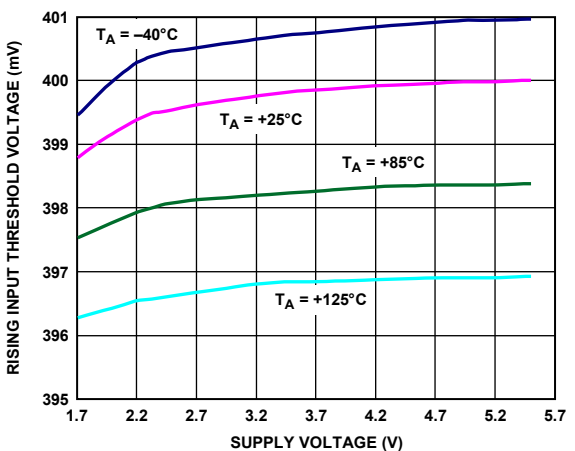


Figure 9. Rising Input Threshold Voltage vs. Supply Voltage

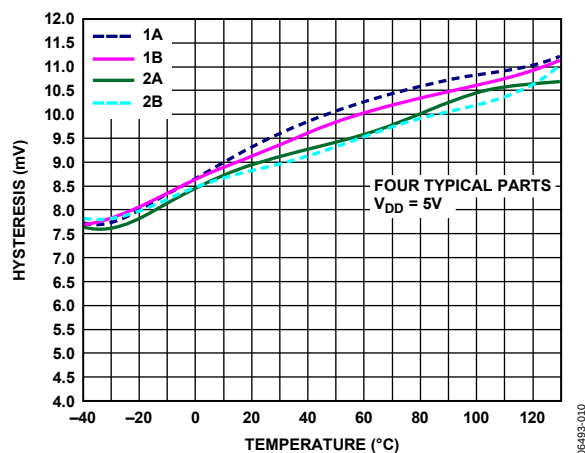


Figure 10. Hysteresis vs. Temperature

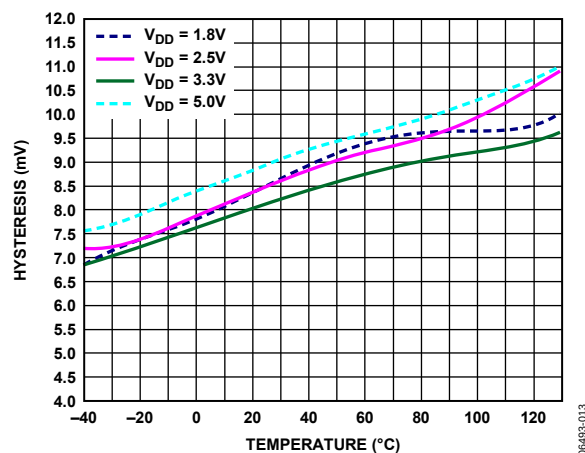


Figure 13. Hysteresis vs. Temperature

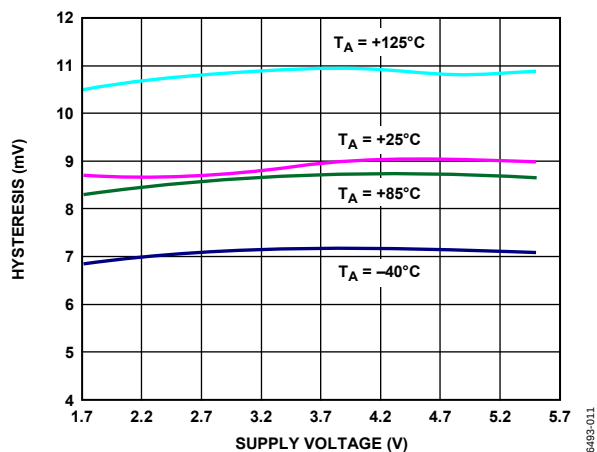


Figure 11. Hysteresis vs. Supply Voltage

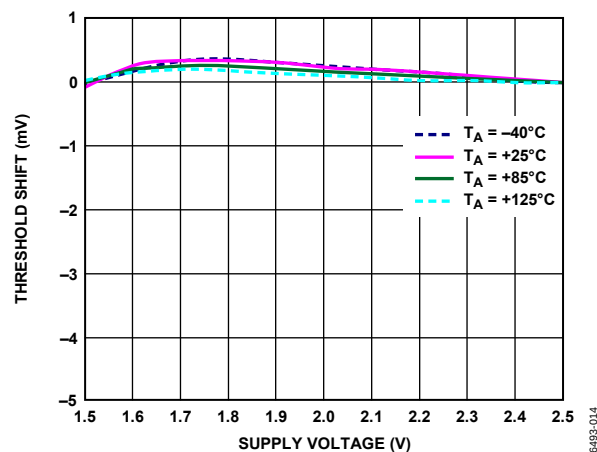


Figure 14. Minimum Supply Voltage

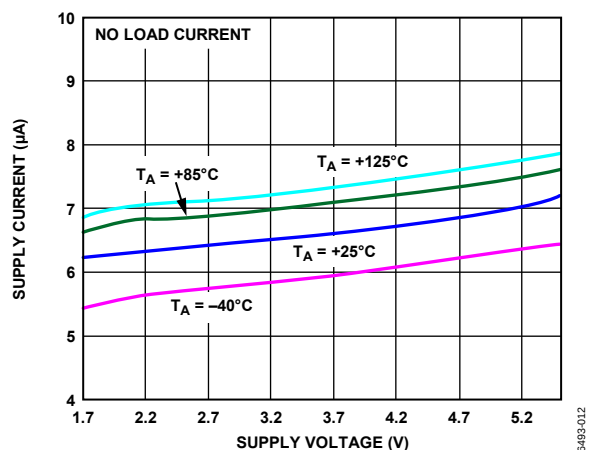


Figure 12. Quiescent Supply Current vs. Supply Voltage

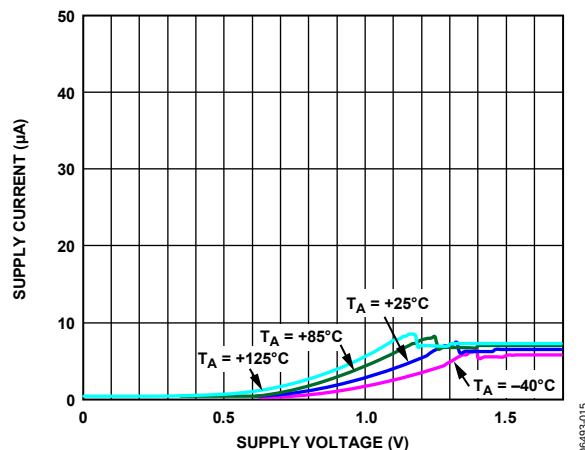


Figure 15. Startup Supply Current

ADCMP670

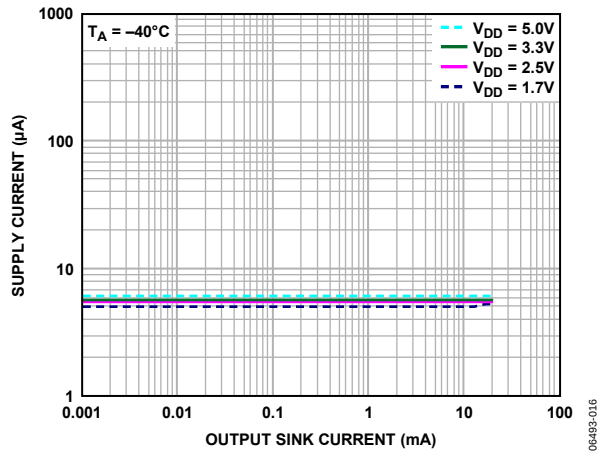


Figure 16. Supply Current vs. Output Sink Current

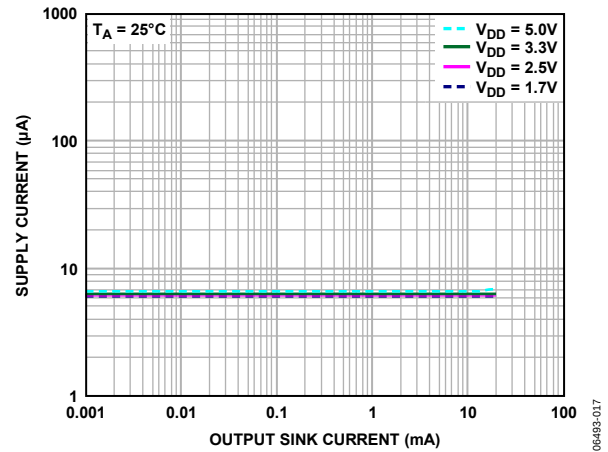


Figure 19. Supply Current vs. Output Sink Current

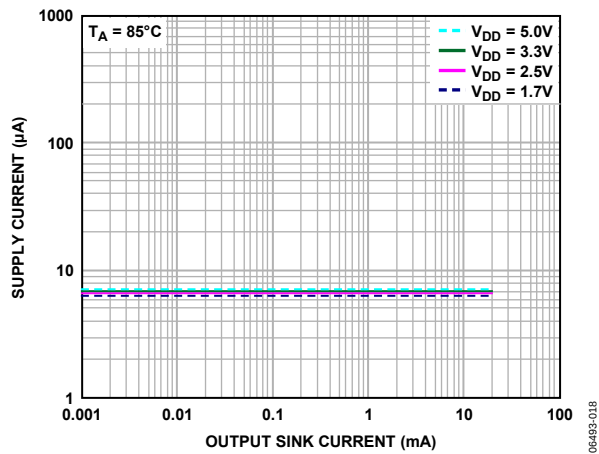


Figure 17. Supply Current vs. Output Sink Current

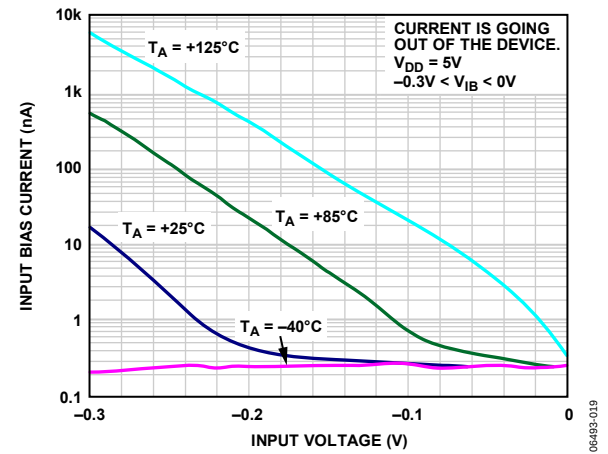


Figure 20. Below Ground Input Bias Current

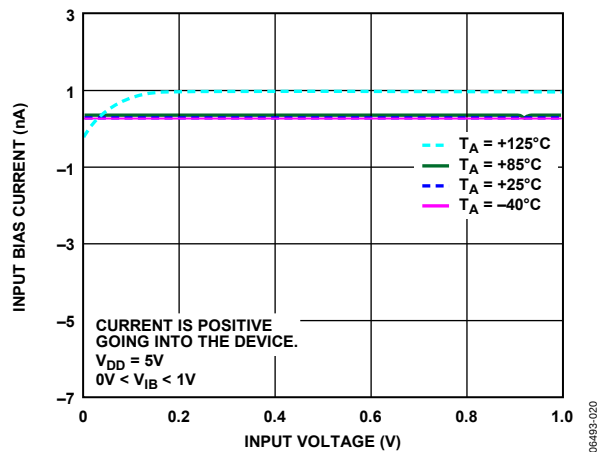


Figure 18. Low Level Input Bias Current

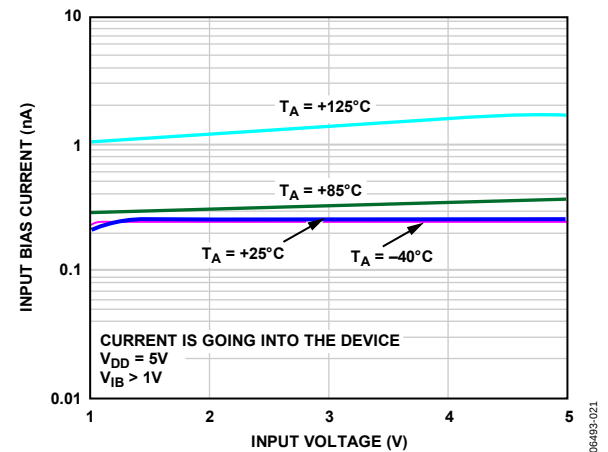


Figure 21. High Level Input Bias Current

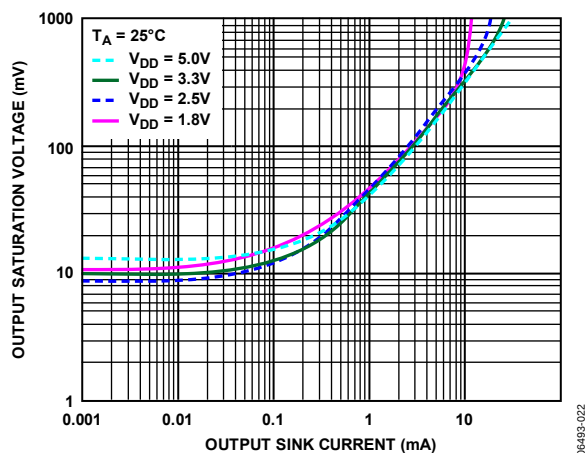


Figure 22. Output Saturation Voltage vs. Output Sink Current

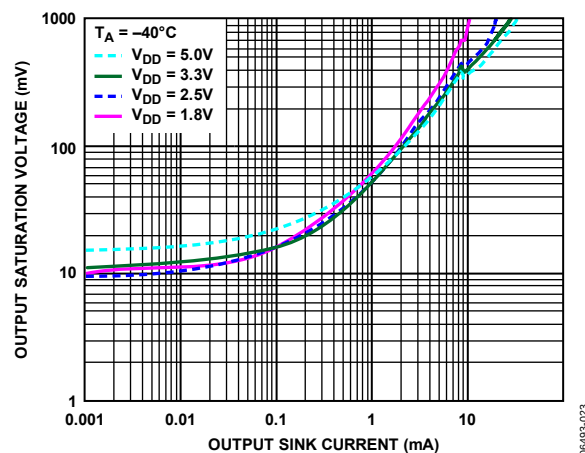


Figure 25. Output Saturation Voltage vs. Output Sink Current

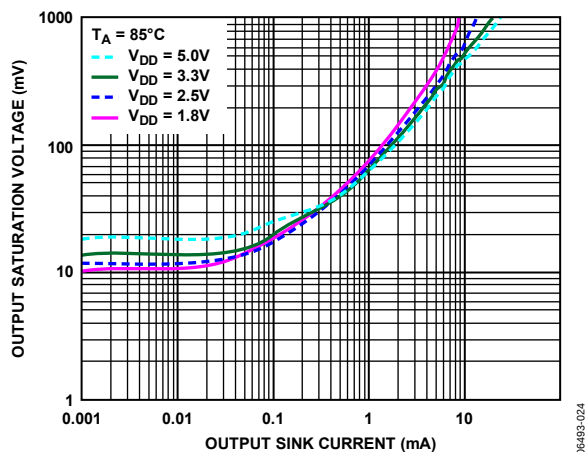


Figure 23. Output Saturation Voltage vs. Output Sink Current

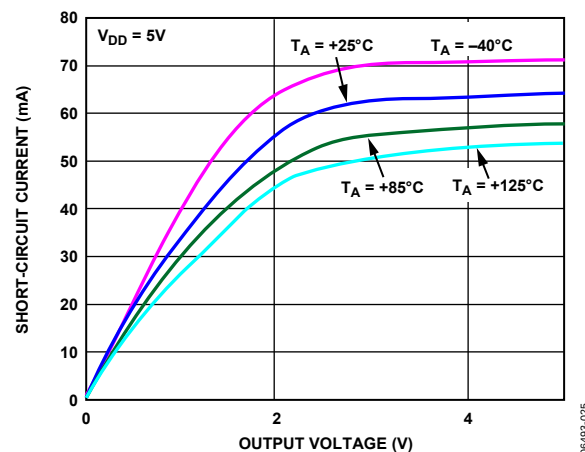


Figure 26. Output Short-Circuit Current

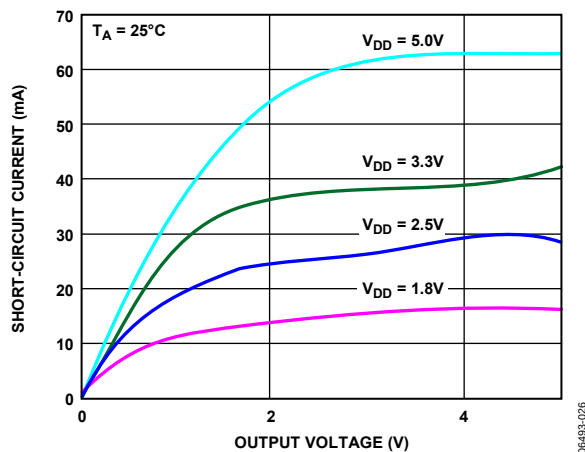


Figure 24. Output Short-Circuit Current

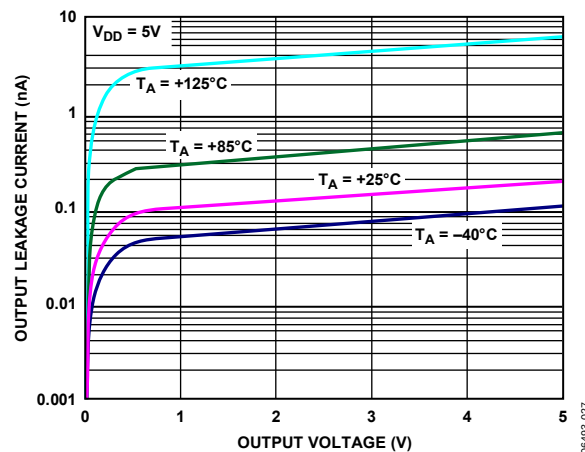


Figure 27. Output Leakage Current

ADCMP670

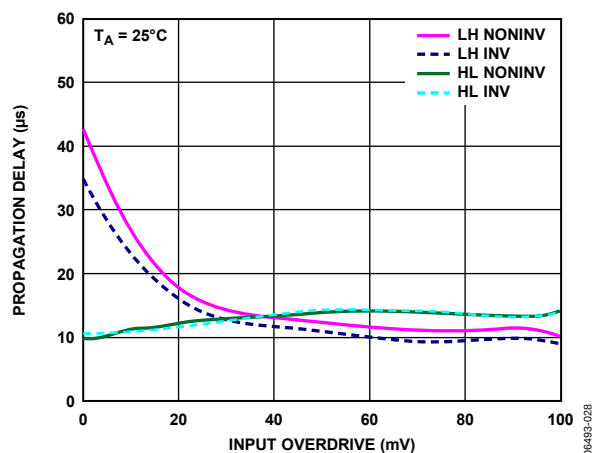


Figure 28. Propagation Delay vs. Input Overdrive

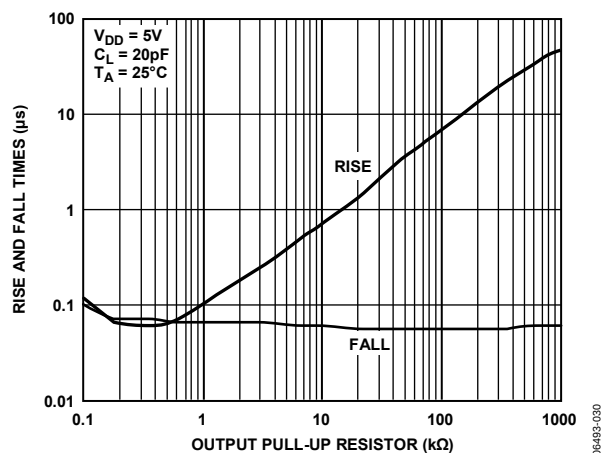


Figure 30. Rise and Fall Times vs. Output Pull-Up Resistor

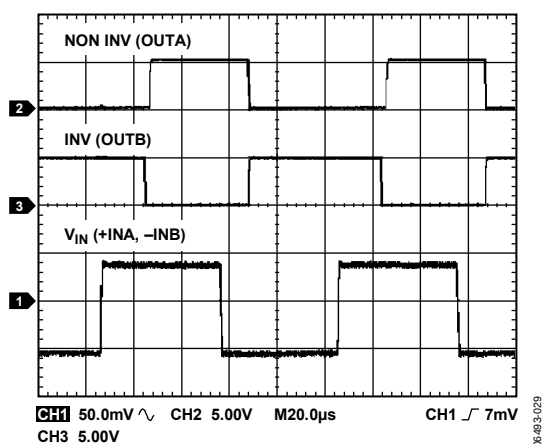


Figure 29. Noninverting and Inverting Comparators Propagation Delay

APPLICATION INFORMATION

The ADCMP670 is a dual low power comparator with a built-in 400 mV reference that operates from 1.7 V to 5.5 V. The comparator is 1.5% accurate with a built-in hysteresis of 8.9 mV. The outputs are open-drain, capable of sinking 40 mA.

COMPARATORS AND INTERNAL REFERENCE

Each comparator has one input available externally.

Comparator A has a noninverting input and Comparator B has an inverting input available. The other comparator inputs are connected internally to the 400 mV reference. The rising input threshold voltage of the comparators is designed to be equal to that of the reference.

POWER SUPPLY

The ADCMP670 is designed to operate from 1.7 V to 5.5 V. A 0.1 μ F decoupling capacitor is recommended between V_{DD} and GND.

INPUTS

The comparator inputs are limited to the maximum V_{DD} voltage range. The voltage on these inputs can be above V_{DD} but never above the maximum allowed V_{DD} voltage. When adding a resistor string to the input, care must be taken when choosing resistor values. This is due to the fact that the input bias current will be in parallel with the bottom resistor of the string. This bottom resistor must therefore be chosen first to control the error introduced by this bias current.

OUTPUTS

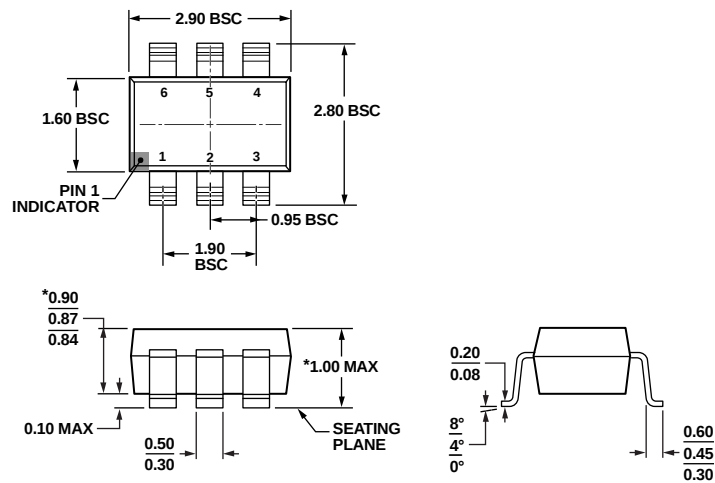
The comparator outputs are open-drain and are also limited to the maximum specified V_{DD} voltage range, regardless of the V_{DD} voltage. These outputs are capable of sinking up to 40 mA. Outputs can be tied together to provide a window comparator with a single output.

ADDING HYSTERESIS

To prevent oscillations at the output caused by noise or slowly moving signals passing the switching threshold, each comparator has built-in hysteresis of approximately 8.9 mV. Positive feedback can be used to increase hysteresis to the noninverting comparator.

ADCMP670

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-193-AA WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 31.. 6-Lead Thin Small Outline Transistor Package [TSOT] (UJ-6)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADCMP670-1YUJZ-RL7 ¹	−40°C to +125°C	6-Lead Thin Small Outline Transistor Package [TSOT]	UJ-6	M97

¹ Z = RoHS Compliant Part.

NOTES

NOTES