UM8250A

Asynchronous Communication Element (ACE)

Jameco Part Number 52610

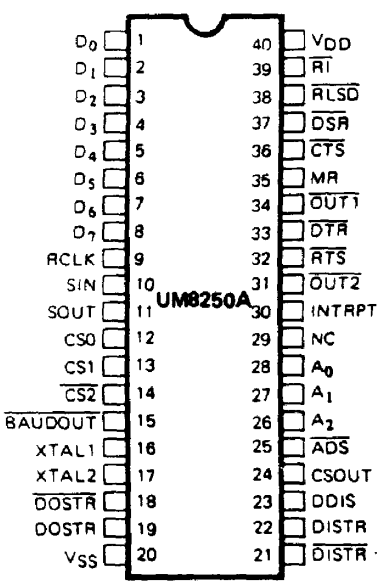
Features

- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from serial data stream.
- Full double buffering eliminates need for precise synchronization.
- Independently-controlled transmit, receive, line status, and data set interrupts.
- Programmable baud rate generator allows division of any input clock by 1 to $(2^{16}-1)$ and generates the internal 16X clock.
- Independent receiver clock input.
- Modem control functions (CTS, RTS, DSR, DTR, RI, and carrier detect).
- Single +5 volt power supply.
- Fully programmable serial-interface characteristics.
  - 5-, 6-, 7-, or 8-bit characters.
  - Even, odd, or no-parity bit generation and detection.
  - 1-, 1½-, or 2-stop bit generation.
  - Baud rate generation (DC to 56K baud).
- False start bit detection.
- Complete status reporting capabilities.
- Easily interfaces to most popular microprocessors.
- Line break generation and detection.
- Internal diagnostic capabilities.
  - Loopback controls for communications link fault isolation.
  - Break, parity, overrun, framing error simulation.
- Full prioritized interrupt system controls.

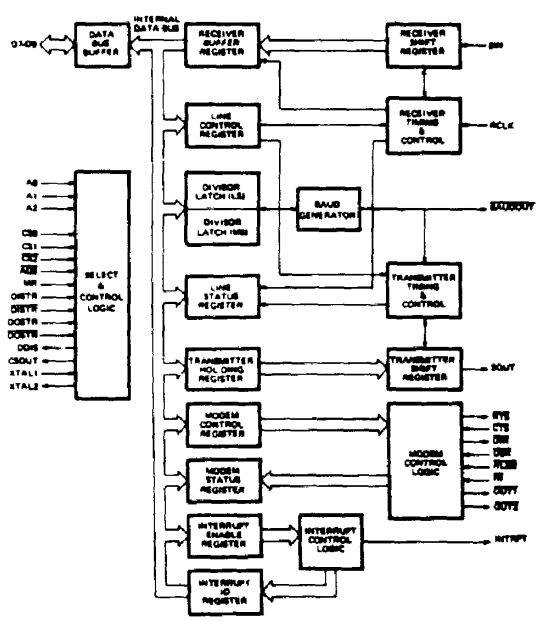
General Description

The UM8250A is a programmable Asynchronous Communication Element (ACE) chip fabricated with Si-Gate NMOS process. This product performs serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the ACE at any time during operation. It also includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16}-1)$, and producing a 16X clock for driving the internal transmitter logic.

Pin Configuration



Block Diagram



Absolute Maximun Rating*

D.C. Supply Voltage V_{DD} . . . . . −0.5V to 7V

(With respect to V_{SS})

Operating Temperature. . . . . .0°C − 70°C

Storage Temperature . . . . . −65°C − 150°C

Comments*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. Characteristics

(T_A = 25°C, V_{DD} = 5V ± 5% unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IHX}	Clock Input High-Level Voltage	2.0	–	V_{DD}	V	
V_{ILX}	Clock Input Low-Level Voltage	−0.5	–	0.8	V	
V_{IH}	Input High-Level Voltage	2.0	–	V_{DD}	V	
V_{IL}	Input Low-Level Voltage	−0.5	–	0.8	V	
V_{OH}	Output High-Level Voltage	2.4	–	–	V	I_{OL} = 1.6 mA on all outputs
V_{OL}	Output Low-Level Voltage	–	–	0.4	V	I_{OH} = −100 uA on all outputs
I_{IN}	Input Leakage	–	–	±10	uA	V_{IN} = 5V − 0V
I_{CIN}	Input Leakage	–	–	±10	uA	Clock input
I_{CC} (AVG)	AVG Power Supply Current	–	–	90	mA	V_{IN} = V_{DD} or 0V, No load
I_{OZ}	OFF-State Output Current	–	–	20	μA	V_O = V_{DD} − 0V

Capacitance

(T_A = 25°C, V_{DD} = V_{SS} = 0V)

Symbol	Parameter	Min.	Max.	Unit	Condition
C x IN	Clock Input Capacitance	–	20	pF	f_C = 1 MHz Unmeasured Pins Returned to V_{SS}
C x OUT	Clock Output Capacitance	–	25	pF	
C_{IN}	Input Capacitance	–	10	pF	
C_{OUT}	Output Capacitance	–	20	pF	

A. C. Characteristics

Timing Requirements

Symbol	Parameter	Min.	Max.	Unit	Condition
t_{AW}	Address Strobe Width	90	–	ns	
t_{AS}	Address Setup Time	90	–	ns	

(Cont.)

Symbol	Parameter	Min.	Max.	Unit	Condition
t_{AH}	Address Hold Time	0	–	ns	
t_{CS}	Chip Select Setup Time	90	–	ns	
t_{CH}	Chip Select Hold Time	0	–	ns	
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	175	–	ns	
t_{RC}	Read Cycle Delay	500	–	ns	
RC	Read Cycle = $t_{AW} + t_{DID} + t_{DIW} + t_{RC}$	755	–	ns	
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	175	–	ns	
t_{WC}	Write Cycle Delay	500	–	ns	
WC	Write Cycle = $t_{AW} + t_{DOD} + t_{DOW} + t_{WC}$	755	–	ns	
t_{DS}	Data Setup Time	90	–	ns	
t_{DH}	Data Hold Time	60	–	ns	
t_{RA}*	Address Hold Time from $\overline{DISTR}$/DISTR	20	–	ns	
t_{RCS}*	Chip Select Hold Time from $\overline{DISTR}$/DISTR	20	–	ns	
t_{AR}*	$\overline{DISTR}$/DISTR Delay from Address	80	–	ns	
t_{CSR}*	$\overline{DISTR}$/DISTR Delay from Chip Select	80	–	ns	
t_{WA}*	Address Hold Time from $\overline{DOSTR}$/DOSTR	20	–	ns	
t_{WCS}*	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR	20	–	ns	
t_{AW}*	$\overline{DOSTR}$/DOSTR Delay from Address	80	–	ns	
t_{CSW}*	$\overline{DOSTR}$/DOSTR Delay from Chip Select	80	–	ns	
t_{MRM}	Master Reset Pulse Width	10	–	ns	

Timing Response

Symbol	Parameter	Min.	Max.	Unit	Condition
t_{CSS}	CSOUT Delay from Latch	–	90	ns	
t_{DD}	$\overline{DISTR}$/DISTR to Drive Disable Time	–	75	ns	All Outputs Loading 40 pF
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to DATA	–	175	ns	
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	100	300	ns	
t_{CSC}*	CSOUT Delay from Select	–	125	ns	

* Only applies when $\overline{ADS}$ is tied Low.

Other Timing

Baud Generator

Symbol	Parameter	Min.	Max.	Unit	Condition
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay	–	250	ns	40 pF loading
t_{BHD}	Baud Output Positive Edge Delay	–	250	ns	40 pF loading
t_{LW}	Baud Output Down Time	425	–	ns	40 pF loading
t_{HW}	Baud Output Up Time	330	–	ns	40 pF loading

Receiver

Symbol	Parameter	Min.	Max.	Unit	Condition
t_{SCD}	Delay from RCLK to Sample Time	–	2	us	
t_{SINT}	Delay from Stop Bit to Set Interrupt	–	3	RCLK Cycle	40 pF loading
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt	–	890	ns	40 pF loading

Transmitter

Symbol	Parameter	Min.	Max.	Unit	Condition
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR INT) to Reset Interrupt	–	890	ns	40 pF loading
t_{IRS}	Delay from Initial INTR Reset to Transmit Start	8	24	$\overline{BAUDOUT}$ Cycle	
t_{SI}	Delay from Initial Write to Interrupt	16	32	$\overline{BAUDOUT}$ Cycle	
t_{SS}	Delay from Stop to Next Start	–	1	us	40 pF loading
t_{STI}	Delay from Stop to Interrupt (THRE)	–	8	$\overline{BAUDOUT}$ Cycle	
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	–	890	ns	40 pF loading