



74ALVCH16843

18-bit bus-interface D-type latch; 3-State

Rev. 4 — 10 July 2024

Product data sheet

1. General description

The 74ALVCH16843 has two 9-bit D-type latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. The two sections of each register are controlled independently by the latch enable (nLE), clear (nCLR), preset (nPRE) and output enable (nOE) control gates.

When nOE is LOW, the data in the registers appear at the outputs. When nOE is HIGH, the outputs are in the high impedance OFF state. Operation of the nOE input does not affect the state of the flip-flops.

The 74ALVCH16843 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features and benefits

- Wide supply voltage range of 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at $V_{CC} = 3.0$ V.
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimize noise and ground bounce
- All data inputs have bushold
- Output drive capability 50 Ω transmission lines at 85 °C
- 3-state non-inverting outputs for bus oriented applications
- Complies with JEDEC standards:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH16843DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4. Functional diagram

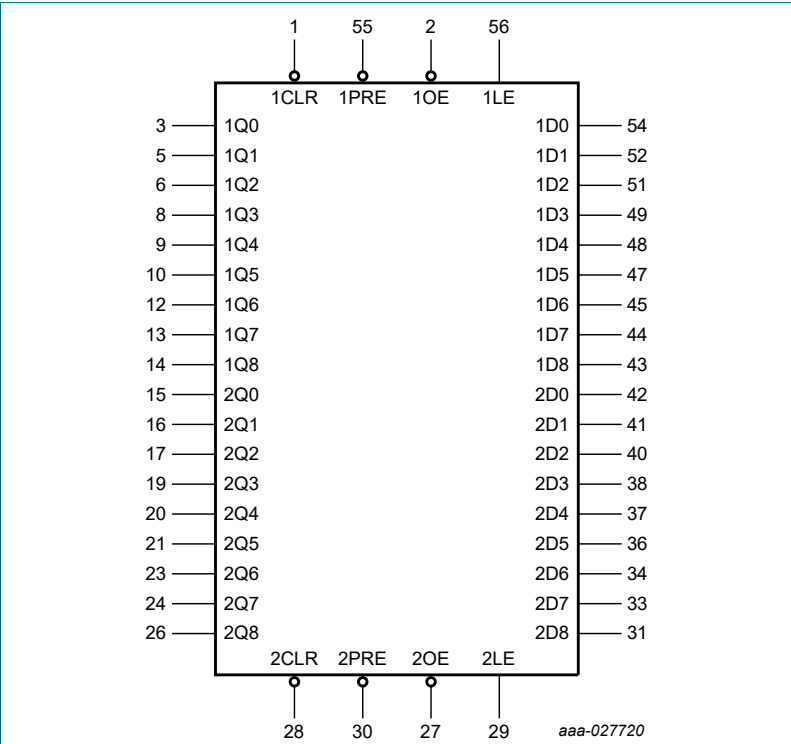


Fig. 1. Logic symbol

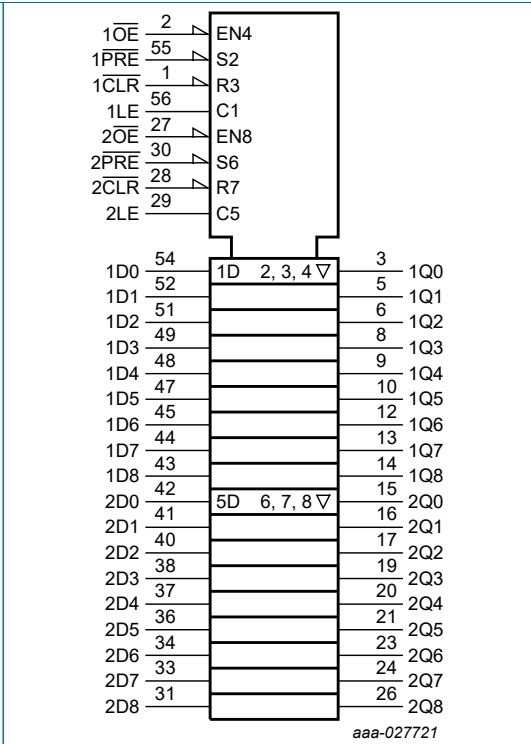


Fig. 2. IEC logic symbol

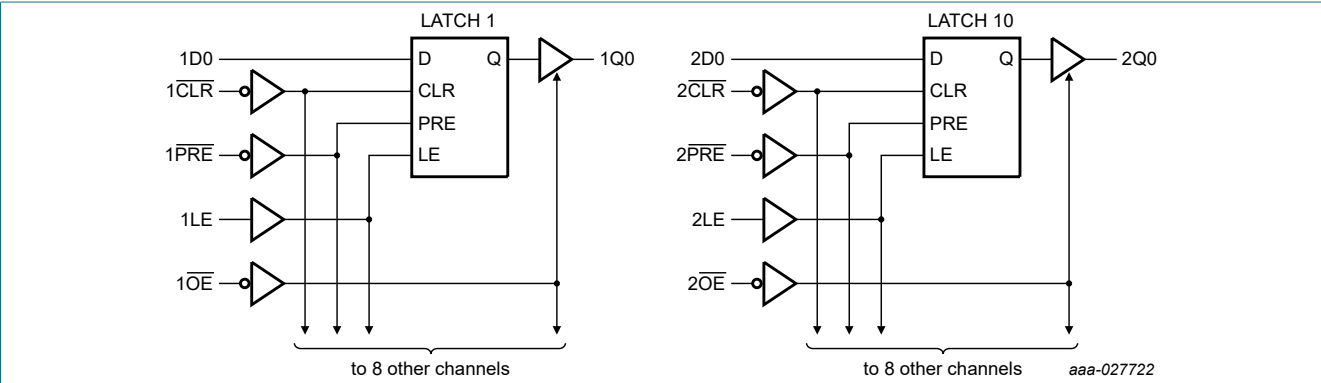


Fig. 3. Logic diagram

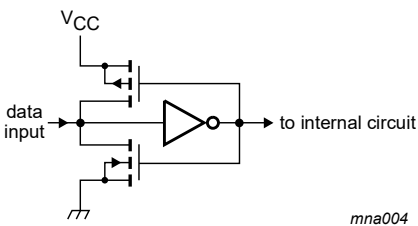
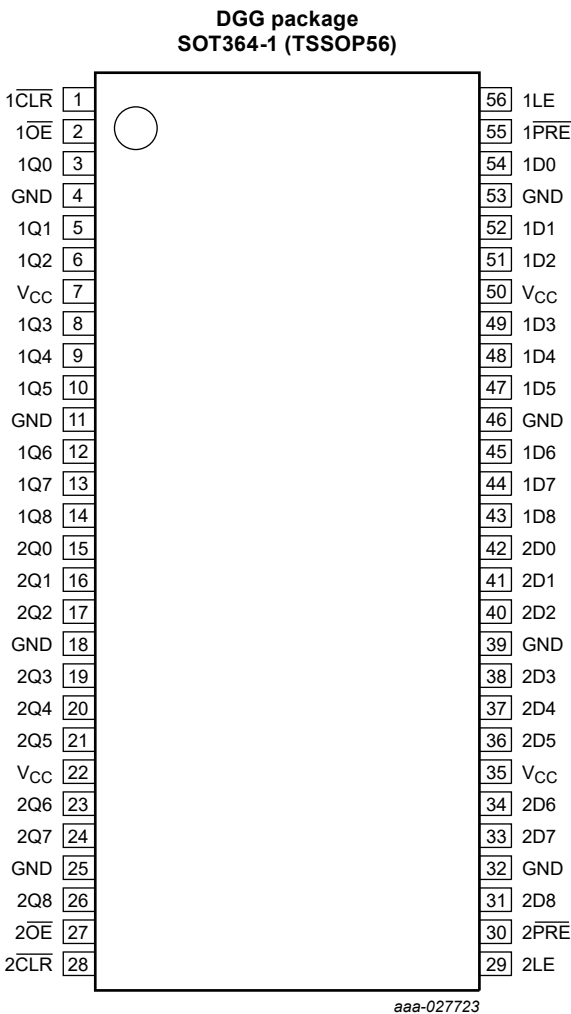


Fig. 4. Bushold circuit

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7, 1D8	54, 52, 51, 49, 48, 47, 45, 44, 43	data inputs
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7, 1Q8	3, 5, 6, 8, 9, 10, 12, 13, 14	data outputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7, 2D8	42, 41, 40, 38, 37, 36, 34, 33, 31	data inputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7, 2Q8	15, 16, 17, 19, 20, 21, 23, 24, 26	data outputs
1OE, 2OE	2, 27	output enable inputs (active LOW)
1PRE, 2PRE	55, 30	preset inputs (active LOW)
1CLR, 2CLR	1, 28	clear inputs (active LOW)
1LE, 2LE	56, 29	latch enable inputs (active HIGH)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V _{CC}	7, 22, 35, 50	supply voltage

6. Functional description

Table 3. Function selection

*H = HIGH voltage level; L = LOW voltage level;
X = don't care; NC = no change; Z = high-impedance OFF-state.*

Inputs					Output
nPRE	nCLR	nOE	nLE	nDn	nQn
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	NC
X	X	H	X	X	Z

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	For control pins [1]	-0.5	+4.6	V
		For data inputs [1]	-0.5	V _{CC} + 0.5	V
V _O	output voltage	[1]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage	maximum speed performance			
		C _L = 30 pF	2.3	2.7	V
		C _L = 50 pF	3.0	3.6	V
V _I	input voltage		0	V _{CC}	V
V _O	output voltage		0	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 3.0 V	-	20	ns/V
		V _{CC} = 3.0 V to 3.6 V	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 µA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I _O = -6 mA; V _{CC} = 2.3 V	V _{CC} - 0.3	V _{CC} - 0.08	-	V
		I _O = -12 mA; V _{CC} = 2.3 V	V _{CC} - 0.6	V _{CC} - 0.26	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	V _{CC} - 0.14	-	V
		I _O = -12 mA; V _{CC} = 3.0 V	V _{CC} - 0.6	V _{CC} - 0.09	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	V _{CC} - 1.0	V _{CC} - 0.28	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I _O = 6 mA; V _{CC} = 2.3 V	-	0.07	0.40	V
		I _O = 12 mA; V _{CC} = 2.3 V	-	0.15	0.70	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.14	0.40	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.27	0.55	V
I _I	input leakage current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} or GND	-	0.1	5	µA
I _{OZ}	OFF-state output current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	-	0.1	10	µA
I _{CC}	supply current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.2	40	µA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	150	750	µA
I _{BHL}	bus hold LOW current	V _{CC} = 2.3 V; V _I = 0.7 V	45	-	-	µA
		V _{CC} = 3.0 V; V _I = 0.8 V	75	150	-	µA
I _{BHH}	bus hold HIGH current	V _{CC} = 2.3 V; V _I = 1.7 V	-45	-	-	µA
		V _{CC} = 3.0 V; V _I = 2.0 V	-75	-175	-	µA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V	500	-	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6 V	-500	-	-	µA
C _I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t _{pd}	propagation delay	nDn to nQn; see Fig. 5 [2]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.2	4.3	ns
		V _{CC} = 2.7 V	1.0	2.3	4.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.1	3.5	ns
		nLE to nQn; see Fig. 6				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.3	4.6	ns
		V _{CC} = 2.7 V	1.0	2.1	3.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.0	3.5	ns
		nPRE to nQn; see Fig. 5 [3]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.5	4.8	ns
		V _{CC} = 2.7 V	1.0	2.6	4.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.2	3.8	ns
		nCLR to nQn; see Fig. 5				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.5	4.8	ns
		V _{CC} = 2.7 V	1.0	2.5	4.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.3	3.9	ns
t _{en}	enable time	nOE to nQn; see Fig. 9 [3]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.8	5.8	ns
		V _{CC} = 2.7 V	1.0	3.0	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.5	4.4	ns
t _{dis}	disable time	nOE to nQn; see Fig. 9 [4]				
		V _{CC} = 2.3 V to 2.7 V	1.1	2.2	4.3	ns
		V _{CC} = 2.7 V	1.3	2.8	4.4	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	2.6	4.0	ns
t _{su}	set-up time	nDn to nLE; see Fig. 7				
		V _{CC} = 2.3 V to 2.7 V	0.5	-0.1	-	ns
		V _{CC} = 2.7 V	0.5	-0.3	-	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	0.0	-	ns
t _h	hold time	nDn to nLE; see Fig. 7				
		V _{CC} = 2.3 V to 2.7 V	0.9	0.5	-	ns
		V _{CC} = 2.7 V	0.9	0.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	0.9	0.5	-	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t _w	pulse width	nLE HIGH; see Fig. 6				
		V _{CC} = 2.3 V to 2.7 V	1.5	0.5	-	ns
		V _{CC} = 2.7 V	1.5	0.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	0.5	-	ns
		nPRE LOW; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V	1.5	0.5	-	ns
		V _{CC} = 2.7 V	1.5	0.6	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	0.5	-	ns
		nCLR LOW; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V	1.5	0.5	-	ns
		V _{CC} = 2.7 V	1.5	0.5	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	0.5	-	ns
t _{rec}	recovery time	nPRE to nLE; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V	0.5	1.1	-	ns
		V _{CC} = 2.7 V	0.8	-0.2	-	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	0.4	-	ns
		nCLR to nLE; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V	0.5	1.0	-	ns
		V _{CC} = 2.7 V	0.6	-0.4	-	ns
		V _{CC} = 3.0 V to 3.6 V	0.8	0.2	-	ns
C _{PD}	power dissipation capacitance	per latch; V _I = GND to V _{CC} [5]				
		transparent mode; outputs enabled	-	17	-	pF
		transparent mode; outputs disabled	-	3	-	pF
		clocked mode; outputs enabled	-	19	-	pF
		clocked mode; outputs disabled	-	9	-	pF

[1] Typical values are measured at T_{amb} = 25 °C
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.

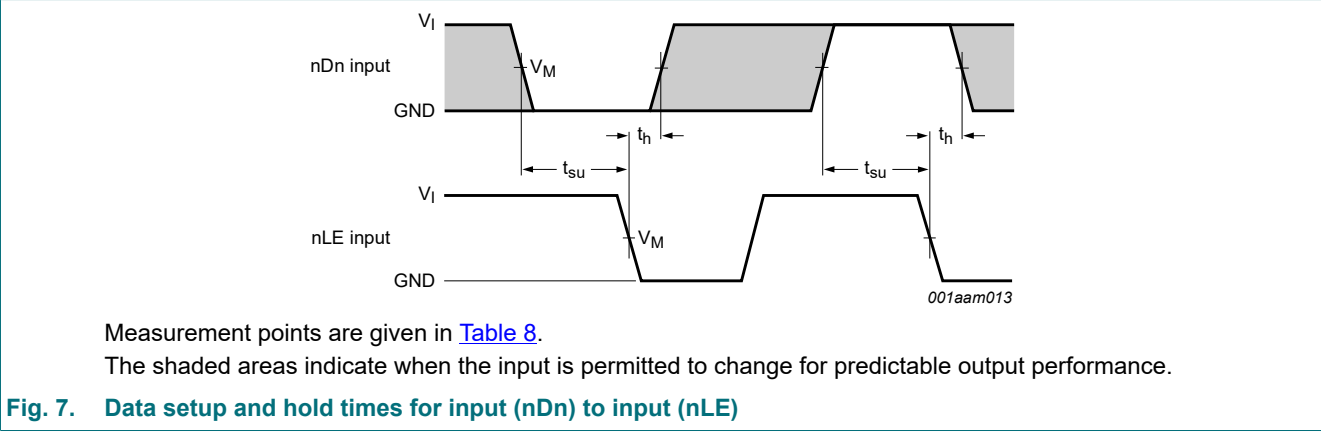
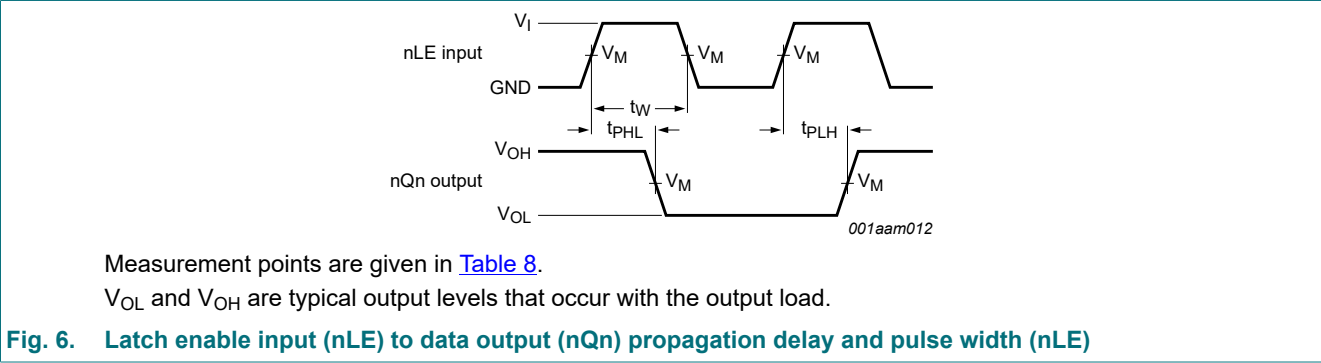
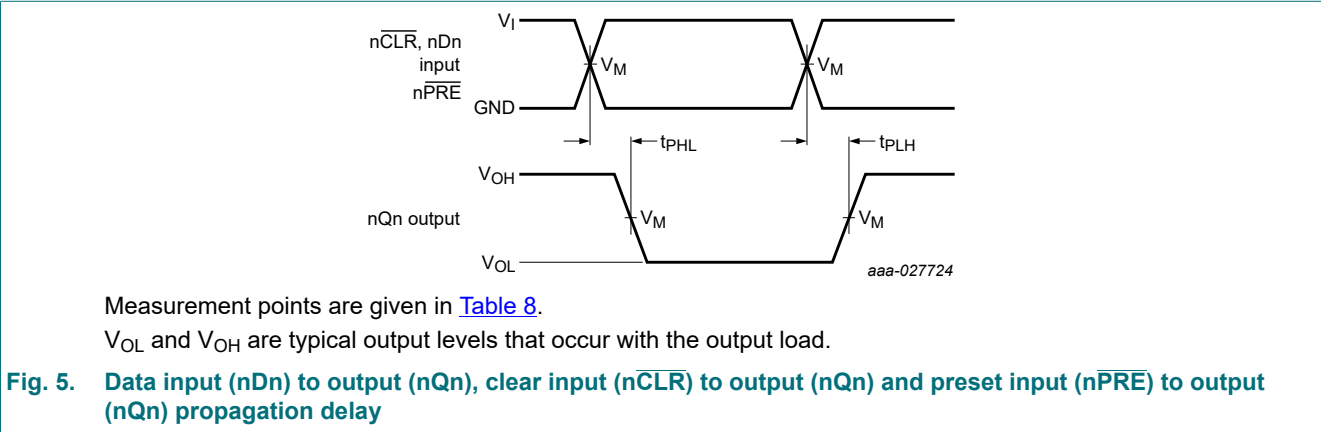
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

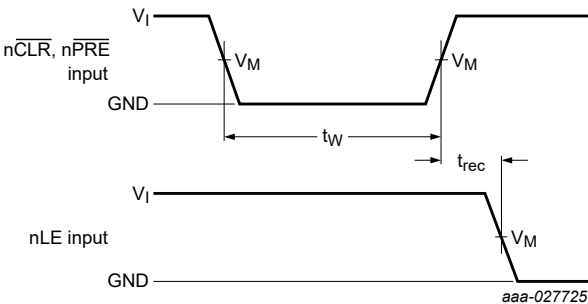
[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
Σ(C_L × V_{CC}² × f_o) = sum of outputs.

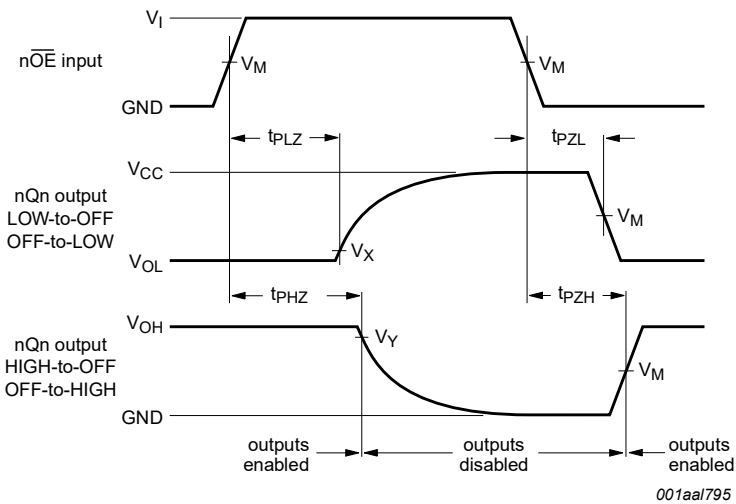
10.1. Waveforms and test circuit





Measurement points are given in [Table 8](#).

Fig. 8. Clear ($\overline{nCLR}$) and preset ($\overline{nPRE}$) pulse width, the clear ($\overline{nCLR}$) and preset ($\overline{nPRE}$) to latch (nLE) recovery time



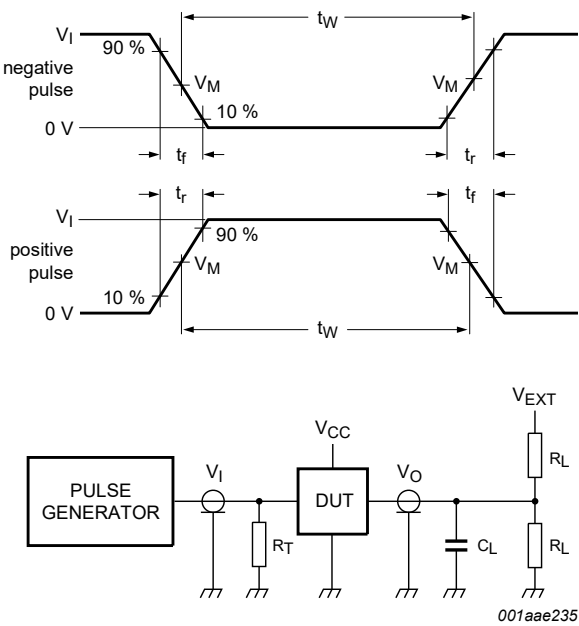
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 9. 3-State enable and disable times

Table 8. Measurement points

Input			Output		
V_{CC}	V_I	V_M	V_M	V_x	V_y
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_L = Load resistance;
 C_L = Load capacitance including jig and probe capacitance;
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;
 V_{EXT} = External voltage for measuring switching times.

Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Input			Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	500 Ω	30 pF	GND	$2 \times V_{CC}$	open
2.7 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	$2 \times V_{CC}$	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	500 Ω	50 pF	GND	$2 \times V_{CC}$	open

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

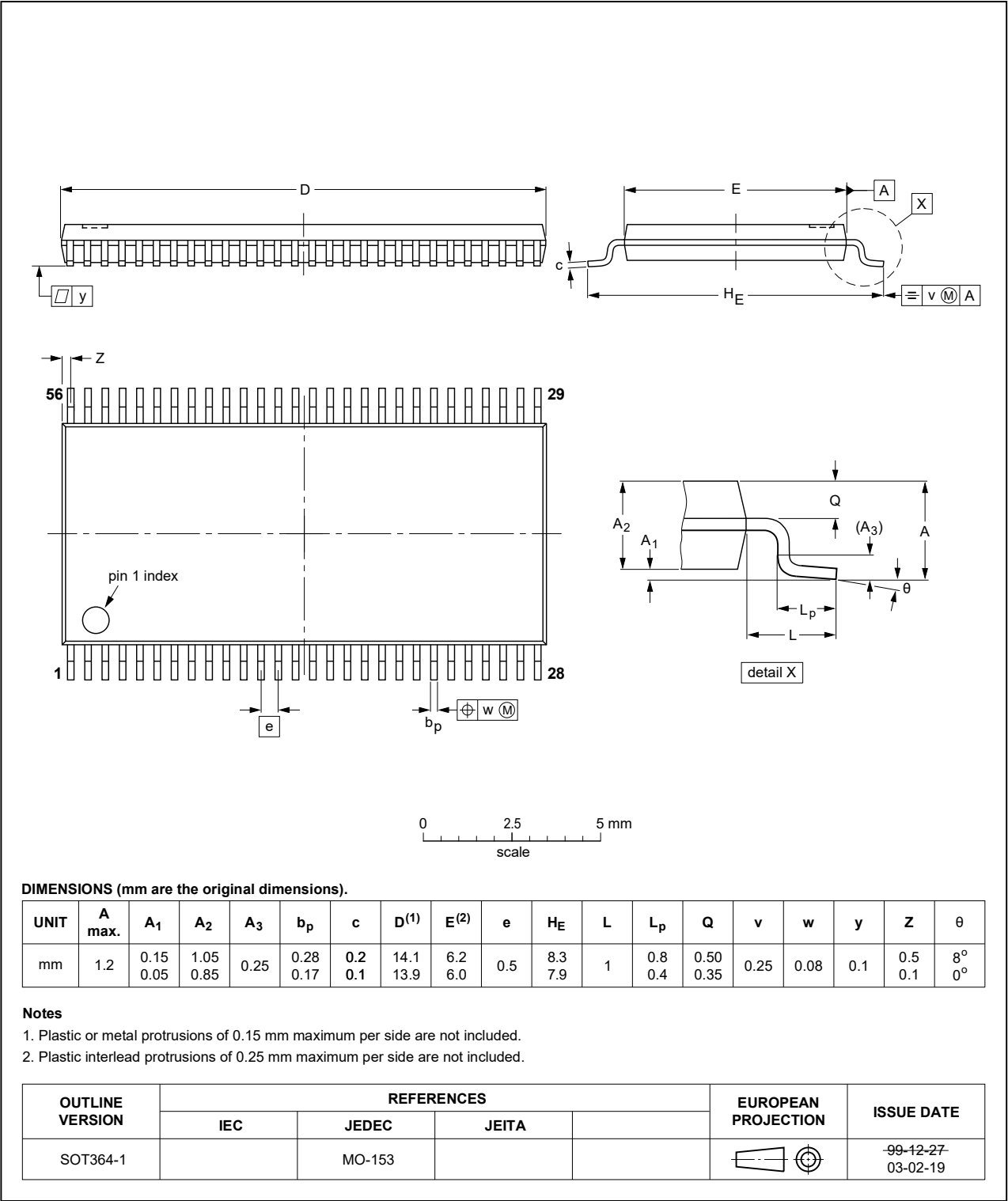


Fig. 11. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16843 v.4	20240710	Product data sheet	-	74ALVCH16843 v.3
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - Table 4: P_{tot} total power dissipation updated.			
74ALVCH16843 v.3	20171120	Product data sheet	-	74ALVCH16843 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate.			
74ALVCH16843 v.2	19980804	Product specification	-	74ALVCH16843 v.2
74ALVCH16843 v.1	19980804	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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