Pulse Width Modulation Amplifiers

RoHS COMPLIANT

FEATURE

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The SA12 is a pulse width modulation amplifier that can supply 3000W to the load. An internal 400kHz oscillator requires no external components. The clock input stage divides the oscillator frequency by two, which provides the 200 kHz switching frequency. External oscillators may also be used to lower the switching frequency or to synchronize multiple amplifiers. Current sensing is provided for each half of the H-bridge giving amplitude and direction data. A shutdown input turns off all four drivers of the H-bridge output. A high side current limit and the programmable low side current limit protect the amplifier from shorts to supply or ground in addition to load shorts. The H-bridge output MOSFETs are protected from thermal overloads by directly sensing the temperature of the die. The 12-pin hermetic MO-127 power package occupies only 3 square inches of board space.

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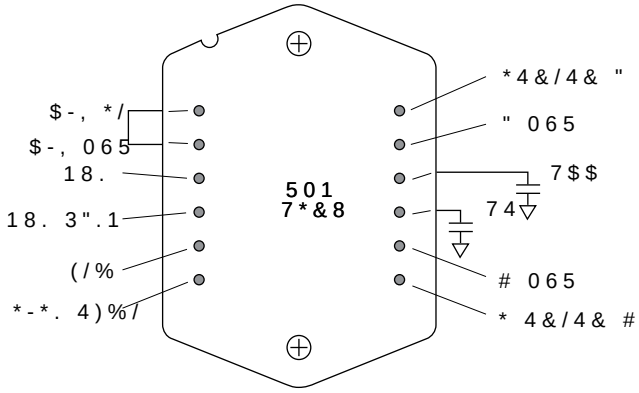

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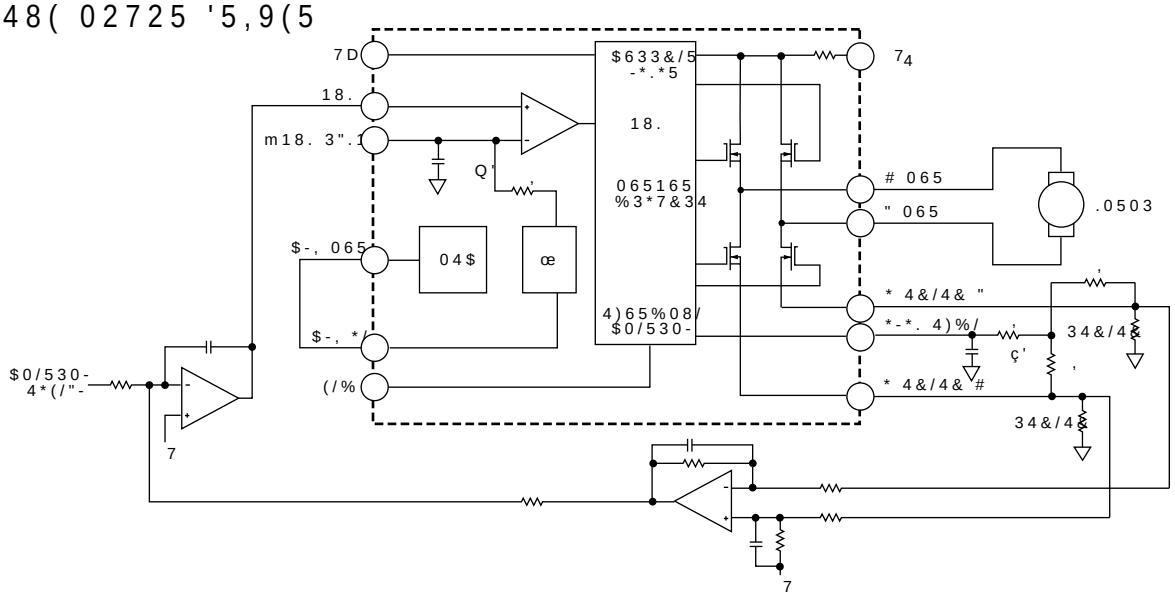

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SUPPLY VOLTAGE, $+V_S$	200V
SUPPLY VOLTAGE, V_{CC}	16V
POWER DISSIPATION, internal	250W[1]
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[3]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C
INPUT VOLTAGE, +PWM	0 to +11V
INPUT VOLTAGE, –PWM	0 to +11V
INPUT VOLTAGE, I_{LIM}	0 to +10V

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PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
CLOCK (CLK)					
CLK OUT, high level[4]	I_{OUT} 1mA	4.8		5.3	V
CLK OUT, low level[4]	I_{OUT} 1mA	0		.4	V
FREQUENCY		392	400	408	kHz
RAMP, center voltage			5		V
RAMP, P-P voltage			4		V
CLK IN, low level[4]		0		.9	V
CLK IN, high level[4]		3.7		5.4	V
OUTPUT					
TOTAL R_{ON}[4]				.4	
EFFICIENCY, 10A output	V_S = 200V		97		%
SWITCHING FREQUENCY	OSC in ÷ 2	196	200	204	kHz
CURRENT, continuous[4]	65°C case	15			A
CURRENT, peak[4]		20			A
POWER SUPPLY					
VOLTAGE, V_S	Full temperature range	16	120	200	V
VOLTAGE, V_{CC}	Full temperature range	14	15	16	V
CURRENT, V_{CC}	I_{OUT} = 0			125	mA
CURRENT, $V_{CC,}$ shutdown				80	mA
CURRENT, V_S	No Load			200	mA
I_{LIM}/SHUTDOWN					
TRIP POINT		90		110	mV
INPUT CURRENT				100	nA
THERMAL[3]					
RESISTANCE, junction to case	Full temperature range, for each die			1	°C/W
RESISTANCE, junction to air	Full temperature range		12		°C/W
TEMPERATURE RANGE, case	Meets full range speci cations	–25		+85	°C

NOTES:
1. Each of the two active output transistors can dissipate 125W.
2. Unless otherwise noted: T_C = 25°C, V_S, V_{CC} at typical speci cation.
3. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
4. Guaranteed but not tested.

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The SA12 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

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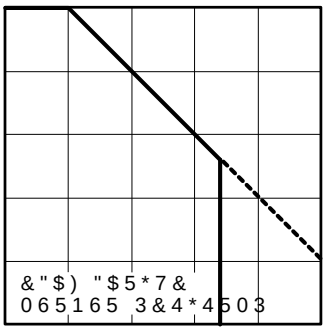

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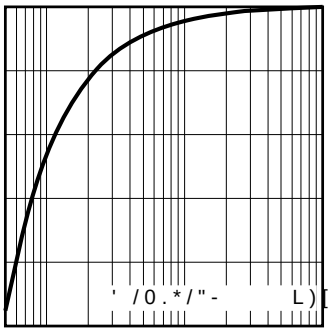

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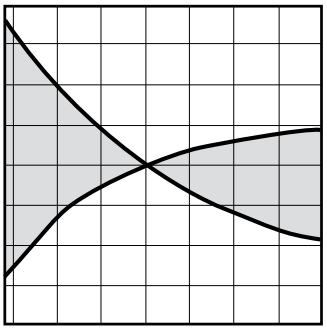

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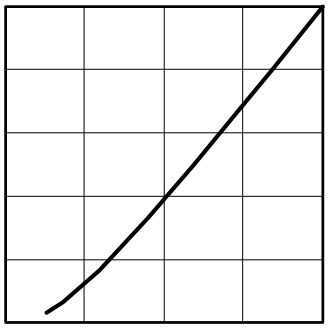

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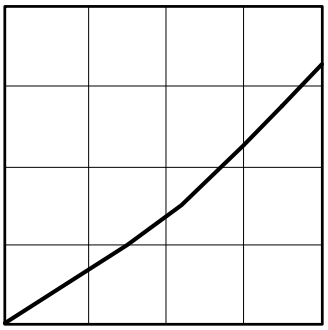

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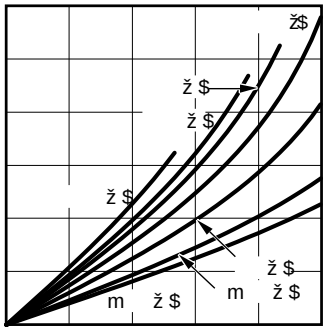

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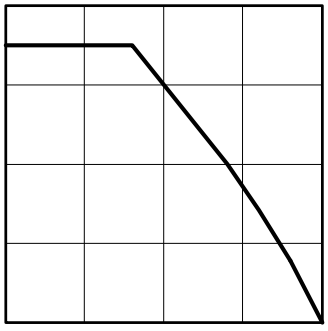

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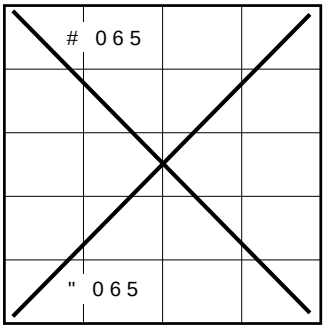

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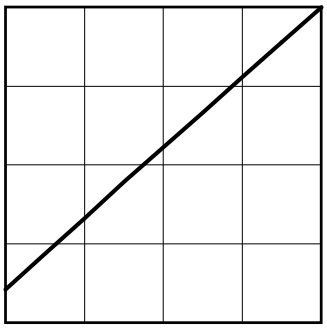

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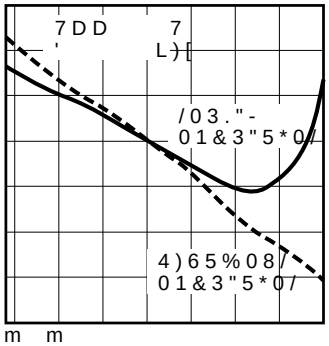

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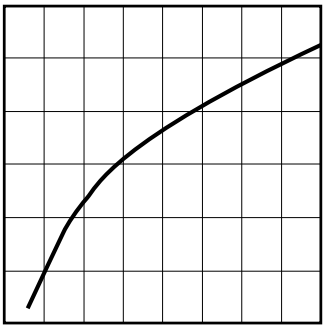

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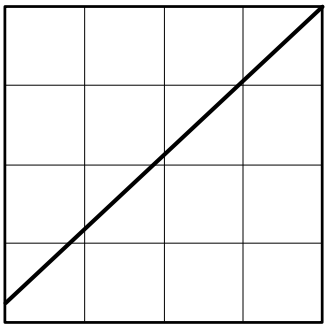

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Please read Application Note 30 on "PWM Basics". Refer to Application Note 1 "General Operating Considerations" for helpful information regarding power supplies, heat sinking and mounting. Visit www.Cirrus.com for design tools that help automate pwm lter design; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

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The clock frequency is internally set to a frequency of approximately 400kHz. The CLK OUT pin will normally be tied to the CLK IN pin. The clock is divided by two and applied to an RC network which produces a ramp signal at the –PWM/RAMP pin. An external clock signal can be applied to the CLK IN pin for synchronization purposes. If a clock frequency lower than 400kHz is chosen an external capacitor must be tied to the –PWM/RAMP pin. This capacitor, which parallels an internal capacitor, must be selected so that the ramp oscillates 4 volts p-p with the lower peak 3 volts above ground.

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The full bridge driver may be accessed via the pwm input comparator. When +PWM > -PWM then A OUT > B OUT. A motion control processor which generates the pwm signal can drive these pins with signals referenced to GND.

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A xed internal current limit senses the high side current. Should either of the outputs be shorted to ground the high side current limit will latch off the output transistors. The temperature of the output transistors is also monitored. Should a fault condition raise the temperature of the output transistors to 165°C the thermal protection circuit will latch off the output transistors. The latched condition can be cleared by either recycling the V_{cc} power or by toggling the I LIMIT/SHDN input with a 10V pulse. See Figures A and B. The outputs will remain off as long as the shutdown pulse is high (10V).

When supply voltage is over 100V, these circuits may not protect the FET switches in the case of short circuits directly at the pins of the ampli er. However, a small inductance between the ampli er and the short circuit will limit current rise time and the protection circuits will be effective. A pair of 12 inch wires is adequate inductance.

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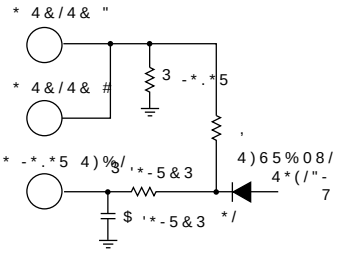
There are two load current sensing pins, I SENSE A and I SENSE B. The two pins can be shorted in the voltage mode connection but both must be used in the current mode connection (see gures A and B). It is recommended that R_{LIMIT} resistors be non-inductive. Load current ows in the I SENSE pins. To avoid errors due to lead lengths connect the I LIMIT/SHDN pin directly to the R_{LIMIT} resistors (through the lter network and shutdown divider resistor) and connect the R_{LIMIT} resistors directly to the GND pin.



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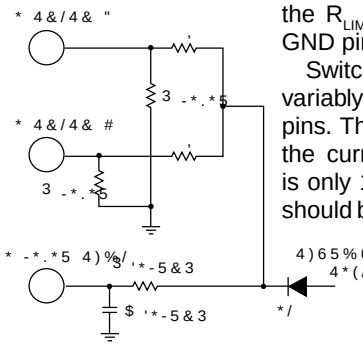

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Switching noise spikes will invariably be found at the I SENSE pins. The noise spikes could trip the current limit threshold which is only 100 mV. R_{FILTER} and C_{FILTER} should be adjusted so as to reduce the switching noise well below 100 mV to prevent false current limiting. The sum of the DC level plus the noise peak will determine the current limiting value. As in most switching circuits it may be difficult to determine the true noise amplitude without careful attention to grounding of the oscilloscope probe. Use the shortest possible ground lead for the probe and connect exactly at the GND terminal of the ampli er. Suggested starting values are C_{FILTER} = .01uF, R_{FILTER} = 5k .

The required value of R_{LIMIT} in voltage mode may be calculated by:

$$R_{LIMIT} = .1\ V / I_{LIMIT}$$

where R_{LIMIT} is the required resistor value, and I_{LIMIT} is the maximum desired current. In current mode the required value of each R_{LIMIT} is 2 times this value since the sense voltage is divided down by 2 (see Figure B). If R_{SHDN} is used it will further divide down the sense voltage. The shutdown divider network will also have an effect on the lter circuit.

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Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The Vs supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of at least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The bypass capacitors must be physically connected directly to the power supply pins. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the Vcc supply are less stringent, but still necessary. A .1µF to .47µF ceramic capacitor connected directly to the Vcc pin will suffice.

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The high side of the all N channel H-bridge is driven by a bootstrap circuit. For the output circuit to switch high, the low side circuit must have previously been switched on in order to charge the bootstrap capacitor. Therefore, if the input signal to the SA12 demands a 100% duty cycle upon start-up the output will not follow and will be in a tri-state (open) condition. The ramp signal must cross the input signal at some point to correctly determine the output state. After the ramp crosses the input signal one time the output state will be correct thereafter. In addition, if during normal operation the input signal drives the SA12 beyond its linear modulation range (approximately 95%) the output will jump to 100% modulation.

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For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.
For inquiries via email, please contact apex.support@cirrus.com.
International customers can also request support by contacting their local Cirrus Logic Sales Representative.
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